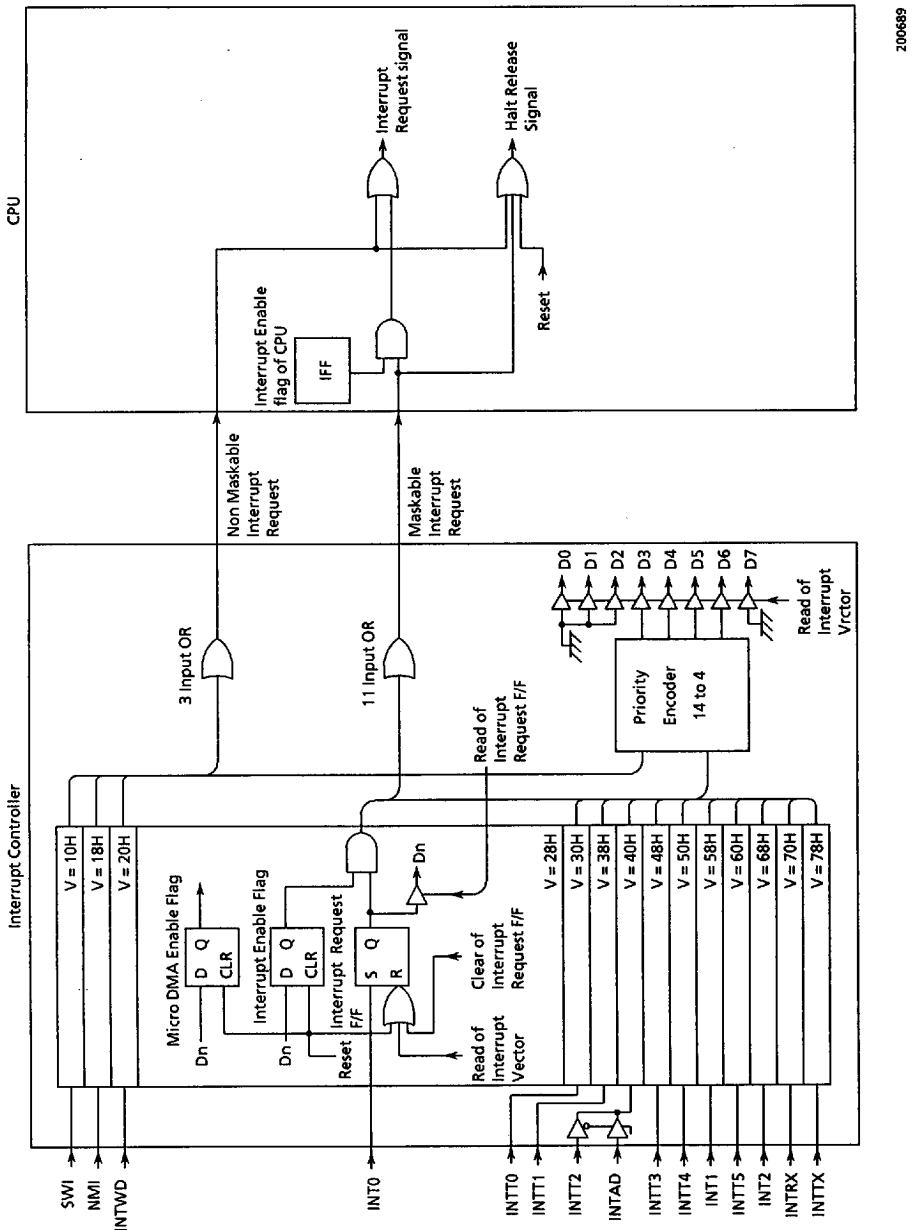

Figure 3.3 (8) Block Diagram of Interrupt Controller

The interrupt enable flags provided for all interrupt request channels are assigned to the memory address FFE6H or FFE7H. Setting any of these flags to "1" enables an interrupt of the respective channel. These flags are initialized to "0" by resetting.

Clear the interrupt enable flag in the DI status.

The micro DMA enable flag also provided for each interrupt request channel is assigned to the memory address FFE7H or FFE8H. The interrupt processing for each channel is placed in the micro DMA processing mode by setting this flag to "1". This flag is initialized to "0" (general purpose interrupt processing mode) by resetting.

Figure 3.3. (9) shows the bit configuration of the interrupt enable flags and micro DMA enable flags.

Interrupt by Timer 2 (INTT2) and that by A/D converter (INTAD) use a common interrupt request channel. The interrupt controller first accepts INTT2 after a reset. INTAD can be used by setting the "INTT2/INTAD selection bit" (ADIS: Bit 3 of memory address FFE7H) to "1".

The function of the external interrupts is as follows.

Interrupt	Common terminal	Mode	How to set
$\overline{NMI}$	—	Falling edge	——
INT0	P80	Level	P8CR<EDGE> = 0
		Rising edge	P8CR<EDGE> = 1
INT1	P81	Rising edge	T4MOD<CAPM1, 0> = 0, 0 or 0, 1 or 1, 1
		Falling edge	T4MOD<CAPM1, 0> = 1, 0
INT2	P82	Rising edge	——

For the pulse width for the external interrupts, see section 4.8 "Interrupt Operation".

Attention should be paid to the following three modes having special circuits:

INT0 Level mode	IF INT0 is not an edge-based interrupt, the function of Interrupt Request Flip-flop is canceled. Therefore the interrupt request signal must be held until the interrupt request is acknowledged by the CPU. A change in the mode (edge to level) automatically clears the interrupt request flag. When the CPU has been put in the interrupt response sequence with INT0 level mode, it is necessary to leave INT0 at "1" until the second bus cycle of the interrupt response sequence is completed. Also, "1" must always be held until HALT is cleared when using the INT0 level mode to clear HALT. (Use care to prevent noise changing "1" back to "0".) When switching from the level mode to the edge mode, the interrupt request flag set in the level mode is not cleared; therefore, use the following sequence to clear the interrupt request flag. DI LD (0FFD1H), 01H: switch from level to edge LD (0FFC3H), 05H: clear interrupt request flag EI
INTAD level mode	The Interrupt Request Flip-flop can be cleared only by resetting or reading the register that stores A/D conversion value, and cannot be cleared by an instruction. A change in the interrupt source (between INTAD and INTT2) automatically clears the interrupt request flag.
INTRX level mode	The Interrupt Request Flip-flop is cleared only by resetting or reading the serial channel receiving buffer, and not by an instruction.

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