FEATURES

- **On-Chip ALBO Diode**
- **Clock Shutdown Circuit (RPT-81)**
- **On-Chip Voltage Regulator (RPT-81)**
- **Low Power Operation (100mW)**
- **Pin-Compatible with XR-C277**
- **Improved Pre-Amplifier Response (RPT-82)**

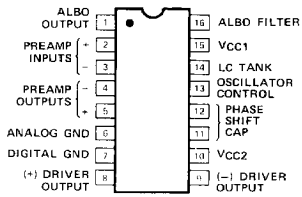
GENERAL DESCRIPTION

The PMI PCM Repeater Circuits are monolithic integrated circuits which perform all the active functions required for a regenerative repeater operating at 1.544-2.048 Mega-bits per second (Mbps) data rates on PCM lines.

In a PCM carrier system, coded information is transmitted over paired cables by the presence or absence of pulses in specified time slots. The RPT-81/RPT-82 regenerate all pulses that meet threshold requirements without inserting pulses incorrectly during empty time slots.

Additional system functions have been incorporated on-chip. These include an Automatic Line Build Out (ALBO) circuit that compensates for up to 36dB of line loss and an oscillator control pin that permits injectioned-locked (free-running) or pulsed-tank operation. The RPT-81 also incorporates an automatic clock shutdown circuit. The clock shutdown inhibits the clock amplifier when the input signal is too low to provide reliable data transmission.

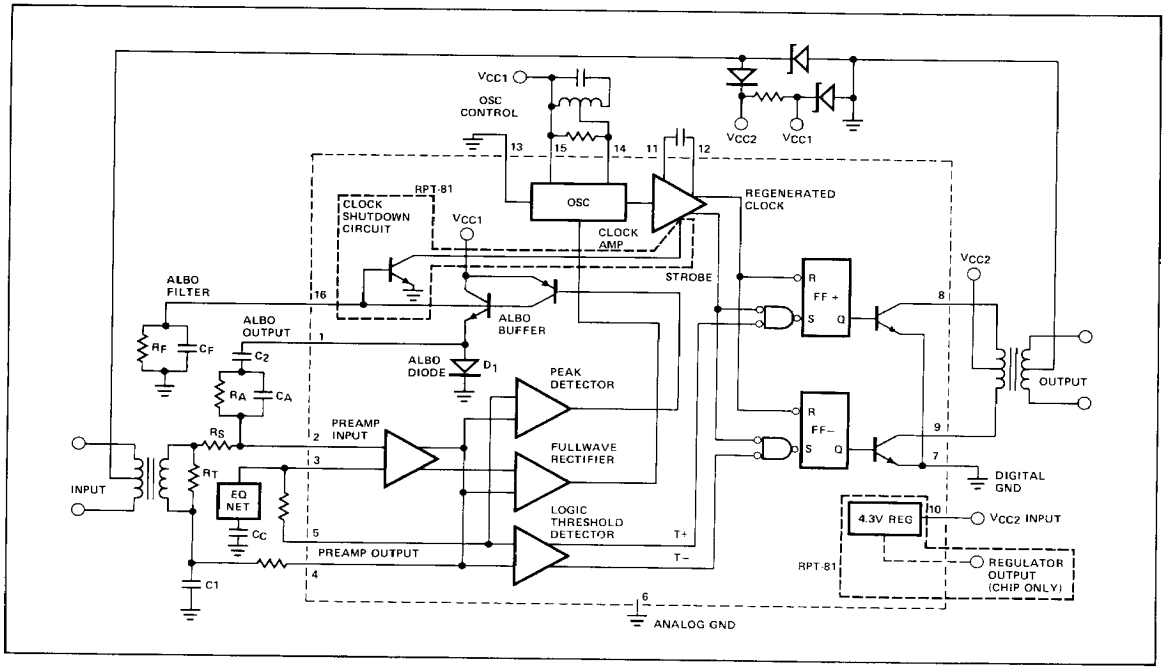
PIN CONNECTIONS & ORDERING INFORMATION



16-PIN HERMETIC DUAL-IN-LINE
(Q-Suffix)
RPT-81FQ
RPT-82FQ

*The on-chip (RPT-81) 4.3V regulated output voltage is not available for external use in 16-Pin package.

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Biopolar pulse transmission, the transmission of alternately positive and negative pulses, is used on repeatered lines to remove the DC component from the unipolar PCM pulse train. This also places the principle energy components in the 0-1.544MHz band, as opposed to the 0-3.088MHz band for the unipolar pulse train. The absence of a DC component in the bipolar pulse train permits the repeater to be transformer coupled to the line and helps to prevent time shifting of the regenerator firing level with variation in input pulse density.

The bipolar PCM pulse train is transformer coupled into the preamplifier as shown in the RPT-81/RPT-82 functional block diagram. The secondary of the input transformer is loaded with the proper terminating resistor R_T to match the line impedance. One side of the transformer secondary is AC coupled to ground by capacitor C1, the other side of the secondary winding is in series with resistance R_S. Resistor R_S and RC network R_AC_A are AC coupled to the ALBO output by capacitor C2. The impedance from the ALBO output to ground is governed by the amount of current through the ALBO diode. R_S in series with R_AC_A provides maximum signal attenuation when maximum current flows through the ALBO diode. When minimum current flows through the ALBO, diode C2 is effectively isolated from ground and the input signal attenuation is minimal. The RPT-81/RPT-82 ALBO circuits can compensate for 36dB of line loss.

The preamplifier amplifies the signal and applies it to the three comparators labeled *logic threshold detector, fullwave rectifier,* and *peak detector,* respectively. Each comparator is set to trigger on both positive and negative pulses. Each comparator trips at a different threshold. The logic threshold is set to trip at the 50% point, the fullwave rectifier trips at the 65% point, and the peak detector trips at peak amplitude. Thresholds and waveforms are drawn on the RPT-81/RPT-82 waveforms and thresholds diagram.

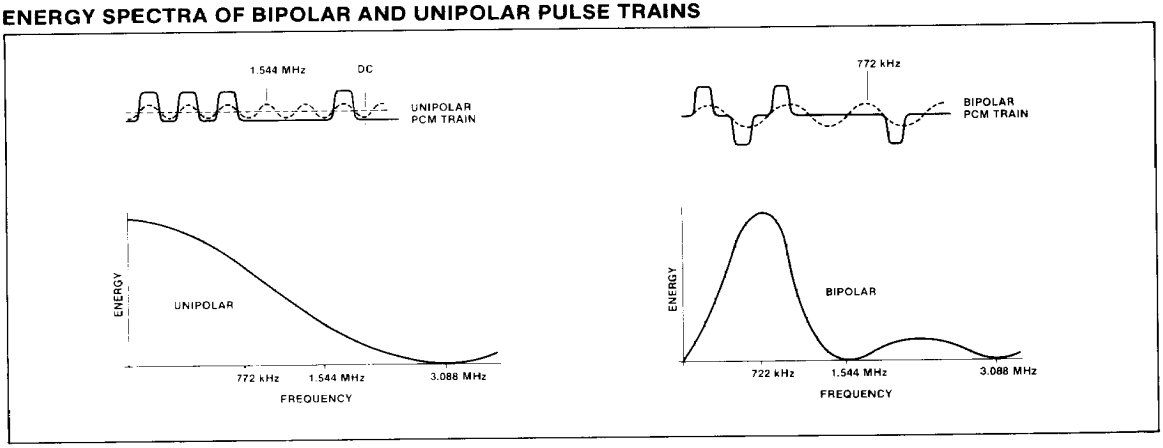
The peak detector output charges the capacitor of the ALBO filter. The voltage on this capacitor causes a relatively constant current to flow through D1 by means of the emitter follower ALBO buffer. A decaying voltage on the ALBO filter enables the clock shutdown circuit when there is no input signal. The clock shutdown circuit turns off the clock amplifier so that neither the regenerated clock nor the strobe outputs are sent to FF+ or FF– flip flops.

The fullwave detector output injection locks the oscillator to the input frequency. The clock amplifier shapes the oscillator output and shifts it in time. To optimize noise rejection, select the phase-shift capacitor (0 to 30pF, 10pF typical) such that the strobe pulse occurs at the center of the incoming pulses.

The logic threshold detector produces an output on the T+ line for a positive pulse and an output on the T– line for a negative pulse. The T+ line enables the NAND gate of FF+ and the T– line enables the NAND gate of FF–. A T+ output pulse from the logic threshold detector is ANDed with the strobe pulse to set the FF+ flip flop which turns on its corresponding output transistor, causing current to flow through one half of the output transformer primary. A positive output pulse results. Similarly, A T– output pulse and a strobe pulse are ANDed to set the FF– flip flop, thus causing a negative output pulse. The flip flops are turned off (and the output pulse terminated) by the regenerated clock pulse. In this way the output pulse is controlled by the oscillator tank circuit and not the incoming pulse.

When pin 13 is grounded, the full-wave detector injection-locks the oscillator to the input frequency. With pin 13 ungrounded, the system operates in the "pulsed tank" mode.

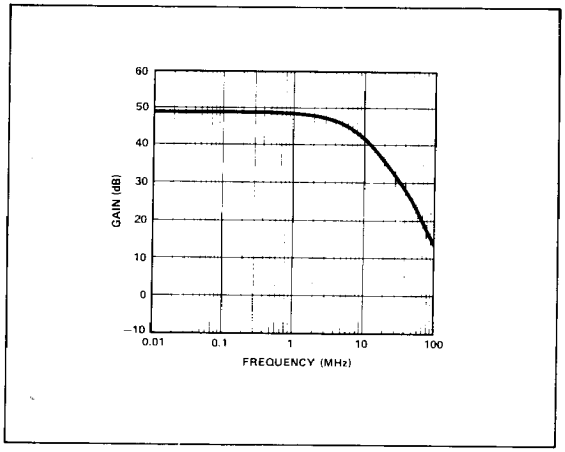
ENERGY SPECTRA OF BIPOLAR AND UNIPOLAR PULSE TRAINS



PREAMPLIFIER

The preamplifier has wideband frequency response in order to amplify the 1.544Mb/sec pulse train. In addition it has well-behaved roll-off characteristics to simplify the application of feedback.

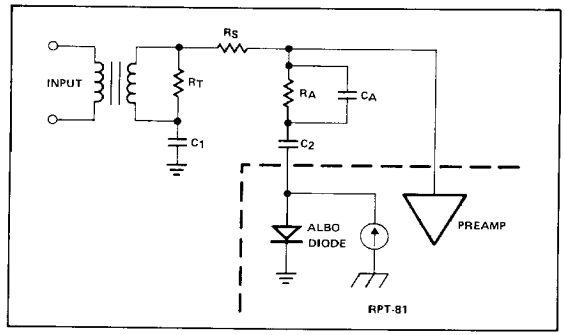
PREAMPLIFIER FREQUENCY RESPONSE



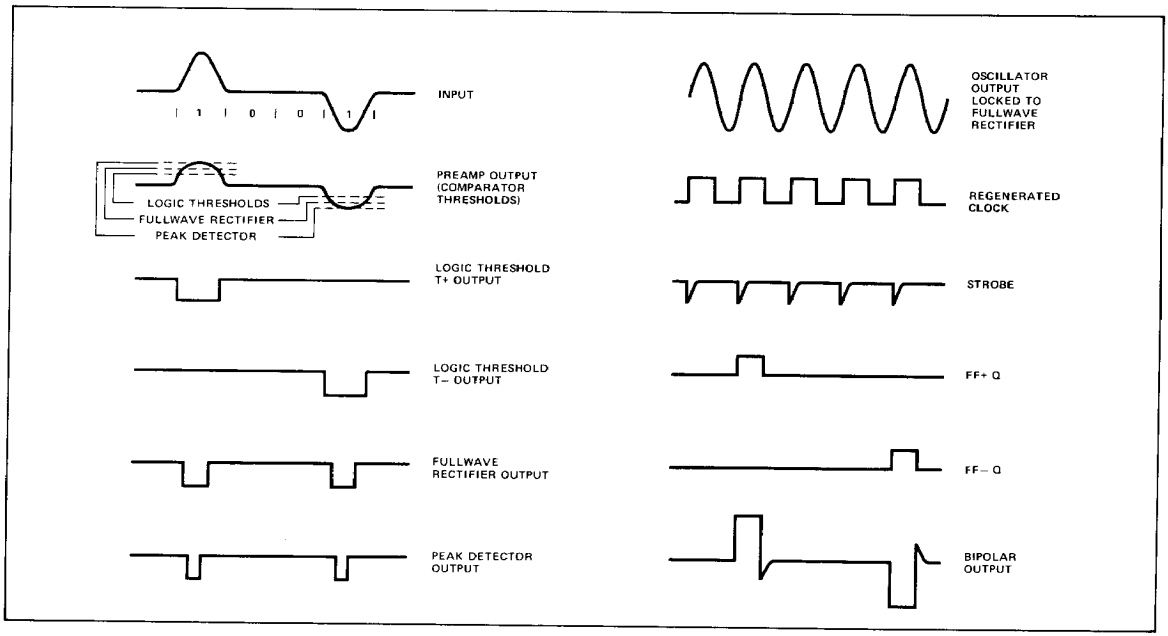
AUTOMATIC LINE BUILDOUT EXTERNAL CIRCUIT

The external circuitry required to achieve automatic line buildout must attenuate the signal while simultaneously matching the transformer to the line. Capacitors C1 and C2 are blocking capacitors. R_A and C_A in parallel shape the frequency response of the attenuator network to compensate for the reactive source impedance of the line. Resistor R_T provides an input match to this line. R_S is the series branch of the attenuator.

AUTOMATIC LINE BUILDOUT EXTERNAL CIRCUITRY



WAVEFORMS AND THRESHOLDS



ABSOLUTE MAXIMUM RATINGS

Pin 10 to Pin 7 or 6 ..... 16.0V, −0.2V
Pin 15 to Pin 7 or 6 ..... 8.0V, −0.2V
Maximum Voltage at Pins 8 or 9 ..... 30V, −0.2V
Maximum Voltage
at Pins 2, 3, 4, 5, 11, 12, 14 ..... V_{CC2}
Maximum Sinking Current at Pin 8 or 9 ..... 300mA
Operating Temperature Range ..... −40° C to +85° C
Storage Temperature Range ..... −65° C to +150° C
Power Dissipation 500mW
Lead Soldering Temperature ..... 300° C

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
16-Pin Hermetic DIP (Q)	100° C	10mW/° C

ELECTRICAL CHARACTERISTICS at V_{CC1} = 4.4V, V_{CC2} = 6.8V, −40° C ≤ T_A ≤ +85° C, unless otherwise noted.

$V_{pin\ 6} = V_{pin\ 7} = V_{pin\ 13}$ = GND.

PARAMETER	SYMBOL	CONDITIONS	RPT-81 MIN	RPT-81 TYP	RPT-81 MAX	RPT-82 MIN	RPT-82 TYP	RPT-82 MAX	UNITS
SUPPLY									
Differential Output Voltage (Low Level)	V_{CC1}	Power Supply Range over which device will function	4.3	4.4	4.7	4.1	4.4	4.7	V
Power Supply Voltage	V_{CC2}	Power Supply Range over wich device will function	5.0	6.8	7.25	5.0	6.8	7.5	V
Supply Current	I_{CC1}	T_A = 25° C, Note 1	—	8.5	—	—	8.5	—	mA
Supply Current	I_{CC2}	T_A = 25° C, Note 1	—	2.5	—	—	2.5	—	mA
PREAMPLIFIER									
Total Supply Current	$I_{CC1} + I_{CC2}$	T_A = 25° C, Note 1	6.0	11.0	13	6.0	11.0	13	mA
Preamplifier Open-Loop $\frac{\Delta V_{pin\ 5}}{\Delta V_{pin\ 2}}$	A_0	Measure $\Delta V_{pin\ 2}$ necessary to change pins from 1.8V to 3.3V	44	48	52	44	48	52	dB
Preamplifier Bandwidth	B_W	3dB Points	—	5	—	—	7	—	MHz
Preamplifier Input Impedance	Z_{IN}	Shunted by 2pF	—	600	—	—	600	—	kΩ
Preamplifier Input Offset Voltage	V_{OS}	Note 1, $V_{pin\ 2}$-$V_{pin\ 3}$	—	1	15	—	1	15	mV
Preamplifier Output Impedance	Z_{OUT}		—	80	—	—	80	—	Ω
Preamplifier Output High Voltage	V_{OHA}	T_A = 25° C, $V_{pin\ 4}$, $V_{pin\ 2}$ = 2.5V, $V_{pin\ 3}$ = 2.7V	3.25	3.45	3.75	3.4	3.5	3.75	V
Preamplifier Output Low Voltage	V_{OHL}	T_A = 25° C, $V_{pin\ 4}$, $V_{pin\ 2}$ = 2.5V, $V_{pin\ 3}$ = 2.3V	1.25	1.4	1.55	1.2	1.4	1.5	V
Preamplifier Input Bias Current	I_B	$I_{pin\ 2}$ or $I_{pin\ 3}$, Note 1	—	1.0	4	—	1.0	4	μA
Preamplifier Input Offset Current	I_{OS}	$I_{pin\ 2}$-$I_{pin\ 3}$, Note 1	—	0.05	2	—	0.05	2	μA
OUTPUT DRIVE									
Output Voltage Swing	V_{OP}	$V_{pin\ 8\ High}$-$V_{pin\ 8\ Low}$, $V_{pin\ 9\ High}$-$V_{pin\ 9\ Low}$	—	6.0	—	—	6.0	—	V
Low Level Output Voltage	V_{OL}	T_A = 25° C, I_{LOAD} = 15mA, Note 2	0.65	0.8	0.95	0.65	0.8	0.95	V
Differential Output Voltage (Low Level)	V_{OLD}	T_A = 25° C, I_{LOAD} = 15mA, Note 2	—	0.02	0.15	—	0.02	0.15	V
High Level Output Leakage Current	I_{OH}	$V_{pin\ 14}$ = 4.9V, Note 1, $V_{pin\ 8}$ = $V_{pin\ 9}$ = 20V, T_A = 25° C	—	0.05	50	—	0.05	50	μA
Output Pulse Rise Time	T_{os}	AC Test Circuit	—	30	—	—	30	—	ns
Output Pulse Fall Time	T_{of}	AC Test Circuit	—	10	—	—	10	—	ns
Output Pulse Width	P_w	AC Test Circuit	—	324	—	—	324	—	ns
Pulse Width Differential	P_{wD}	AC Test Circuit	—	3	—	—	3	—	ns
Bipolar Violations at Maximum Density	BV_1 MAX	Repeater Test Circuit Line Atten. = 6-36dB	—	0	—	—	0	—	—
Bipolar Violations with Quasi-Random Input Pattern	BV_R MAX	Repeater Test Circuit Line Atten. = 6-36dB	—	0	—	—	0	—	—
CLOCK CIRCUIT									
Tank Emitter Follower Base Current	I_{TB}	$I_{pin\ 14}$, Note 1, $V_{pin\ 14}$ = 4.9V	—	4	15	—	4	15	μA
Tank Input Impedance	Z_{INT}	Measured from pin 14 to pin 15	—	300	—	—	300	—	kΩ
Oscillator Bias Current	I_{OSC}	Note 1, $V_{pin\ 14}$ = 3.9V (I_{OSC}-I_{TB})	10	30	50	10	30	50	μA
Oscillator Injection Current	I_{INJ}	Set $V_{pin\ 4}$-$V_{pin\ 5}$ = ±1.4V, $V_{pin\ 14}$ = 3.9V (I_{INJ}-I_{OSC})	75	120	160	75	120	160	μA
Delay Circuit Resistor	R_d	Measured from pin 11 or pin 12 to pin 15, T_A = 25° C	3.2	4.0	4.8	3.2	4.0	4.8	kΩ

NOTES:

1. $V_{pin\ 2}$ = 2.5V, adjust $V_{pin\ 3}$ until $V_{pin\ 4} = V_{pin\ 5}$.
2. A dynamic test, pin 2 = 2.5V, pin 3 pulsed at 100Hz rate, pin 14 pulsed at 200Hz rate.

ELECTRICAL CHARACTERISTICS at $V_{CC1} = 4.4V$, $V_{CC2} = 6.8V$, $-40°C \leq T_A \leq +85°C$, unless otherwise noted. $V_{pin\ 6} = V_{pin\ 7} = V_{pin\ 13} = GND$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	RPT-81 MIN	RPT-81 TYP	RPT-81 MAX	RPT-82 MIN	RPT-82 TYP	RPT-82 MAX	UNITS
MISCELLANEOUS									
ALBO Threshold	V_{TA}	Differential voltage, measured between pins 4 and 5, required to trip Peak Detector. $T_A = 25°C$	1.35	1.5	1.65	1.35	1.5	1.65	V
Clock Threshold	V_{TC}	Differential voltage, measured between pins 4 and 5, required to drive Fullwave Rectifier. $T_A = 25°C$	0.85	1.0	1.2	0.9	1.08	1.25	V
Logic Threshold	V_{TL}	Differential voltage, measured between pins 4 and 5, required to trip Logic Threshold. $T_A = 25°C$	0.65	0.75	0.85	0.65	0.75	0.85	V
Clock Threshold as % of ALBO Voltage	V_{TC}	$T_A = 25°C$	62	66	70	68	72	76	%
Logic Threshold as % of ALBO Voltage	V_{TL}	$T_A = 25°C$	47	50	53	46	49	52	%
ALBO ON Voltage	V_{D16}	Measured at pin 16, $\lvert V_{p4}\text{-}V_{p5}\rvert$ = ALBO Threshold	1.0	1.7	2.5	1.0	1.7	2.5	V
ALBO OFF Voltage	V_{F16}	Measured at pin 16 and pin 1 Note 1. $T_A = 25°C$	—	—	75	—	—	75	mV
Minimum ALBO Diode Resistance	R_D Min		—	8	—	—	8	—	Ω
Maximum ALBO Diode Resistance	R_D Max		—	30	—	—	30	—	kΩ

NOTE:

1. $V_{pin\ 2} = 2.5V$, adjust $V_{pin\ 3}$ until $V_{pin\ 4} = V_{pin\ 5}$.

REPEATER DEFINITIONS

ALBO THRESHOLD

The differential voltage measured between pins 4 and 5, required to activate the internal peak detector.

AUTOMATIC LINE BUILD OUT

An automatic gain control circuit which operates by simulating a line "build-out" or extension.

BIPOLAR VIOLATION

The transmission of two consecutive pulses of the same polarity.

CLOCK THRESHOLD

The differential voltage measured between pins 4 and 5, required to drive the internal fullwave rectifier.

DATA THRESHOLD

The differential voltage measured between pins 4 and 5, required to trip logic threshold detector.

DIFFERENTIAL OUTPUT VOLTAGE

The difference in voltage of the two outputs with a binary one output of either polarity.

ALBO DIODE RESISTANCE

Small signal resistance of ALBO diode measured between pins 1 and 6. The ALBO diode is a diode connected transistor whose current-resistance relationship is $R_D = 26/I_O$ where R_D = ALBO diode resistance and I_O = ALBO diode current in mA.

DELAY CIRCUIT RESISTANCE

Resistance seen at pins 11 and 12.

LINE BUILD OUT

The attenuation added to the output of a short line.

MAXIMUM DENSITY

An input signal pattern consisting of all ones.

MINIMUM DENSITY

An input signal pattern consisting of two ones followed by 14 zeros.

OUTPUT PULSE RISE (FALL) TIME

Rise (Fall) time of regenerated pulse. Measured from the 10-90% points.

OUTPUT PULSE WIDTH DIFFERENTIAL

In a T1 carrier system a typical pulse width is 324nsec. The pulse width differential is the difference in pulse width of the two outputs.

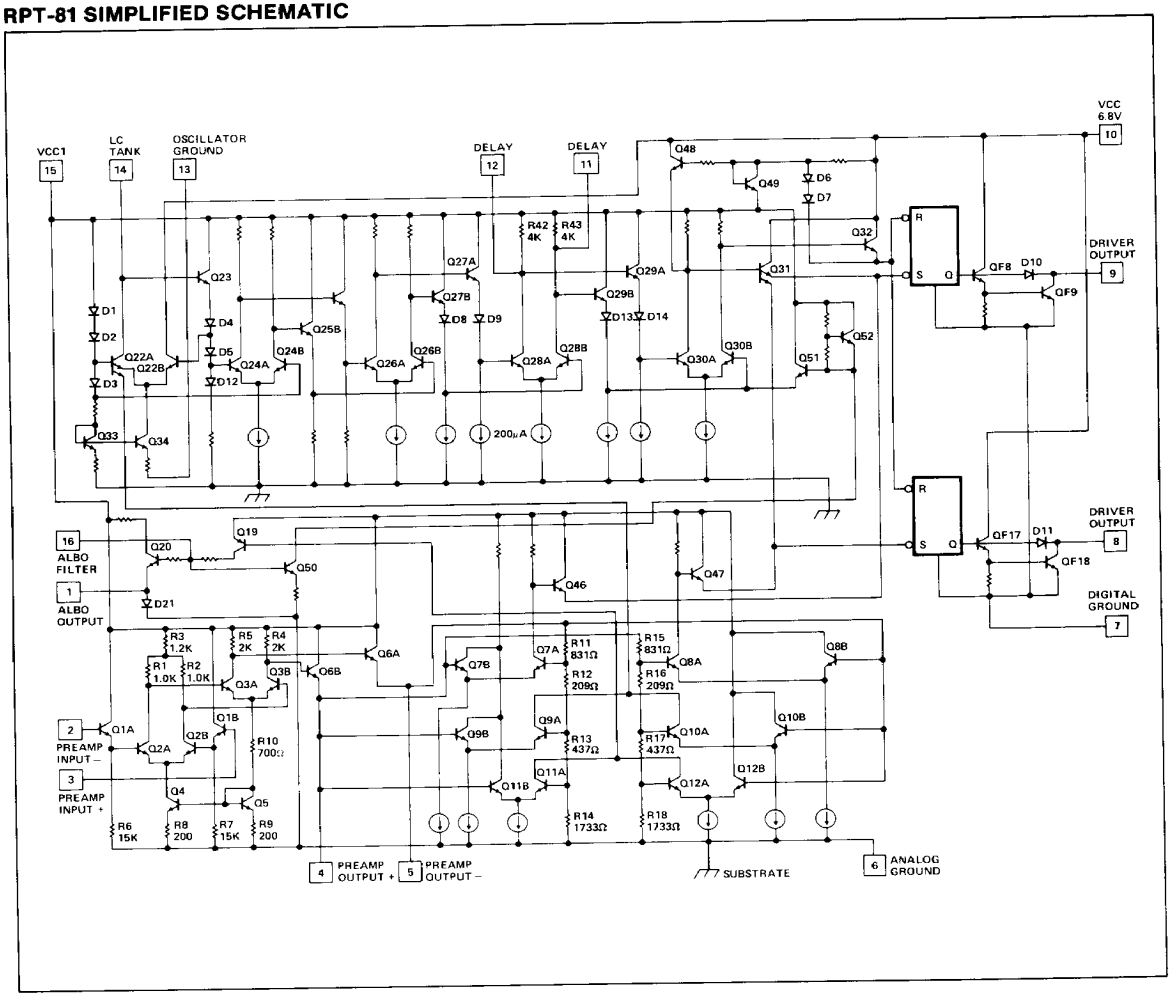
PREAMPLIFIER BANDWIDTH

3dB bandwidth of preamplifier circuit.

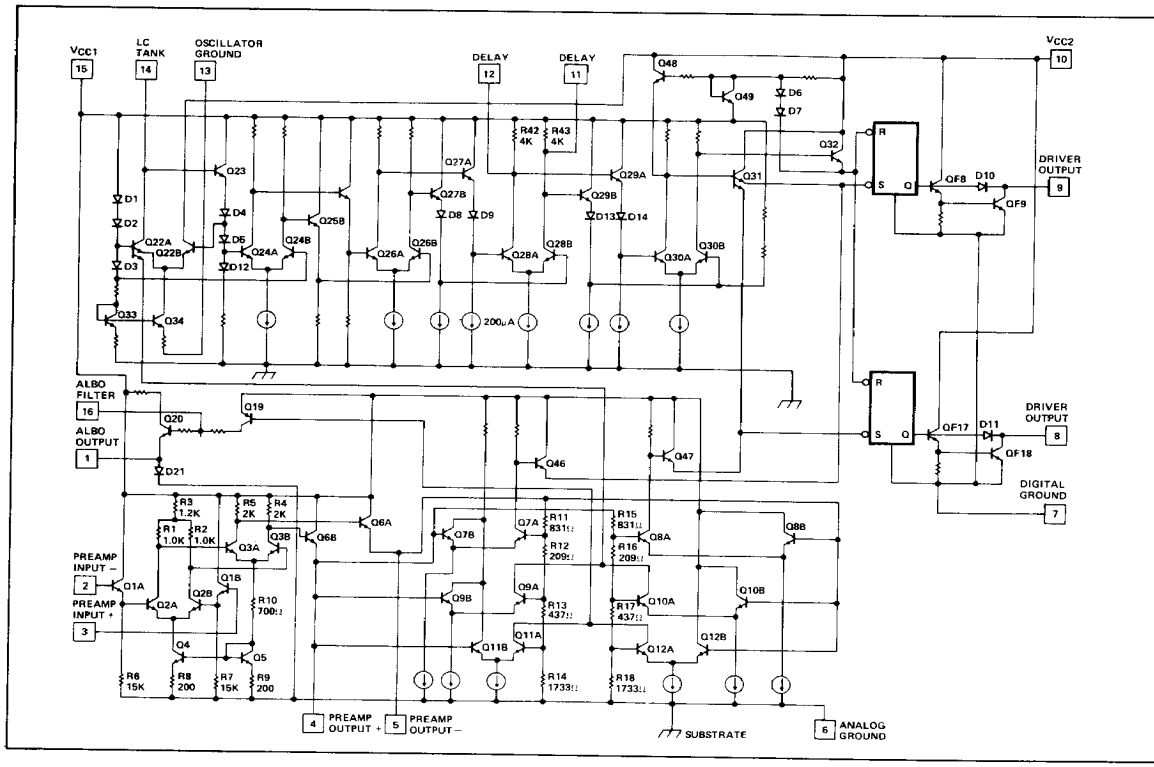
EQUALIZING NETWORK

A network which compensates for the amplitude and phase response of the cable over the operating bandwidth.

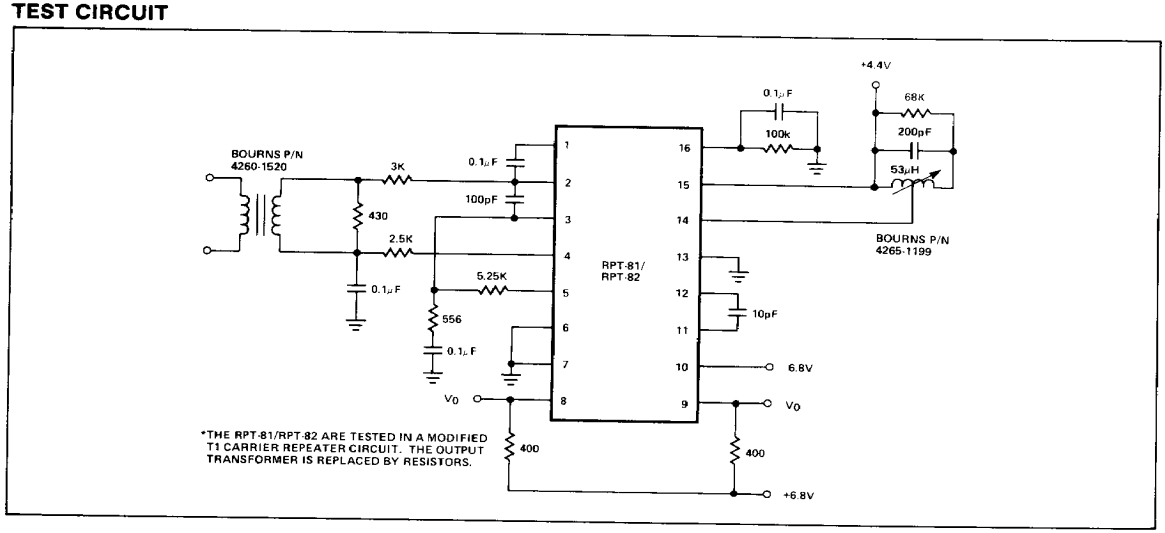
RPT-81 SIMPLIFIED SCHEMATIC



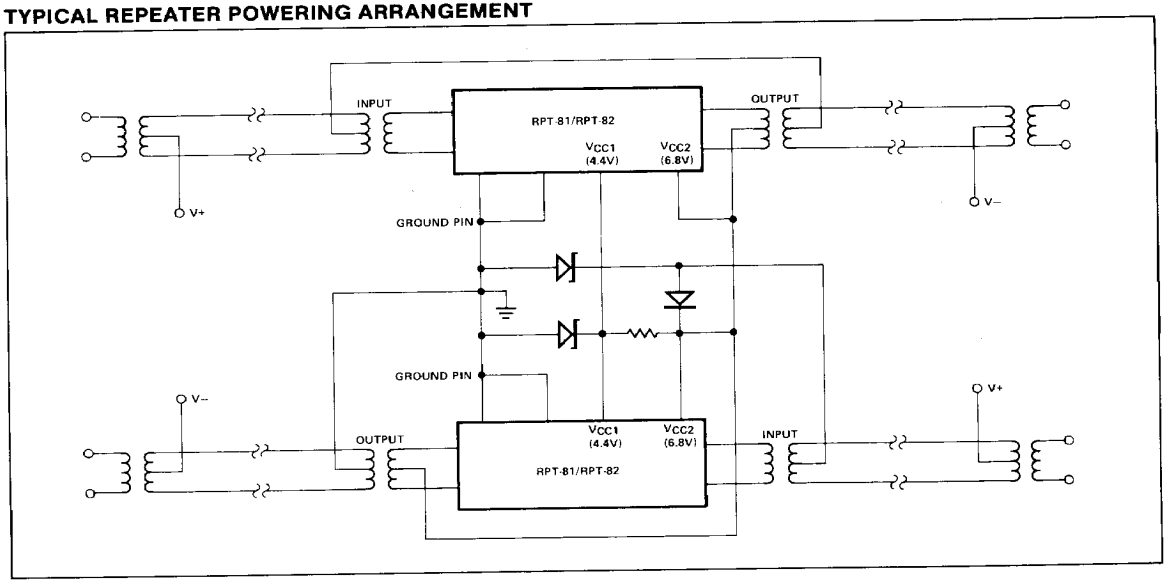
RPT-82 SIMPLIFIED SCHEMATIC



TEST CIRCUIT



TYPICAL REPEATER POWERING ARRANGEMENT



REPEATER CURRENT REQUIREMENTS

For comparison to CCIT or ATT specifications it is convenient to estimate total repeater current requirements. Repeater current is typically calculated in the following manner:

i. Each of the two zeners used as regulators have idle current requirements of approximately 1.0mA (2mA).

ii. Total no-signal supply current, from the electrical characteristics table, is 13.0mA (guaranteed maximum) for each side.

iii. To compute worst case (all ones) output current assumes a 6.0 volt pulse across a 400Ω transformer primary (50% d.f.) for the U.S. or a 6.0 volt pulse across a 480Ω transformer primary (50% d.f.) for CCITT. These currents compute to 15mA and 12.5mA respectively (for both sides).

iv. ALBO diode current is 26mA divided by the minimum required ALBO resistance (approximately 8Ω), which is 6.5mA for both sides.

Adding the currents in ii, iii, and iv gives the following typical repeater current requirements:

i. U.S. ..... 49.5mA (worst case all ones output)
ii. Europe ..... 47.0mA (worst case all ones output)

APPLICATIONS INFORMATION

In a typical repeater system extensive external circuitry is required. The regulator network assembled from zener diodes and resistors is used to power the integrated circuit. Normally one common circuit is provided for the two ICs operating in opposite directions. Input and output transformers are used to couple the transmission lines. The input one-to-one transformer secondary is loaded with a line matching resistor to avoid reflections on the input lines. An attenuator network may be installed after this input transformer as a fixed line-build-out pad. Feedback resistors are used to set the DC bias of the circuit. Additionally the bias network is connected to a fixed resistive voltage divider to tie the biasing network to a fixed potential. The ALBO network consists of a series impedance and a shunt impedance where the shunt impedance is AC terminated to the ALBO diode.

The shunt impedance should have both resistive and reactive components to assist in line equalization. The equalizing network is basically a series-tuned circuit in one of the input legs of the preamplifier whose function is to give the preamplifier a frequency response which corrects for the amplitude and phase response of the input line. The design of the equalizing network is very important to the system performance. A lag capacitor across the preamplifier input stabilizes the preamplifier. The output transformer normally incorporates a fault locating winding which is used, in conjunction with appropriate filters, to detect defective repeaters. The input transformer has a center-tapped primary to allow for a simplex powering system.

The RPT-81/RPT-82 oscillator allows two modes of operation controllable by pin 13 (Oscillator Control). When grounded, the oscillator is in a free-running mode. With pin 13 open, the oscillator works in a pulsed, ringing mode. In both cases the external L-C tank circuit determines the oscillation frequency.

The external delay capacitor (across pins 11 and 12) provides 90° of phase shift through the clock amplifier.

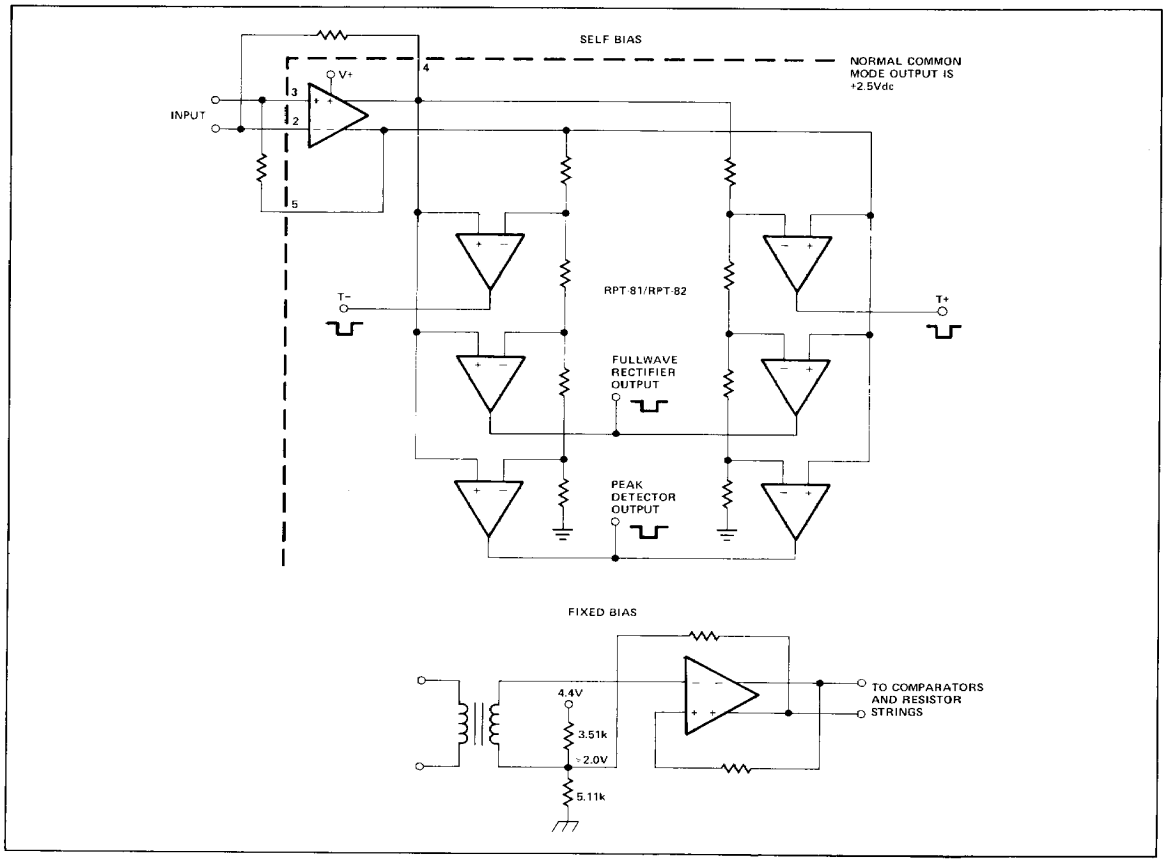
Oscillator-tank-circuit Q directly affects the clock regeneration circuitry. The effective Q of the L-C oscillator tank circuit must be high enough that ringing will be maintained with minimum pulse densities. The resonant Q cannot, however, be arbitrarily large, or operating temperature changes and component aging will cause resonant frequency shifts. The RPT-81/RPT-82 will operate with Q's as low as 75.

In order to provide noise rejection, the analog and digital grounds have been isolated. Low noise/distortion operation can be enhanced if the high-power output leads and external circuitry are physically located as far as possible from the preamplifier inputs. Supply bypassing of V_{CC1} and V_{CC2} close to device pins is recommended.

PREAMPLIFIER BIASING SCHEMES

Both inverting and noninverting outputs of the RPT-81/RPT-82 preamplifier are available so that either self-biasing or fixed-biasing techniques may be employed. The effect of the DC biasing is to set the thresholds of the detectors. All the thresholds move together, the relative threshold which is defined in terms of a percentage of the peak detector threshold is determined by the resistor string. In a self-biased scheme, the noninverting output is returned to the inverting input and the inverting output is returned to the noninverting input. In this manner the input leads are biased to the normally-occurring common-mode output voltage. The best noise performance is obtained with this system, but some problems are encountered at low temperatures where the circuit tends to turn itself off. In a fixed biased scheme, one of the inputs is biased to a fixed DC level while the other input is biased to the opposite output in the same manner as with self bias. Note that with fixed bias a differential output offset will be caused if the fixed bias is not matched to the normally-occuring output level. If the fixed level is very close to the normally-occuring output level, then there is an improvement in performance at low temperature.

PREAMPLIFIER BIASING SCHEMES



RPT-81/RPT-82 IN TYPICAL 1.544MHz T1 REPEATER SYSTEM