

HB56D236B/SB Series

T-46-23-18

2,097,152-Word x 36-Bit High Density Dynamic RAM Module

DESCRIPTION

The HB56D236B/SB/BS/SBS is a 2M x 36 dynamic RAM module, mounted 16 pieces of 4 Mbit DRAM (HM514400JP/AJ) sealed in SOJ package and 8 pieces of 1 Mbit DRAM (HM511000JP) sealed in SOJ package (HB56D236B/SB or 8 pieces of 1 Mbit DRAM (HM511000ATS) sealed in TSOP package (HB56D236SB/SBS). An outline of the HB56D236B/SB/BS/SBS is 72-pin single in-line package. Therefore, the HB56D236B/SB/BS/SBS makes high density mounting possible without surface mount technology. The HB56D236B/SB/BS/SBS provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ or beside each TSOP but only on the one side of its module board.

FEATURES

- 72-pin Single In-line Package
Lead Pitch 1.27 mm
- Single 5V ($\pm 5\%$) Supply
- High Speed
Access Time 60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
Active Mode 6.825W/6.195W/5.565W/4.935W (max)
Standby Mode 252 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycle (16 ms)
- 2 Variations of Refresh
RAS Only Refresh
CAS Before RAS Refresh
- TTL Compatible

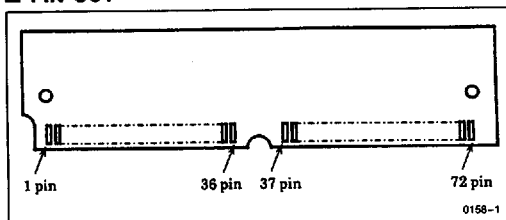
ORDERING INFORMATION

Part No.	Access Time	Package	Contact Pad
HB56D236B/BS-6A	60 ns	72-pin SIP Socket Type	Gold
HB56D236B/BS-7A	70 ns		
HB56D236B/BS-8A	80 ns		
HB56D236B/BS-10A	100 ns		
HB56D236B-8	80 ns		
HB56D236B-10	100 ns	72-pin SIP Socket Type	Solder
HB56D236SB/SBS-6A	60 ns		
HB56D236SB/SBS-7A	70 ns		
HB56D236SB/SBS-8A	80 ns		
HB56D236SB/SBS-10A	100 ns		
HB56D236SB-8	80 ns		
HB56D236SB-10	100 ns		

PRESENCE DETECT PINOUT

Pin No.	Pin Name	HB56D236B/SB/BS/SBS					
		-6A	-7A	-8A	-10A	-8	-10
67	PD1	NC	NC	NC	NC	NC	NC
68	PD2	NC	NC	NC	NC	NC	NC
69	PD3	NC	V _{SS}	NC	V _{SS}	NC	V _{SS}
70	PD4	NC	NC	V _{SS}	V _{SS}	V _{SS}	V _{SS}

PIN OUT



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	19	NC	37	DQ ₁₇	55	DQ ₁₂
2	DQ ₀	20	DQ ₄	38	DQ ₃₅	56	DQ ₃₀
3	DQ ₁₈	21	DQ ₂₂	39	V _{SS}	57	DQ ₁₃
4	DQ ₁	22	DQ ₅	40	CAS ₀	58	DQ ₃₁
5	DQ ₁₉	23	DQ ₂₃	41	CAS ₂	59	V _{CC}
6	DQ ₂	24	DQ ₆	42	CAS ₃	60	DQ ₃₂
7	DQ ₂₀	25	DQ ₂₄	43	CAS ₁	61	DQ ₁₄
8	DQ ₃	26	DQ ₇	44	RAS ₀	62	DQ ₃₃
9	DQ ₂₁	27	DQ ₂₅	45	RAS ₁	63	DQ ₁₅
10	V _{CC}	28	A ₇	46	NC	64	DQ ₃₄
11	NC	29	NC	47	WE	65	DQ ₁₆
12	A ₀	30	V _{CC}	48	NC	66	NC
13	A ₁	31	A ₈	49	DQ ₉	67	PD1
14	A ₂	32	A ₉	50	DQ ₂₇	68	PD2
15	A ₃	33	RAS ₃	51	DQ ₁₀	69	PD3
16	A ₄	34	RAS ₂	52	DQ ₂₈	70	PD4
17	A ₅	35	DQ ₂₆	53	DQ ₁₁	71	NC
18	A ₆	36	DQ ₈	54	DQ ₂₉	72	V _{SS}

PIN DESCRIPTION

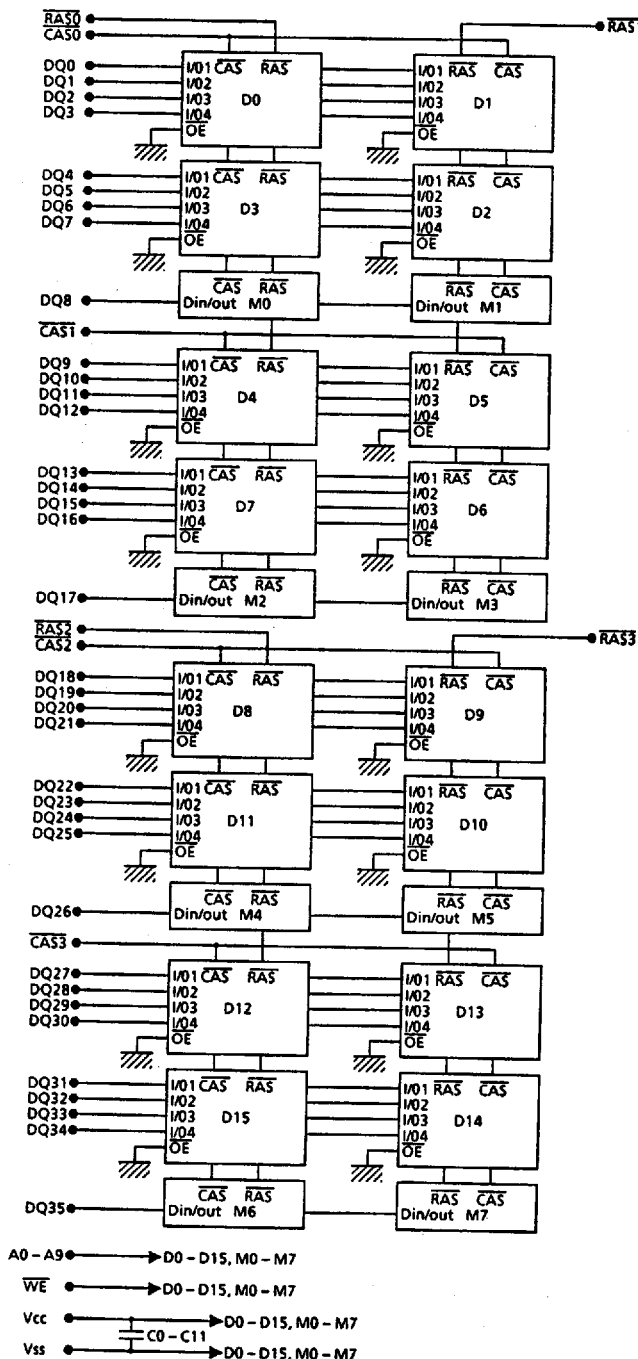
Pin Name	Function
A ₀ -A ₉	Address Input
A ₀ -A ₉	Refresh Address Input
DQ ₀ -DQ ₃₅	Data-in/Data-out
CAS ₀ -CAS ₃	Column Address Strobe
RAS ₀ -RAS ₃	Row Address Strobe
WE	Read/Write Enable
V _{CC}	Power Supply (+ 5V)
V _{SS}	Ground
PD ₁ -PD ₄	Presence Detect Pin
NC	No Connection



BLOCK DIAGRAM

HITACHI/ LOGIC/ARRAYS/MEM

T-46-23-18



*D0-D15: HM514400JP/AJ
M0-M7: HM511000JP/ATS

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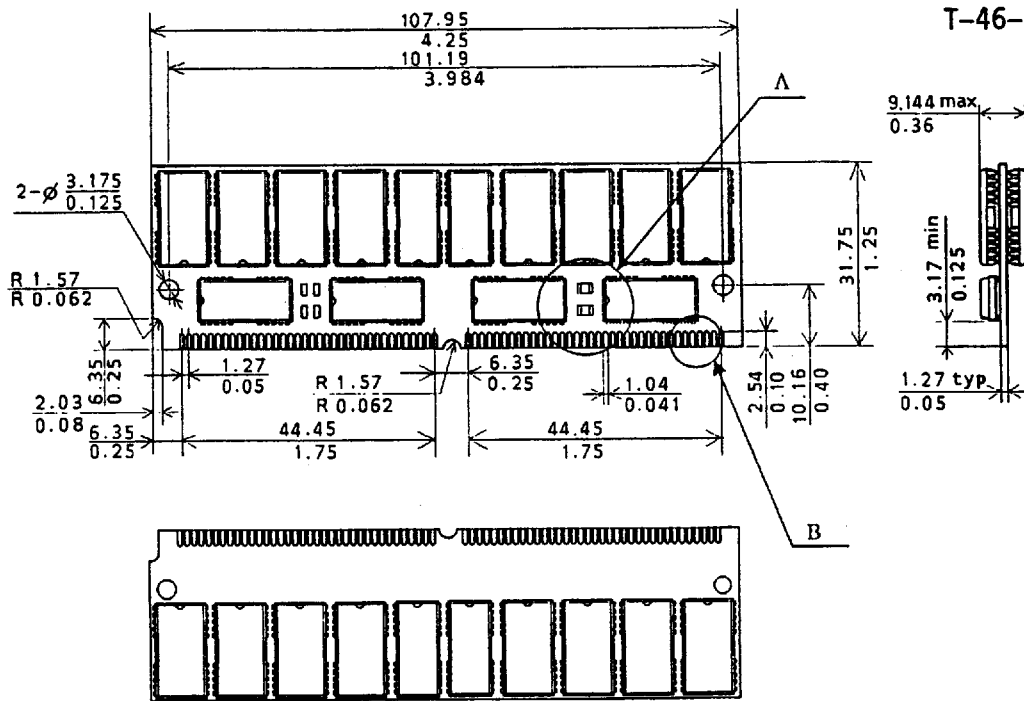
■ PHYSICAL OUTLINE

HITACHI/ LOGIC/ARRAYS/MEM

Unit: $\frac{\text{mm}}{\text{inch}}$

• HB56D236B/SB

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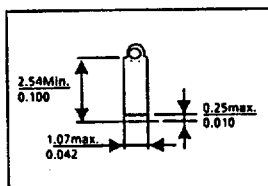


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Detail A

60ns	70ns	80ns	100ns

Detail B



Note: Following the specification of the contact pads.

Part No.	Contact Pad
HB56D236B-XX	Gold
HB56D236SB-XX	Solder

0158-4



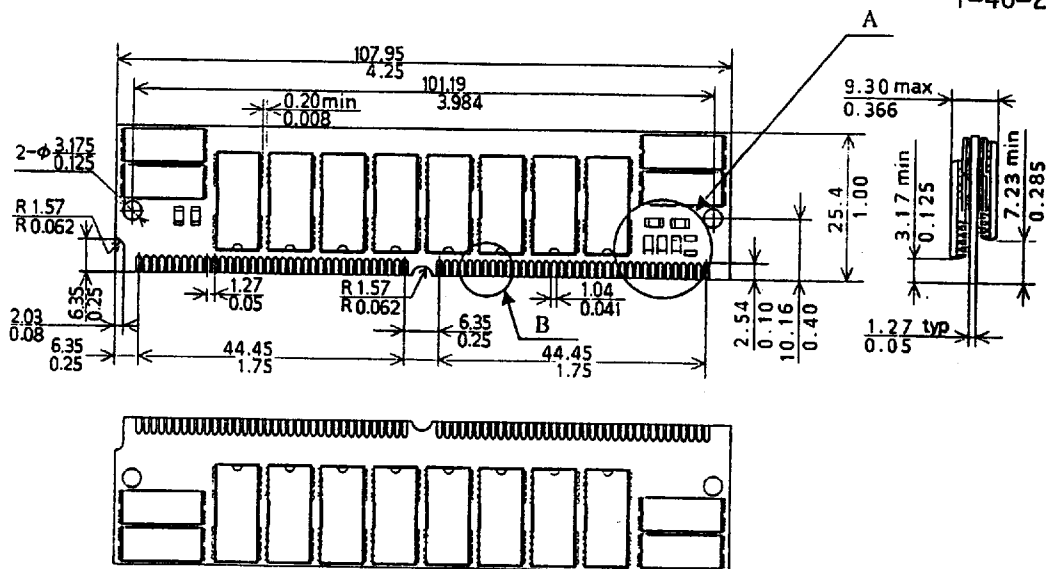
■ PHYSICAL OUTLINE (continued)

HITACHI/ LOGIC/ARRAYS/MEM

Unit: $\frac{\text{mm}}{\text{inch}}$

• HB56D236BS/SBS

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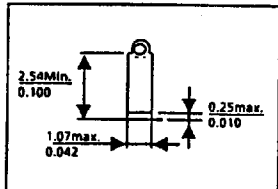


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Detail A

60ns	70ns	80ns	100ns

Detail B



Note: Following the specification of the contact pads.

Part No.	Contact Pad
HB56D236BS-XX	Gold
HB56D236BS-XX	Solder

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■ ABSOLUTE MAXIMUM RATINGS

HITACHI/ LOGIC/ARRAYS/MEM

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Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input) V_{in}	-1.0 to +7.0	V
	(Output) V_{out}	-1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	8	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions ($T_A = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	-1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS} .• DC Electrical Characteristics ($T_A = 0$ to +70°C, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$)

DC Electrical Characteristics (T _A = 0 to +75°C, V _{CC} = 0 to 5.5V, V _{SS} = 0V)																
Parameter	Symbol	HB56D236B/SB/BS/SBS												Unit	Test Conditions	Note
		-6A		-7A		-8A		-10A		-8		-10				
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I _{CC1}	—	1300	—	1180	—	1060	—	940	—	1060	—	940	mA	t _{RC} = Min	1, 2
Standby Current	I _{CC2}	—	48	—	48	—	48	—	48	—	48	—	48	mA	TTL Interface R _{AS} , C _{AS} = V _{IH} D _{out} = High-Z	
		—	24	—	24	—	24	—	24	—	24	—	24	mA	CMOS Interface R _{AS} , C _{AS} ≥ V _{CC} - 0.2V D _{out} = High-Z	
R _{AS} Only Refresh Current	I _{CC3}	—	1300	—	1180	—	1020	—	900	—	1020	—	900	mA	t _{RC} = Min	2
Standby Current	I _{CC5}	—	120	—	120	—	120	—	120	—	120	—	120	mA	R _{AS} = V _{IH} C _{AS} = V _{IL} D _{out} = Enable	1
C _{AS} Before R _{AS} Refresh Current	I _{CC6}	—	1260	—	1140	—	1020	—	900	—	1020	—	900	mA	t _{RC} = Min	
Page Mode Current	I _{CC7}	—	1260	—	1140	—	980	—	900	—	980	—	900	mA	t _{PC} = Min	1, 3
Input Leakage Current	I _{LI}	-10	10	-10	10	-10	10	-10	10	-10	10	-10	10	μA	0V ≤ V _{in} ≤ 7V	
Output Leakage Current	I _{LO}	-10	10	-10	10	-10	10	-10	10	-10	10	-10	10	μA	0V ≤ V _{in} ≤ 7V D _{out} = Disable	
Output High Voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High I _{out} = -5 mA	
Output Low Voltage	V _{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I _{out} = 4.2 mA	

- Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
 2. Address can be changed less than three times while $\overline{RAS} = V_{IL}$.
 3. Address can be changed ≤ 1 time while $\overline{CAS} = V_{IH}$.



• Capacitance ($T_A = 25^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$)

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Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	161	pF	1
Input Capacitance ($\overline{\text{WE}}$)	C_{I2}	—	193	pF	1
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$)	C_{I3}	—	62	pF	1
Output Capacitance ($\text{DQ0-7, 9-16, 18-25, 27-34}$)	$C_{I/O1}$	—	29	pF	1, 2
Output Capacitance (DQ8, 17, 26, 35)	$C_{I/O2}$	—	39	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. $\overline{\text{CAS}} = V_{IH}$ to disable D_{out} .

• AC Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$) 1, 12

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56D236B/SB/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t _{RC}	120	—	130	—	160	—	190	—	160	—	190	—	ns	
RAS Precharge Time	t _{RP}	50	—	50	—	70	—	80	—	70	—	80	—	ns	
RAS Pulse Width	t _{RAS}	60	10000	70	10000	80	10000	100	10000	80	10000	100	10000	ns	
CAS Pulse Width	t _{CAS}	20	10000	20	10000	25	10000	25	10000	25	10000	25	10000	ns	
Row Address Setup Time	t _{ASR}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	12	—	15	—	12	—	15	—	ns	
Column Address Setup Time	t _{ASC}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	15	—	15	—	20	—	20	—	20	—	20	—	ns	
RAS to CAS Delay Time	t _{RCD}	20	40	20	50	22	55	25	75	22	55	25	75	ns	8
RAS to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	20	55	17	40	20	55	ns	9
RAS Hold Time	t _{RSH}	20	—	20	—	25	—	25	—	25	—	25	—	ns	
CAS Hold Time	t _{CSH}	60	—	70	—	80	—	100	—	80	—	100	—	ns	
CAS to RAS Precharge Time	t _{CRP}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t _{REF}	—	16	—	16	—	16	—	16	—	16	—	16	ms	15

Read Cycle

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Parameter	Symbol	HB56D236B/SB/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	—	80	—	100	—	80	—	100	ns	2, 3
Access Time from $\overline{\text{CAS}}$	t_{CAC}	—	20	—	20	—	25	—	25	—	25	—	25	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	40	—	45	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{\text{RAS}}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{RAL}	30	—	35	—	40	—	55	—	40	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	—	20	—	20	—	20	—	25	—	20	—	25	ns	6



Write Cycle

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Parameter	Symbol	HB56D236B/SB/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t _{WCS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t _{WCH}	15	—	15	—	20	—	20	—	20	—	20	—	ns	
Write Command Pulse Width	t _{WP}	10	—	10	—	15	—	20	—	15	—	20	—	ns	
Data-in Setup Time	t _{DS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t _{DD}	15	—	15	—	20	—	20	—	20	—	20	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56D236B/SB/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CAS Setup Time (CAS Before RAS Refresh Cycle)	t _{CSR}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
CAS Hold Time (CAS Before RAS Refresh Cycle)	t _{CHR}	15	—	15	—	20	—	20	—	20	—	20	—	ns	
RAS Precharge to CAS Hold Time	t _{RPC}	10	—	10	—	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HB56D236B/SB/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t _{PC}	45	—	50	—	55	—	55	—	55	—	55	—	ns	
Fast Page Mode CAS Precharge Time	t _{CP}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Fast Page Mode RAS Pulse Width	t _{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	—	100000	ns	13
Access Time from CAS Precharge	t _{ACP}	—	40	—	45	—	50	—	50	—	50	—	50	ns	14
RAS Hold Time from CAS Precharge	t _{RHCP}	40	—	45	—	50	—	50	—	50	—	50	—	ns	

Notes: 1. AC measurements assume t_T = 5 ns.2. Assumes that t_{RCD} ≤ t_{RCD} (max) and t_{RAD} ≤ t_{RAD} (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.

3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.

4. Assumes that t_{RCD} ≥ t_{RCD} (max), t_{RAD} ≤ t_{RAD} (max).5. Assumes that t_{RCD} ≤ t_{RCD} (max), t_{RAD} ≥ t_{RAD} (max).6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.10. Early write cycle only (t_{WCS} ≥ t_{WCS} (min)).

11. These parameters are referenced to CAS leading edge in an early write cycle.

12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS clock such as RAS only refresh).

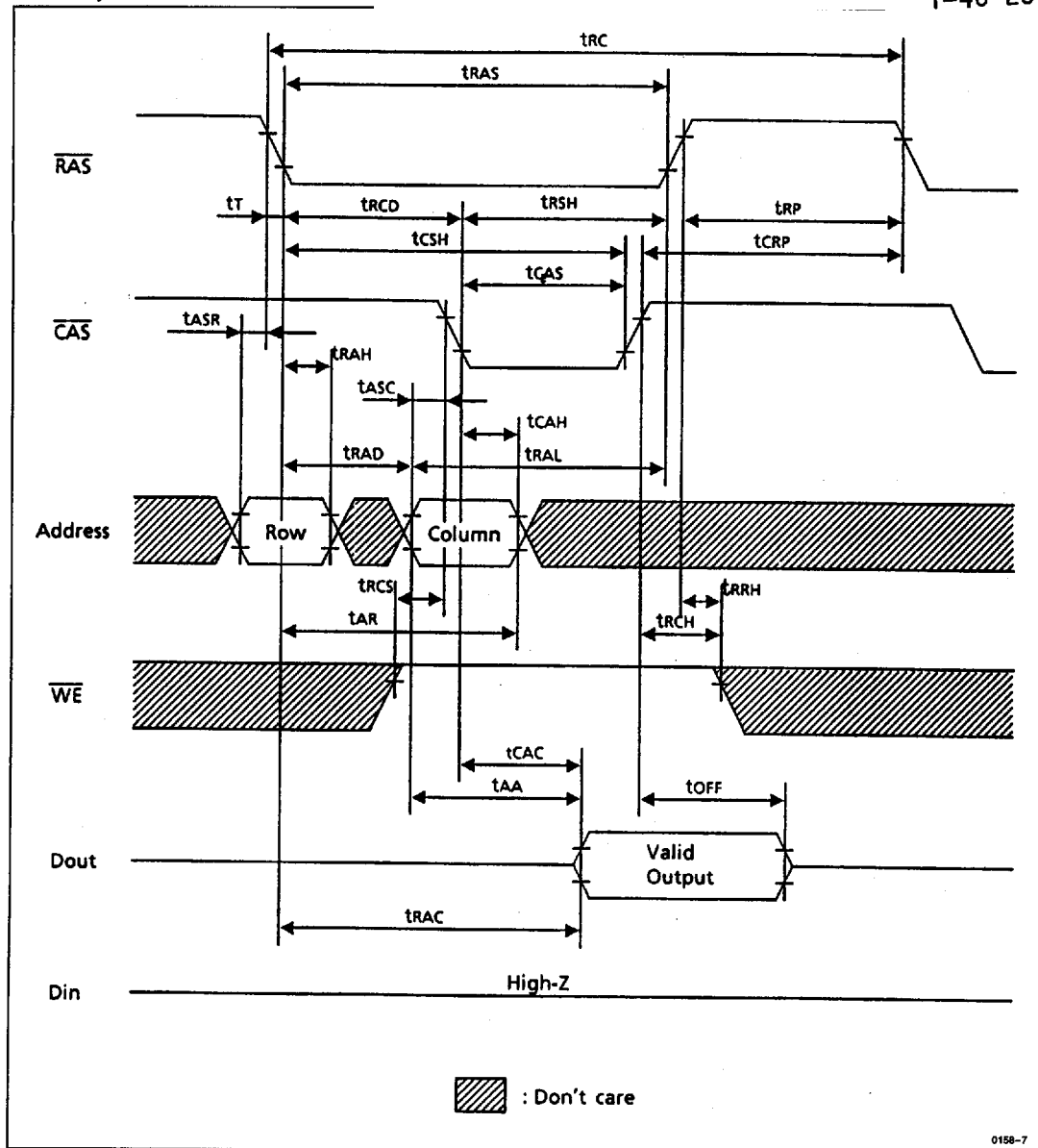
13. t_{RASC} is determined by RAS pulse width in fast page mode cycles.14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.15. t_{REF} is determined by 1,024 refresh cycles.

TIMING WAVEFORMS

• Read Cycle

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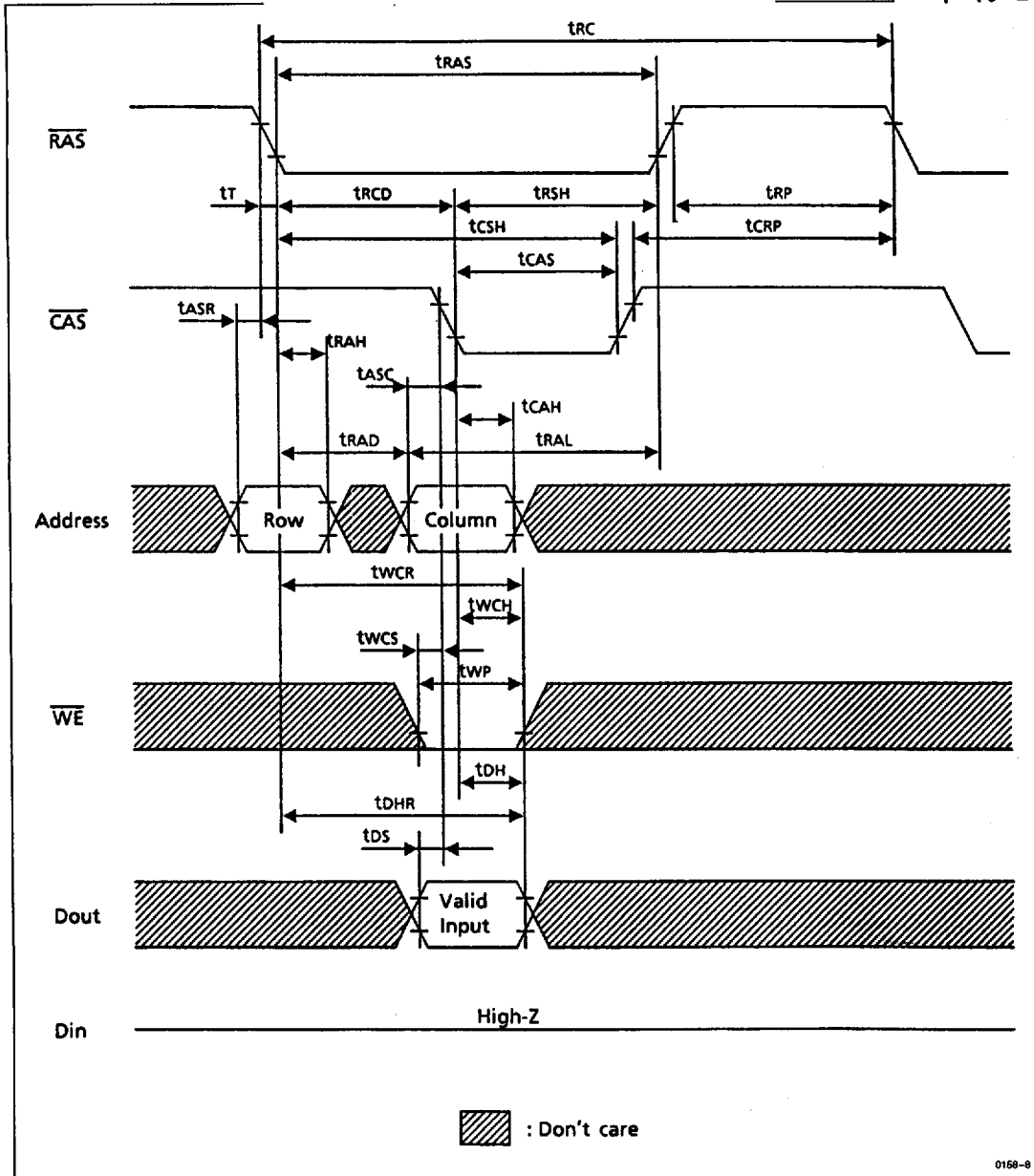
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• Early Write Cycle

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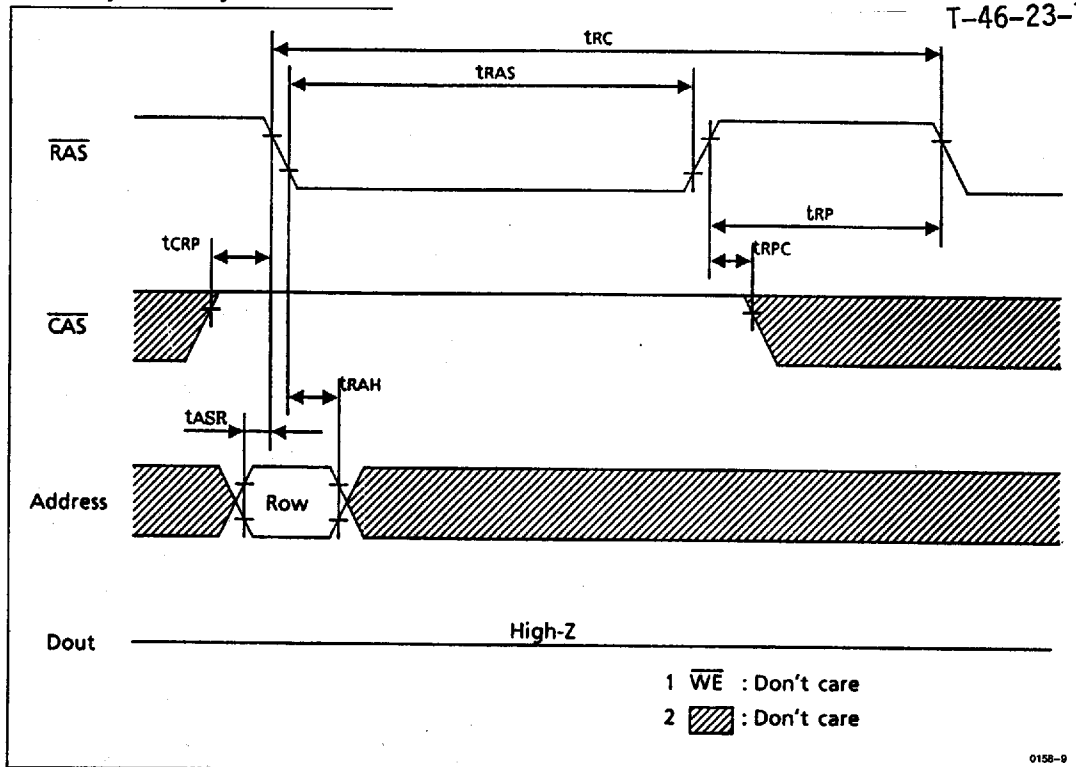
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• RAS Only Refresh Cycle

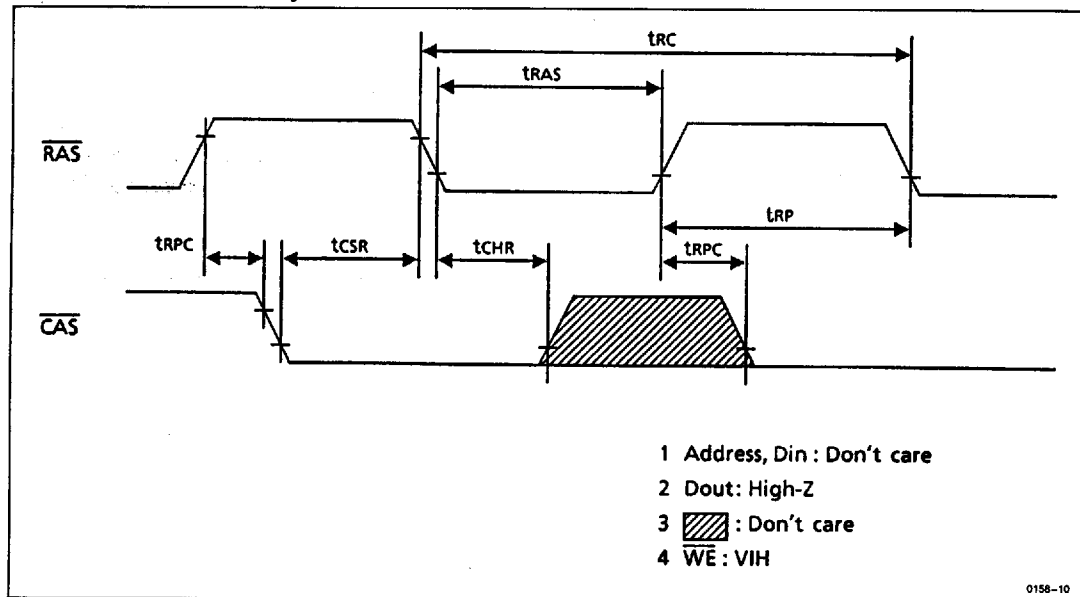
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• CAS Before RAS Refresh Cycle

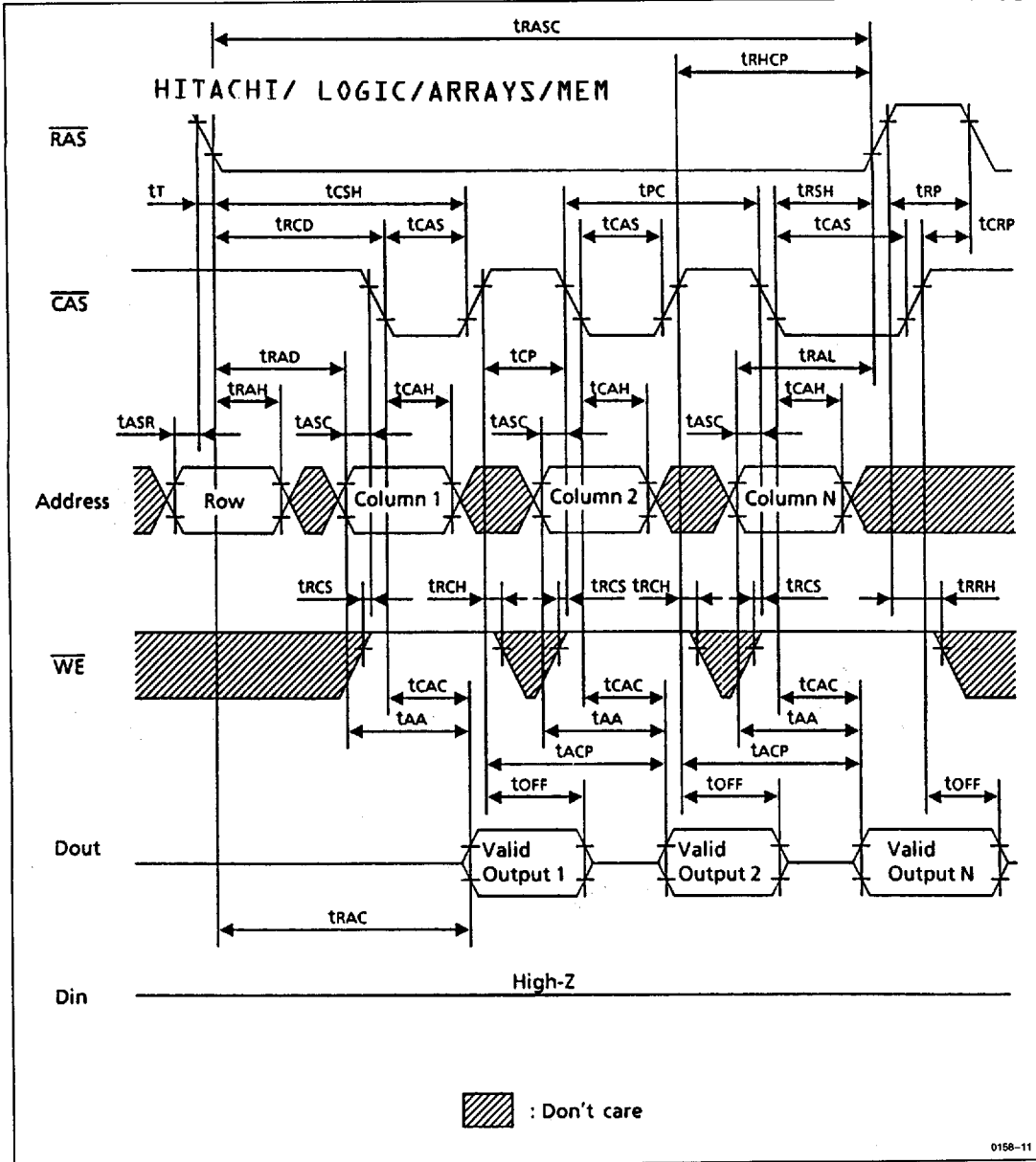


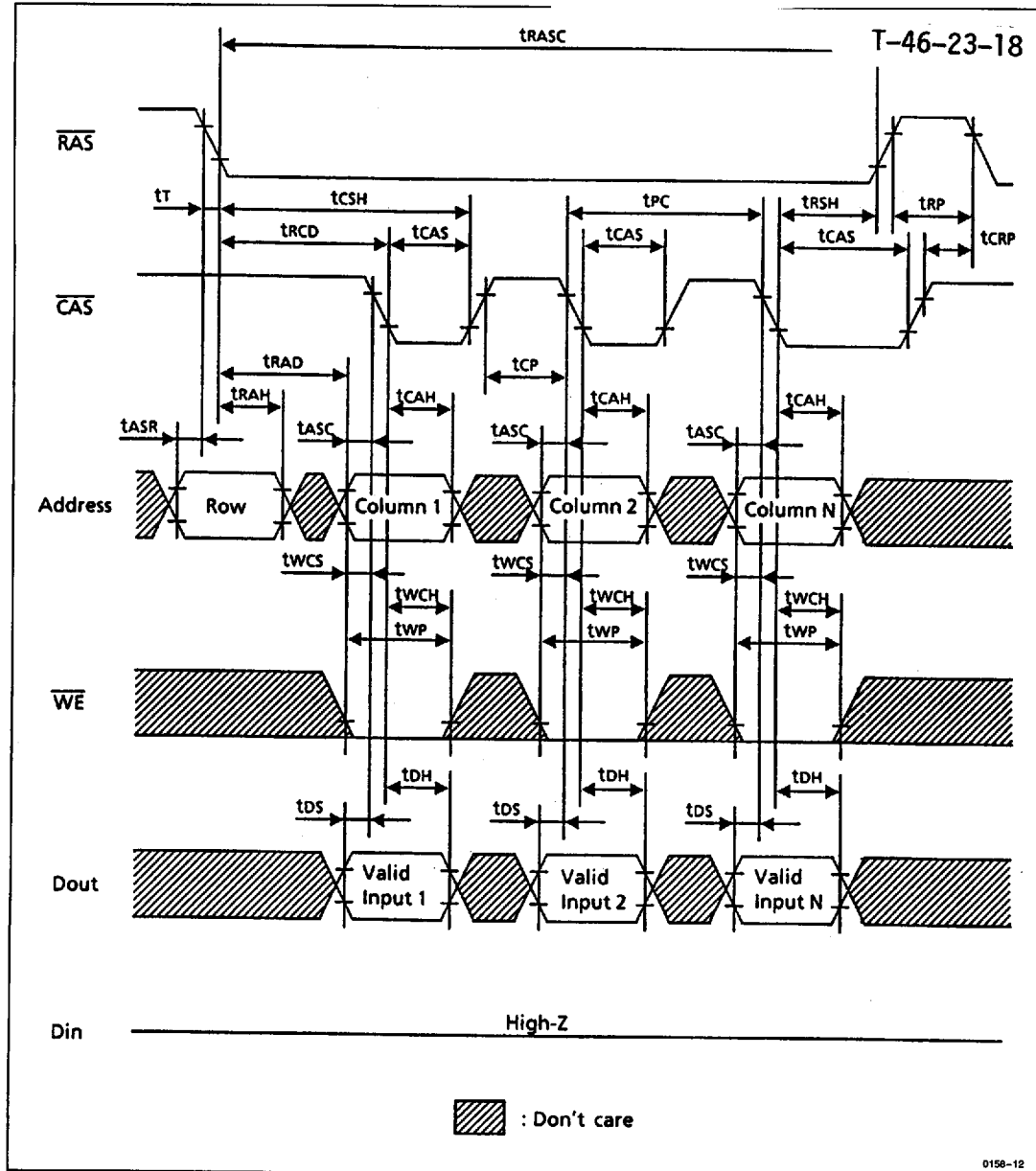
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• Fast Page Mode Read Cycle

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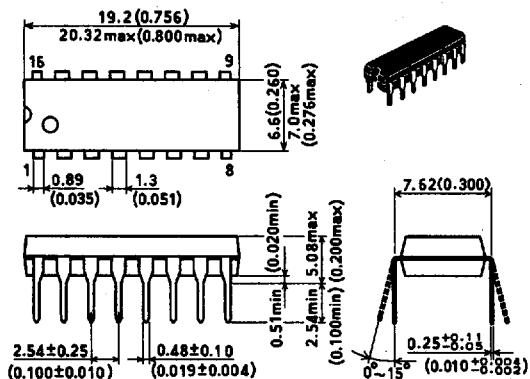


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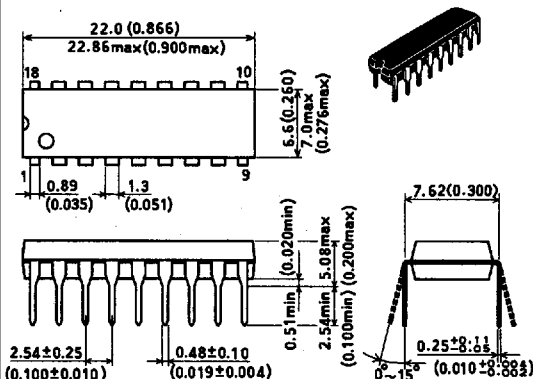
Unit: mm (inch) Scale 3/2

• Dual-in-line Plastic

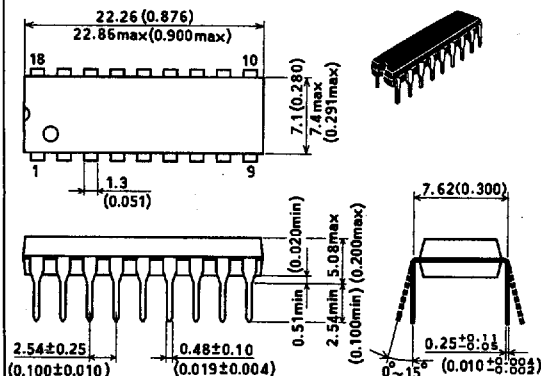
• DP-16B



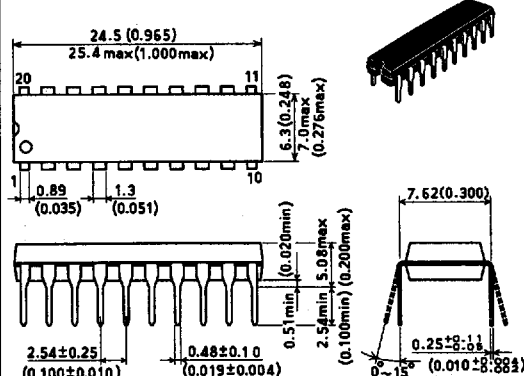
• DP-18B



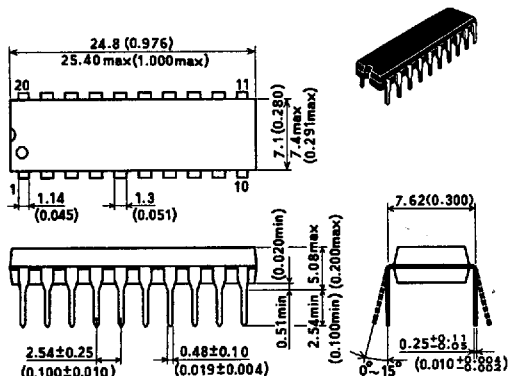
• DP-18C



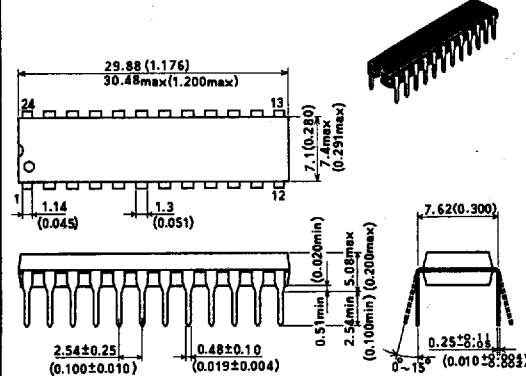
• DP-20N



• DP-20NA



• DP-20NC

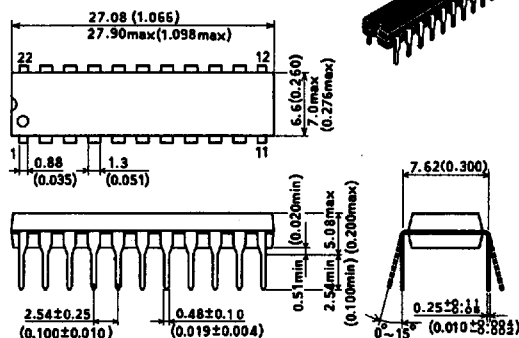


• Dual-in-line Plastic

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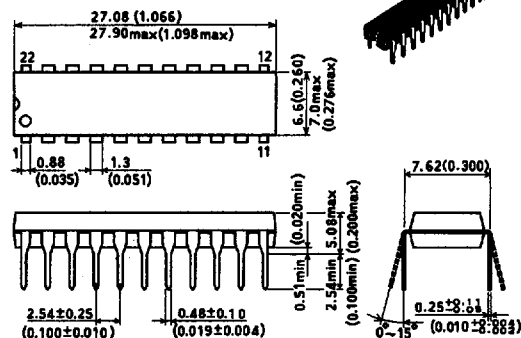
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• DP-22N

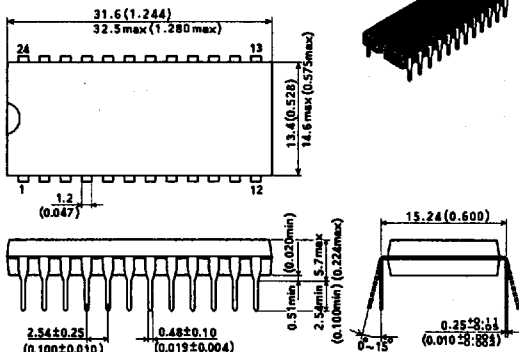


• DP-22NB

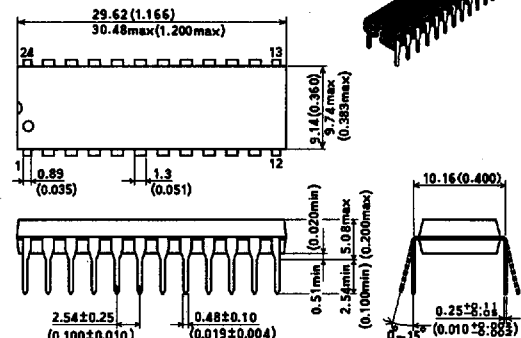
T-90-20



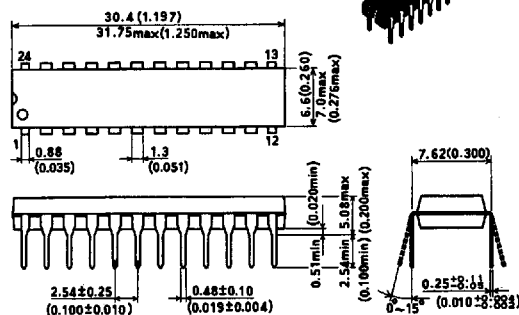
• DP-24



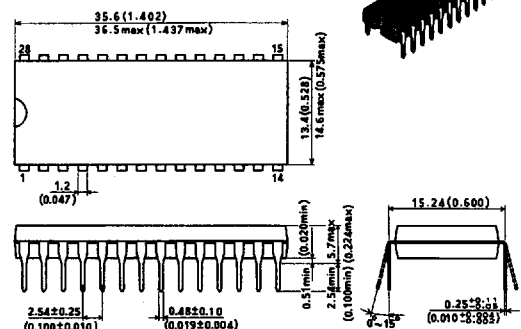
• DP-24A



• DP-24N



• DP-28

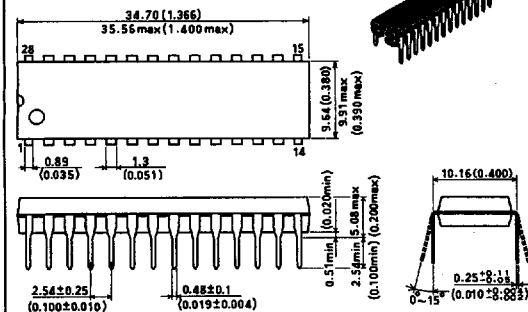


• Dual-in-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

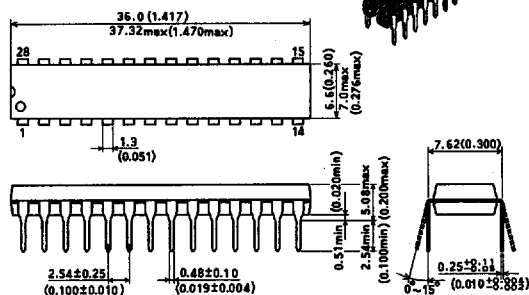
Unit: mm (inch) Scale 3/2

• DP-28C

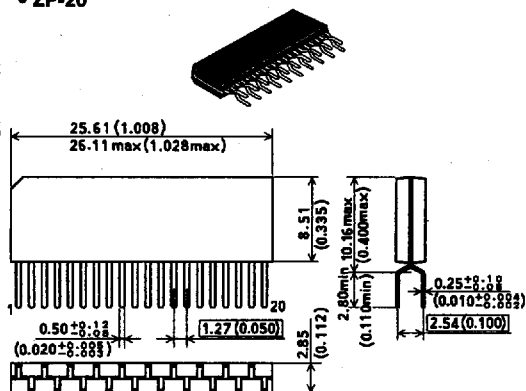


• DP-28N

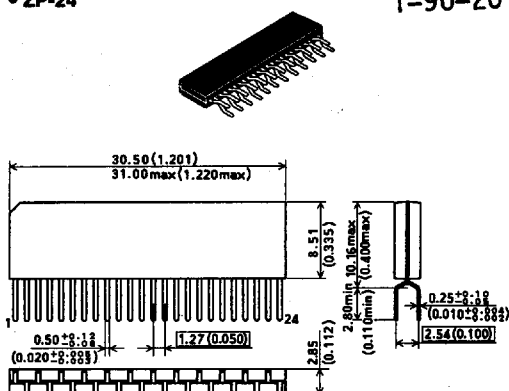
T-90-20



• ZP-20

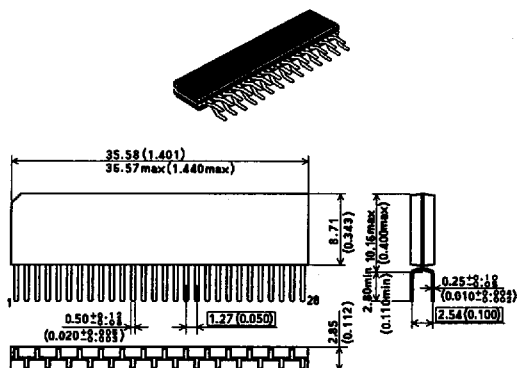


• ZP-24

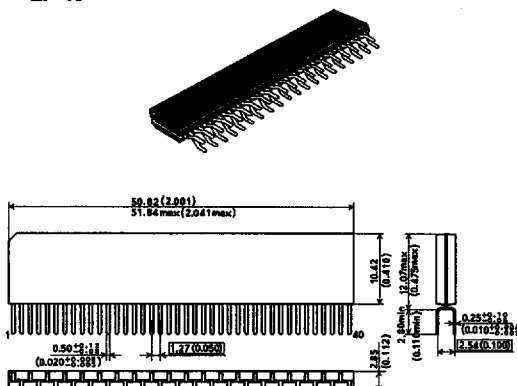


T-90-20

• ZP-28



• ZP-40



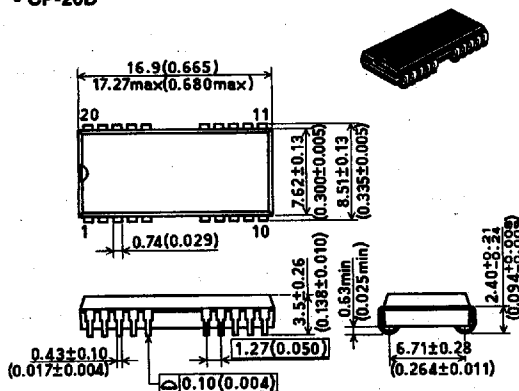
• Flat Package (J-bend Leads)

HITACHI/ LOGIC/ARRAYS/MEM

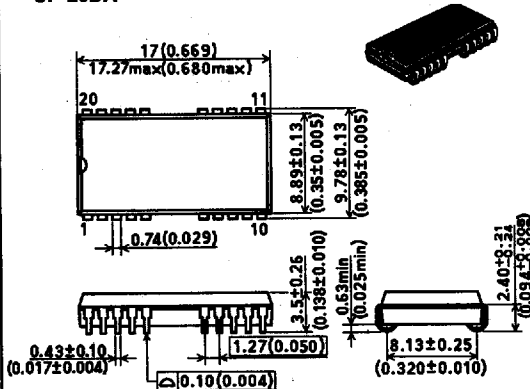
Unit: mm (inch) Scale 3/2

T-90-20

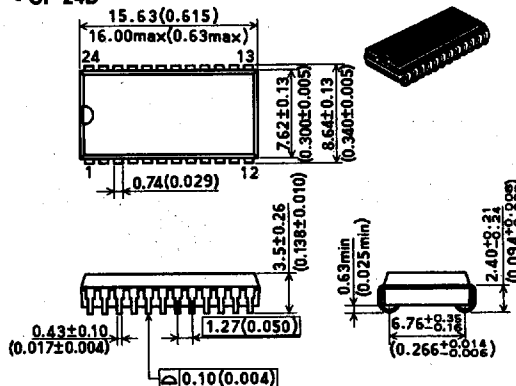
• CP-20D



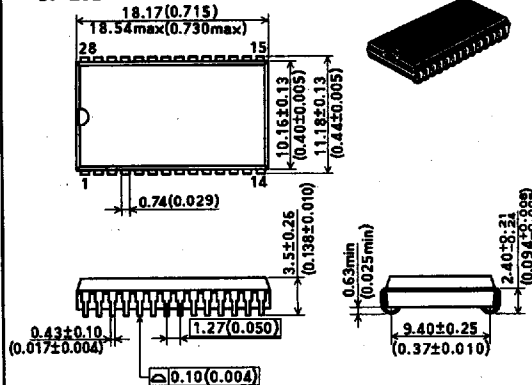
• CP-20DA



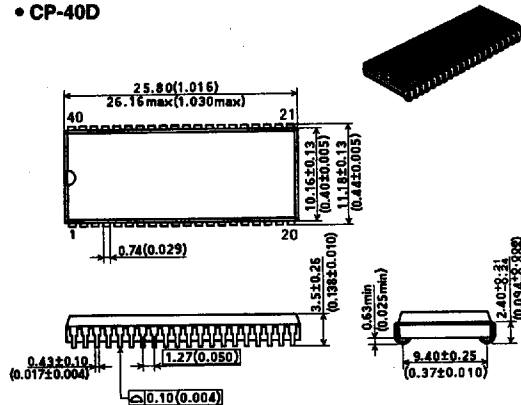
• CP-24D



• CP-28D



• CP-40D

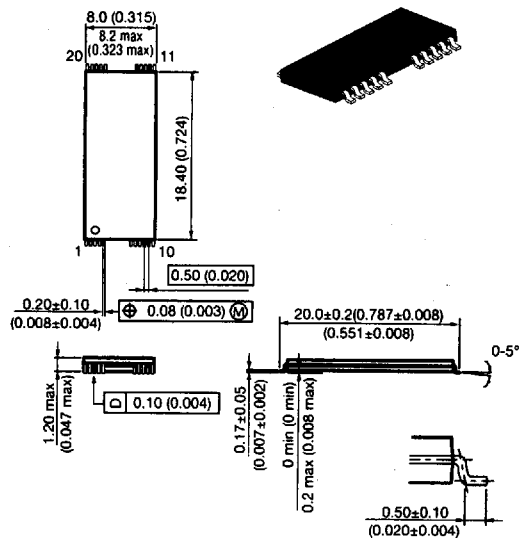


• TSOP (Thin Small Outline Package)

HITACHI/ LOGIC/ARRAYS/MEM

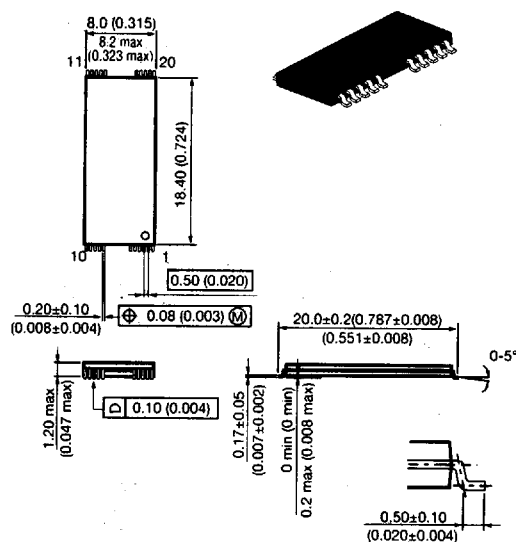
Unit: mm (inch) Scale 3/2

• TFP-20DA

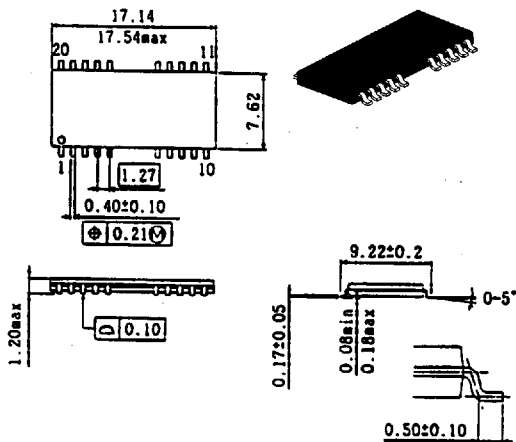


• TFP-20DAR

T-90-20



• TTP-20D



• TTP-20DR

