FX-702-SYNCE-156M250000

Complete VCSO Based Phase Lock Loop

For Synchronous Ethernet Jitter Attenuation

Helping Customers Innovate, Improve & Grow

Description

The FX-702 is a low jitter precision frequency translator that provides clock smoothing/jitter attenuation of a 156.25 MHz input clock. The FX-702's superior jitter performance is achieved through the PLL's integrated VCSO. The FX-702 is housed in a hermetically sealed leadless surface mount package offered on tape and reel.

Features

- 5 x 7.5 x 2.5 mm Package
- Jitter Attenuation at 156.25 MHz
- Integrated Phase Jitter < 200 fsec
- VCSO based PLL for Ultra-Low Jitter
- CMOS / LVDS / LVPECL Inputs compatible
- Differential LVPECL Output
- CMOS Lock Detect
- -40°/+85°C Temperature Range
- Fully Compatible for Lead Free Assembly

Applications

- Jitter Attenuation
- Clock Smoothing
- Synchronous Ethernet, G.8262

Block Diagram

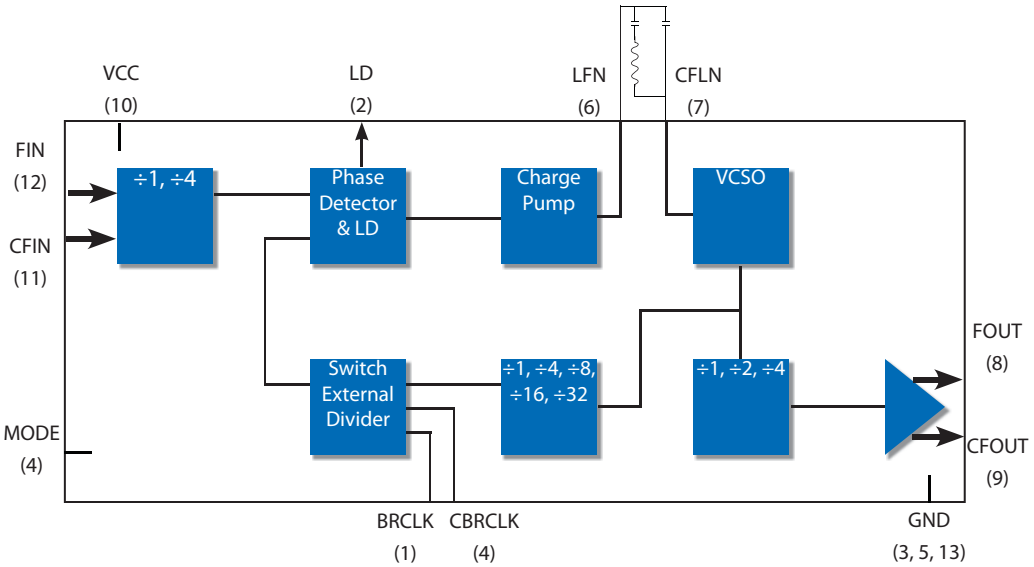


Figure 1. Functional block diagram

Vectron International • 267 Lowell Road, Hudson, NH 03051 • Tel: 1-88-VECTRON-1 • http://www.vectron.com

Performance Specifications

Table 1. Electrical Performance

Parameter	Symbol	Min	Typical	Maximum	Units
Frequency [1, 2, 3]					
Input Frequency	F_{IN}		156.25		MHz
Output Frequency	F_{OUT}		156.25		MHz
Capture Range [1, 2, 3]	APR	±100			
Supply					
Voltage [2, 3]	V_{CC}	2.97	3.3	3.63	V
Current (No Load) [3]	I_{CC}			100	mA
LVCMOS Input [2, 3]					
Input High Voltage	V_{IH}	2.0		V_{CC}	V
Input Low Voltage	V_{IL}	0		0.8	V
LVPECL Input					
Peal-Peak Amplitude Swing [6, 7]		0.20		3.00	V
Lock Detect Output					
Output High Voltage	V_{OH}	0.9*V_{CC}			V
Logic Low Voltage	V_{OL}			0.1*V_{CC}	V
Outputs					
Mid Level - LVPECL [2, 3]		V_{CC}-1.4	V_{CC}-1.25	V_{CC}-1.0	V
Swing - LVPECL [2, 3]		450	600	950	mV-pp
Current [5]	I_{OUT}			20	mA
Rise Time [4, 5]	t_R			400	ps
Fall Time [4, 5]	t_F			400	ps
Symmetry [2, 3]	SYM	45	50	55	%
Jitter Generation - 156.25 MHz output (12kHz-20MHz BW) [5]	Φ_J		150	200	fs-rms
Operating Temp	T_{OP}	-40/85			ºC

1. See Standard Frequencies and Ordering Information.
2. Parameters are tested with production test circuit below (Fig 1).
3. Parameters are tested at ambient temperature with test limits guard banded for specified operating temperature.
4. Measured from 20% to 80% of a full output swing (Fig 2).
5. Not tested in production, guaranteed by design, verified at qualification.
6. Minimum Input Low Voltage not to exceed 2.125 V. Minimum Input High Voltage not to go below 1.49 V.
7. AC coupling is recommended. There is an internal pull-up and pull-down resistor on all clock inputs (Fin, BRCLK).

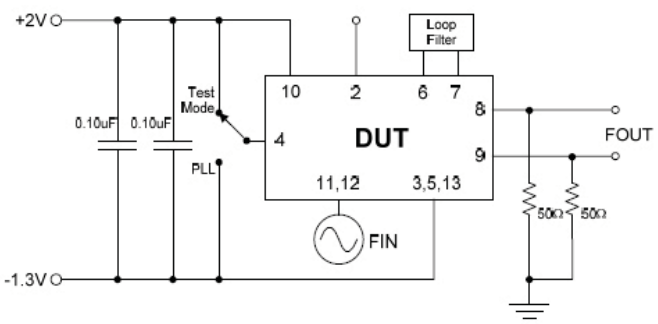


Figure 1. LVPECL Test Circuit

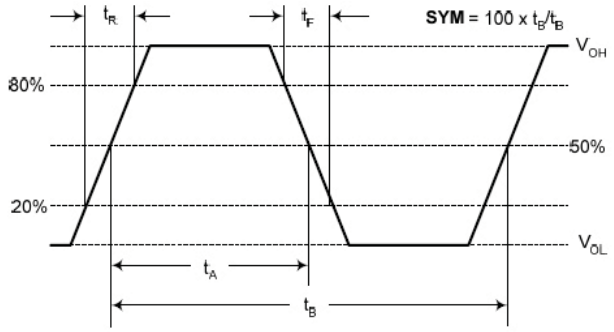


Figure 2. 10K LVPECL Waveform

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{CC}	0 to 6	V
Input Current	I_{IN}	100	mA
Output Current	I_{OUT}	25	mA
Storage Temperature	T_{STR}	-55 to 125	ºC
Soldering Temperature/Duration	T_{PEAK}/t_P	260 / 40	ºC/sec

Reliability

The FX-702 is capable of meeting the following qualification tests:

Table 3. Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016
Moisture Sensitivity Level Rating	MSL 1

Handling Precautions

Although ESD protection circuitry has been designed into the the FX-702, proper precautions should be taken when handling and mounting. VI employs a Human Body Model (HBM) and a Charged Device Model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model.

Table 4. Predicted ESD R$atings

Model	Class	Minimum	Conditions
Human Body Model	2	2000 V	MIL-STD 883, Method 3015
Charged Device Model	C5	1000 V	JEDEC, JESD22-C101
Machine Model	M3	200 V	ESD STM5.2-1999

Table 5. Reflow Profile (IPC/JEDEC J-STD-020C)		
Parameter	Symbol	Value
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 ºC/sec Max
Time Above 217 ºC	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 ºC	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 ºC/sec Max

The device has been qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The FX-702 device is hermetically sealed so an aqueous wash is not an issue.

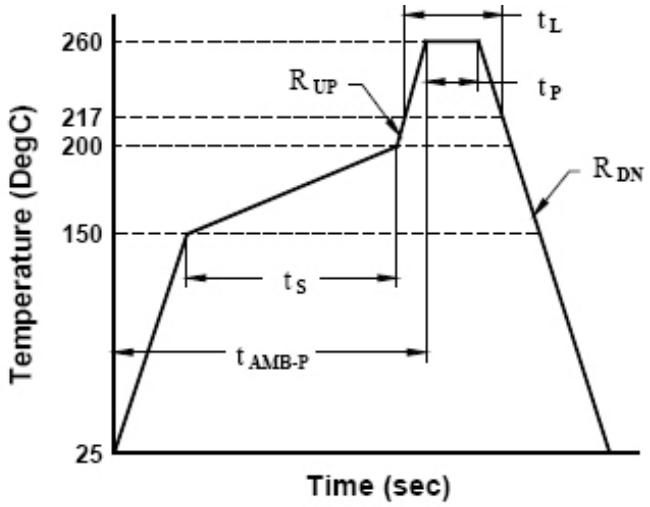


Figure 3. Suggested IR Profile

Table 6. Tape and Reel Information												
Tape Dimensions (mm)					Reel Dimensions (mm)							
W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#/Reel
16	7.5	1.5	4	8	178	1.5	13	20.2	50	16.4	22.4	200

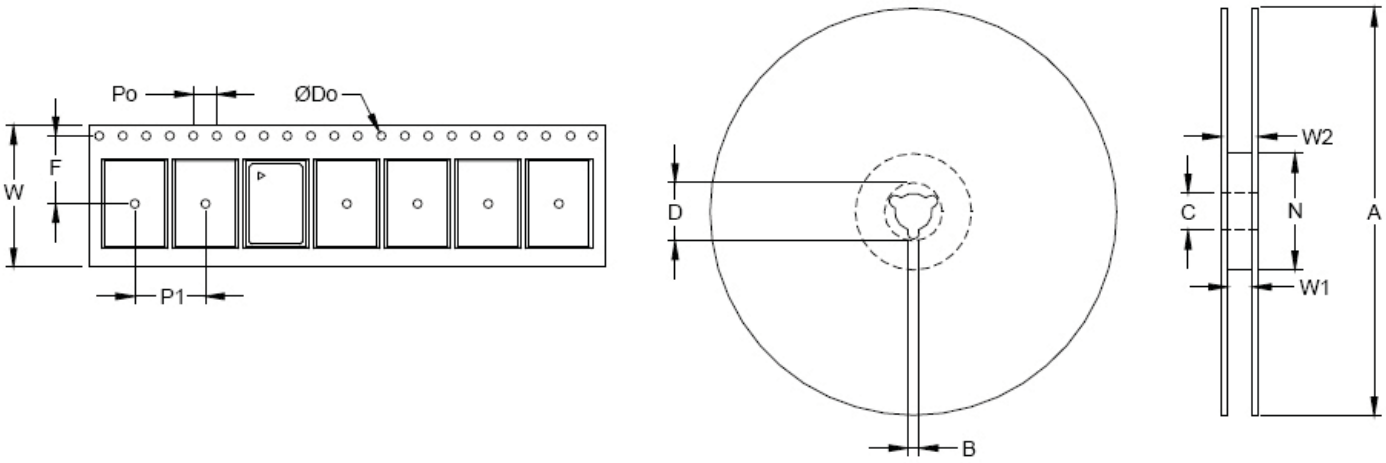


Figure 4. Tape and Reel

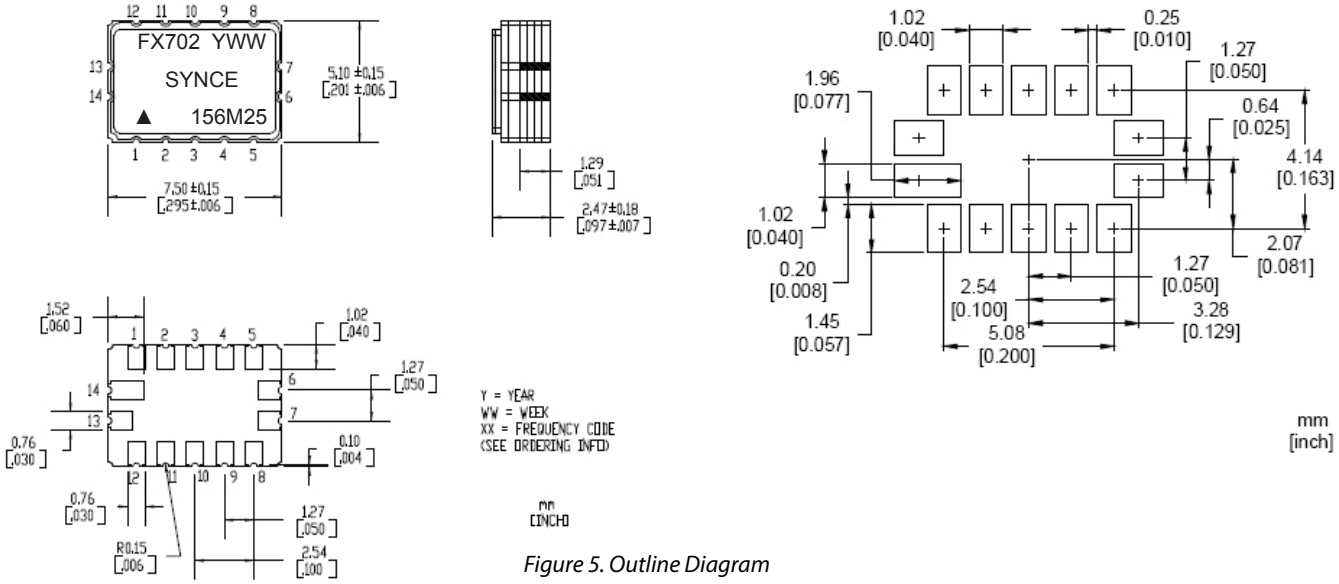


Figure 5. Outline Diagram

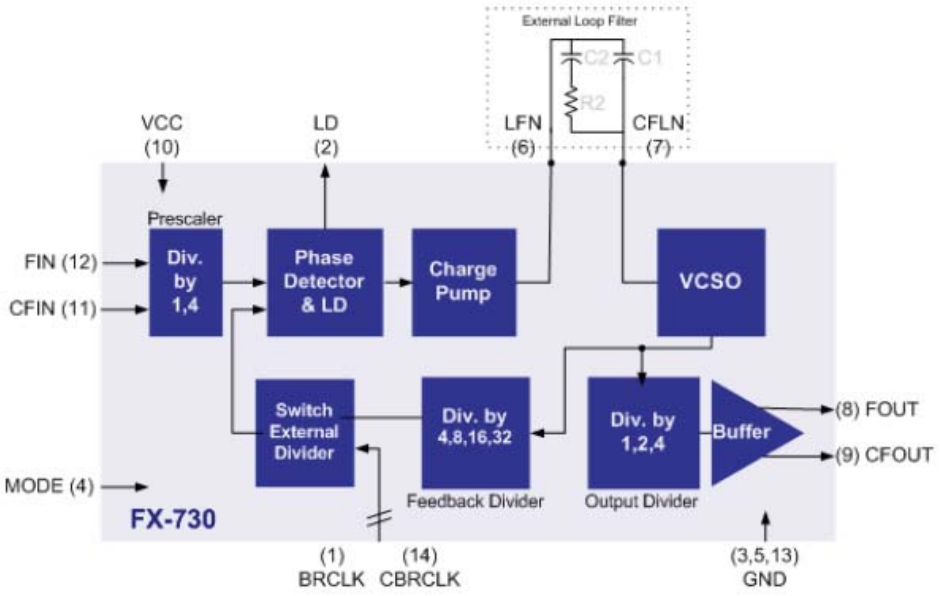
Table 7. Pin Functions

Pad #	Symbol	I/O	Level	Function
1	BRCLK	I	NC or LVPE-CL, LVDS	NC or For External divider application = PD Feedback Frequency
2	LD[1]	O	CMOS	Lock Detect Logic 0 = FX Locked Logic 1 - No Input Output transitioning = Out of Lock
3	GND	GND	Supply	Case and electrical ground
4	MODE[2]	I	CMOS	FX Operating Mode Logic 0 = Standard PLL (Normal Setting) Logic 1 = FIN coupled to FOUT
5	GND	GND	Supply	Case and electrical ground
6	LFN		Analog	Loop Filter Node
7	CLFN		Analog	Complementary Loop Filter Node
8	FOUT	O	LVPECL or LVDS	Frequency Output
9	CFOUT	O	LVPECL or LVDS	Complementary Frequency Output
10	VCC	I	Supply	Power Supply Voltage (+3.3V ±5%)
11	CFIN	I	LVPECL	Complemetary Input Frequency For CMOS inouts, AC-couple unused inputto ground or negative supply
12	FIN	I	CMOS or LVPECL	Input Frequency
13	GND	GND	Supply	Case and electrical ground
14	CBRCLK	I	NC or LVPE-CL, LVDS	NC or For External divider applications = Comp. PD Feedback Frequency

1. It is recommended that a buffer driver is used for best noise isolation.
2. Do not leave the MODE pin floating, it should be set to logic 0 or ground for normal operation.
3. BRCLK and CBRCLK should be left floating if not used.
4. FIN, CFIN, BRCLK, and CBRCLK have internal pull-up/pull-down resistors and it is recommended to AC couple these inputs.

Application Circuits

The FX-702 includes a phase detector, charge pump, frequency dividers and a VCSO with its own an associated divide-by function. The addition of the simple external loop filter shown below completes the design of this low jitter VCXO based PLL.



R2 = 5.3 Kohm C2 = 10uF C1 = 1nF

The above circuit has a 300 Hz loop bandwidth.

Figure 6. 156.25 MHz to 156.25 MHz Jitter Attenuation/Clock Smoothing

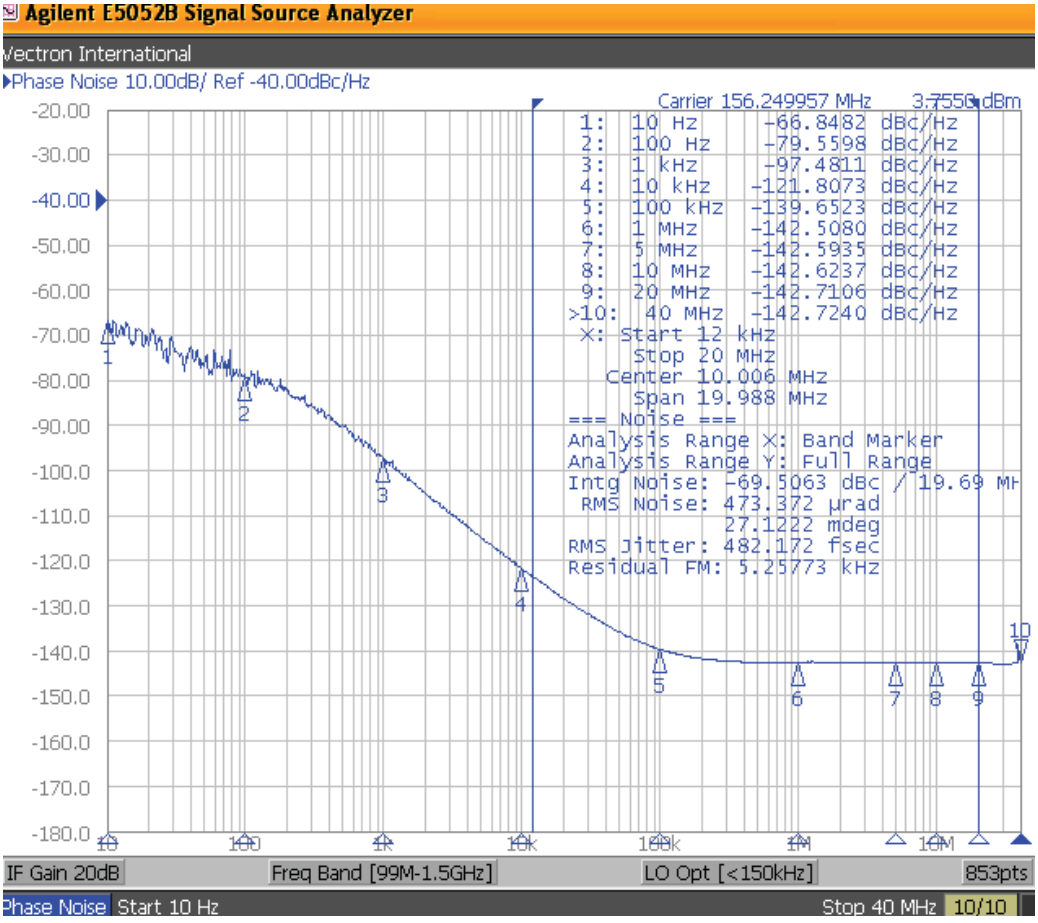


Figure 7. Typical Phase Noise Performance for FX-702-SYNCE-156M250000

Ordering Information

FX- 702 - S Y N C E - 156M250000

Product Family
FX: Frequency Translator

Package
702: 5.0 x 7.5 x 2.0mm

Input
E: 3.3 Vdc ±10%

Output
LVPECL

Operating Temperature
-40 to 85 °C

Absolute Pull Range
± 100 ppm

Input Frequency
Output Frequency

For Additional Information, Please Contact

USA:
Vectron International
267 Lowell Road
Hudson, NH 03051
Tel: 1.888.328.7661
Fax: 1.888.329.8328

Europe:
Vectron International
Landstrasse, D-74924
Neckarbischofsheim, Germany
Tel: +49 (0) 3328.4784.17
Fax: +49 (0) 3328.4784.30

Asia:
Vectron International
1F-2F, No 8 Workshop, No 308 Fenju Road
WaiGaoQiao Free Trade Zone
Pudong, Shanghai, China 200131
Tel: 86.21.5048.0777
Fax: 86.21.5048.1881