

12 Bit D/A Converter - Radiation Hardened

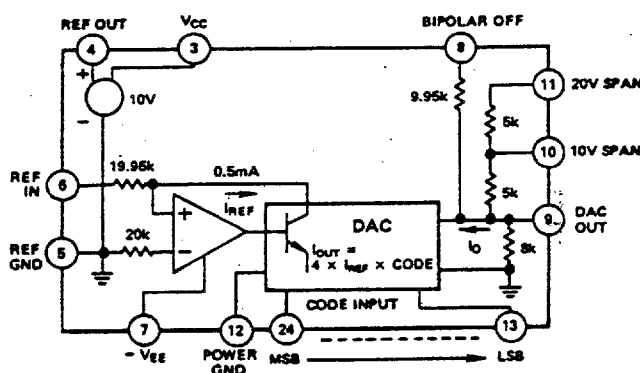
565ARP

High Speed 12 Bit Monolithic
Digital to Analog Converter

*For Space
Applications*

SEI's 565ARP (RP for RAD-PAK®) high speed 12-bit monolithic digital to analog converter features a minimum of 100 kilorad (Si) total dose tolerance. Using SEI's radiation hardened RAD-PAK® packaging technology, the 565ARP uses 12 precision, high-speed bipolar current-steering switches, control amplifier and a laser-trimmed thin-film resistor network to produce a very fast, high accuracy analog output current. The 565ARP also includes a buried zener reference that features low-noise, long-term stability and temperature drift characteristics comparable to the best discrete reference diodes.

The 565ARP has a 10-90% full-scale transition time less than 35ns and settles to within $\pm 1/2$ LSB in 250ns max. High speed and accuracy make the 565ARP the ideal choice for high-speed display drivers as well as fast analog-to-digital converters. The wide output compliance range of the 565ARP is ideally suited for fast, low noise, accurate voltage output configurations without an output amplifier.



565ARP Functional Block Diagram

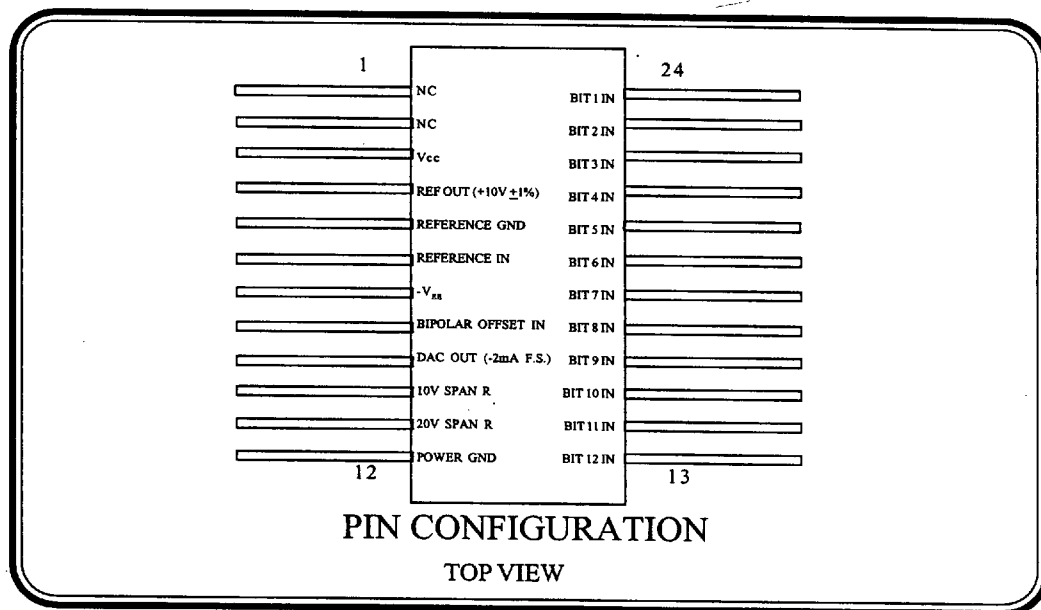


SPACE
ELECTRONICS
INCORPORATED

Tel: (619) 452-4167 Fax: (619) 452-5499

Radiation Hardened 565ARP

High Speed 12 Bit Digital to Analog
Converter



Features:

- 12-Bit High Speed DAC
- Pin Compatible with Analog Devices AD565A
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- Total Dose Hardness > 100krad (Si)
- Excellent Single Event Performance
 - No Single Event Latchup > 120 MeV/mg/cm²
 - SEU LET Threshold > 120 MeV/mg/cm²
- Package:
 - 24 Pin RAD-PAK® Flat Pack
 - 24 Pin RAD-PAK® DIP
- Very High-Speed Settling to 1/2LSB - 250ns max
- Full-Scale Switching Time: 30ns
- Guaranteed for Operation with ±12V Supplies
- Linearity Guaranteed Over Temperature:
 - 3/4LSB max: 565ARP-1
 - 1/2LSB max: 565ARP-2
- Monotonicity Guaranteed Over Temperature
- Low Power: 225mW max
- Class S Screening per TM5004
- QCI per TM5004

Specifications and design are subject to change without notice.



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For Further Information Contact:

Space Electronics Inc.
4031 Sorrento Valley Blvd., San Diego, CA 92121
(619) 452-4167 Fax (619) 452-5499

9011241 0000354 342 352

565ARP ABSOLUTE MAXIMUM RATINGS
($T_A = +25\text{ }^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	MIN	MAX	UNITS
V_{CC} to Power Ground		0	+18	V
V_{EE} to Power Ground		0	-18	V
Voltage on DAC Output (Pin 9)		-3	+12	V
Digital Inputs (Pins 13 to 24) to Power Ground		-1.0	+7	V
Ref In to Reference Ground		-12	+12	V
Bipolar Offset to Reference Ground		-12	+12	V
10V Span R to Reference Ground		-12	+12	V
20V Span R to Reference Ground		-24	+24	V
Ref Out - Indefinite Short to Power Ground Momentary Short to V_{CC}				
Power Dissipation	P_d		1000	mW
Storage Temperature Range	T_s	-65	+150	$^{\circ}\text{C}$



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SAN DIEGO, CA 92121
PHONE: (619) 452-4167
FAX: (619) 452-5499
INTERNET: 102005.1635@COMPUSERVE.COM

■ 9011241 0000355 289 ■ 353

565ARP SPECIFICATIONS

Test	Symbol	Device	Min	Max	Test Condition 1/	Units
Relative Accuracy	RA	-1		3/4	All Bits with Positive Errors On. All Bits with Negative Errors On.	± LSB
		-2		1/2		
Differential Nonlinearity	DNL	-1, 2		1	Major Transitions	± LSB
Gain Error	A _E	-1, 2		0.25	R _{REF} = 50Ω Fixed T _A = +25 °C	± % of FS
Gain Error Temperature Coefficient	TCA _E	-1		30		± ppm of FS/°C
		-2		15		
Offset Error	V _{OS}	-1, 2		0.05	T _A = +25 °C	± % of FS
Offset Error Temperature Coefficient	TCV _{OS}	-1, 2		2		± ppm of FS/°C
Bipolar Zero Error 2/	B _{PZE}	-1		0.15	R _{BO} = 50W Fixed T _A = +25 °C	± % of FS
		-2		0.10		
Bip Zero Error Temperature Coefficient 2/	TCB _{PZE}	-1, 2		10		± ppm of FS/°C
Input Resistance	R _{IN}	-1, 2	15	25	T _A = +25 °C	kΩ
Reference Output Voltage 3/	V _{REF}	-1, 2	9.90	10.10		+V
Reference Output Current 4/	I _{REF}	-1, 2	1.5		T _A = +25 °C	+mA
Full Scale Transition	t _{FS}	-1, 2		30	10% to 90% Delay Plus Rise Time T _A = +25 °C	ns
		-1, 2		50	90% to 10% Delay Plus Fall Time T _A = +25 °C	ns
Output Current Settling Time	t _{SL}	-1, 2		250	T _A = +25 °C	ns
Compliance Voltage	CV	-1, 2	-1.5	10	T _A = +25 °C	V
Output Resistance	R _{OUT}	-1, 2	6	10	Exclusive of Span Resistors T _A = +25 °C	kΩ



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9011241 0000356 115 354

565ARP SPECIFICATIONS (continue)

Test	Symbol	Device	Min	Max	Test Condition	1/	Units
Output Current	I_{OUT}	-1, 2	1.6	2.4	Unipolar (All Bits On) $T_A = +25^\circ\text{C}$		-mA
			0.8	1.2	Bipolar (All Bits On) $T_A = +25^\circ\text{C}$		
Power Supply Rejection Ratio	PSRR	-1, 2		10	$V_{CC} = +11.4\text{V to } 16.5\text{V dc}$ $T_A = +25^\circ\text{C}$		$\pm$ ppm of FSR/%
				25	$V_{EE} = -11.4\text{V to } -16.5\text{V dc}$ $T_A = +25^\circ\text{C}$		
Power Supply Current 4/ 5/	I_{CC}	-1, 2		5	$T_A = +25^\circ\text{C}$		+mA
	I_{EE}	-1, 2		18	$T_A = +25^\circ\text{C}$		-mA
Power Dissipation	P_D	-1, 2		345	$T_A = +25^\circ\text{C}$		mW
Digital Input High Voltage	V_{IH}	-1, 2	2.0	5.5	$T_A = +25^\circ\text{C}$		+V
Digital Input Low Voltage	V_{IL}	-1, 2		0.8	$T_A = +25^\circ\text{C}$		+V
Digital Input High Current	I_{IH}	-1, 2		300	$V_{IH} = 5.5\text{V}$ $T_A = +25^\circ\text{C}$		+ μA
Digital Input Low Current	I_{IL}	-1, 2		100	$V_{IL} = 0\text{V}$ $T_A = +25^\circ\text{C}$		+ μA

Note:

1/ $V_{CC} = +15\text{V}$, $V_{EE} = -15\text{V}$, $V_{IH} = 2.0\text{V}$, $V_{IL} = 0.8\text{V}$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ unless otherwise indicated.

2/ MSB on; all other bits off.

3/ The reference output is loaded with 0.5mA reference input current. The reference must be buffered to supply external loads at elevated temperatures.

4/ Guaranteed for $+11.4 \leq V_{CC} \leq +16.5\text{V}$.

5/ Guaranteed for $-11.4 \geq V_{EE} \geq -16.5\text{V}$.



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9011241 0000357 051 355

565ARP PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	NC	No Connection
2	NC	No Connection
3	V _{CC}	Positive Supply Voltage
4	REF OUT	Reference Output
5	REFERENCE GND	Reference Ground
6	REFERENCE IN	Reference Input
7	-V _{EE}	Negative Supply Voltage
8	BIPOLAR OFFSET IN	Bipolar Offset Input
9	DAC OUT	Digital-to-Analog Converter Output
10	10V SPAN R	10 Volt Span Resistance
11	20V SPAN R	20 Volt Span Resistance
12	POWER GND	Power Ground
13	BIT 12 IN	Data Bit 12 (LSB)
14	BIT 11 IN	Data Bit 11
15	BIT 10 IN	Data Bit 10
16	BIT 9 IN	Data Bit 9
17	BIT 8 IN	Data Bit 8
18	BIT 7 IN	Data Bit 7
19	BIT 6 IN	Data Bit 6
20	BIT 5 IN	Data Bit 5
21	BIT 4 IN	Data Bit 4
22	BIT 3 IN	Data Bit 3
23	BIT 2 IN	Data Bit 2
24	BIT 1 IN	Data Bit 1 (MSB)

565ARP PACKAGE ORDERING GUIDE

PACKAGE STYLE	CASE OUTLINE	1/	DESCRIPTION
D	D-24		24 Pin Dual In Line Package
F	F-24		24 Pin Flat Package

Note:

1/ For outline information, see Appendix A (Package Information - Outline Dimension)



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9011241 0000358 T98 356