Description

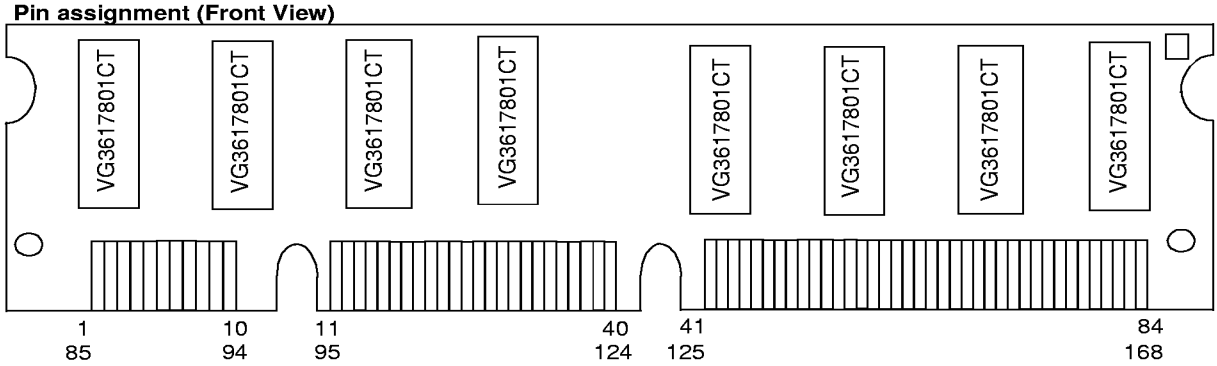
The VS26417801C and VS46417801C are 2M x 64 - bit and 4M x 64 - bit dual - in - line synchronous dynamic RAM module (DIMM). It is mounted with 8/16 pieces of 2M x 8 synchronous DRAM(VG3617801CT), and each in a standard 44 pin TSOP package. The VS26417801C and VS46417801C make high density possible without utilizing the surface mount technology on the printed circuit board. Decoupling capacitors are mounted on power supply line for noise reduction. The module uses serial presence detects implemented via a 2k-bit serial EEPROM component.

Features

VS26417801C, VS46417801C :

- Single 3.3V (±0.3V) power supply
- Utilizes 100MHz SDRAM components
- Fully synchronous with all signals referenced to a positive clock edge
- Programmable burst length (1,2,4,8 & Full page)
- Programmable wrap sequence (Sequential/Interleave)
- Automatic precharge and controlled precharge
- Auto refresh and self refresh modes
- I/O level : LVTTL interface
- Random column access in every cycle
- 2048 refresh cycles/32ms
- Serial Presence Detect (SPD)
- JEDEC Standard pinout
- Comply to Intel PC - 100 4clock unbuffered SDRAM DIMM spec.

Pin assignment (Front View)



Pin Out

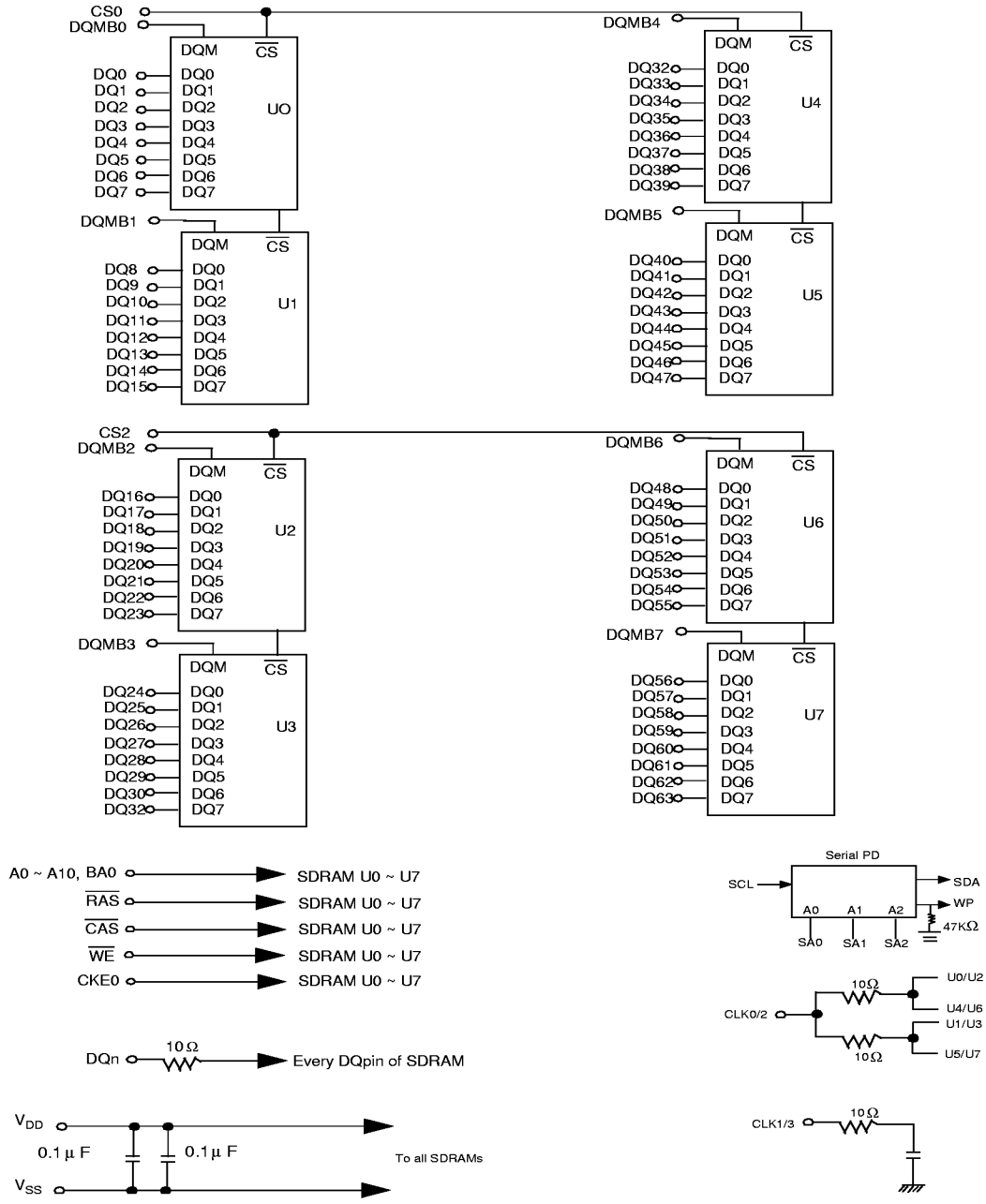
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	22	NC	43	V_{SS}	64	V_{SS}	85	V_{SS}	106	NC	127	V_{SS}	148	V_{SS}
2	DQ0	23	V_{SS}	44	NC	65	DQ21	86	DQ32	107	V_{SS}	128	CKE0	149	DQ53
3	DQ1	24	NC	45	$\overline{CS2}$	66	DQ22	87	DQ33	108	NC	129	$\overline{CS3}$/NC *	150	DQ54
4	DQ2	25	NC	46	DQMB2	67	DQ23	88	DQ34	109	NC	130	DQMB6	151	DQ55
5	DQ3	26	V_{DD}	47	DQMB3	68	V_{SS}	89	DQ35	110	V_{DD}	131	DQMB7	152	V_{SS}
6	V_{DD}	27	$\overline{WE}$	48	NC	69	DQ24	90	V_{DD}	111	$\overline{CAS}$	132	NC	153	DQ56
7	DQ4	28	DQMB0	49	V_{DD}	70	DQ25	91	DQ36	112	DQMB4	133	V_{DD}	154	DQ57
8	DQ5	29	DQMB1	50	NC	71	DQ26	92	DQ37	113	DQMB5	134	NC	155	DQ58
9	DQ6	30	$\overline{CS0}$	51	NC	72	DQ27	93	DQ38	114	$\overline{CS1}$/NC *	135	NC	156	DQ59
10	DQ7	31	NC	52	NC	73	V_{DD}	94	DQ39	115	$\overline{RAS}$	136	NC	157	V_{DD}
11	DQ8	32	V_{SS}	53	NC	74	DQ28	95	DQ40	116	V_{SS}	137	NC	158	DQ60
12	V_{SS}	33	A0	54	V_{SS}	75	DQ29	96	V_{SS}	117	A1	138	V_{SS}	159	DQ61
13	DQ9	34	A2	55	DQ16	76	DQ30	97	DQ41	118	A3	139	DQ48	160	DQ62
14	DQ10	35	A4	56	DQ17	77	DQ31	98	DQ42	119	A5	140	DQ49	161	DQ63
15	DQ11	36	A6	57	DQ18	78	V_{SS}	99	DQ43	120	A7	141	DQ50	162	V_{SS}
16	DQ12	37	A8	58	DQ19	79	CLK2	100	DQ44	121	A9	142	DQ51	163	CLK3
17	DQ13	38	A10	59	V_{DD}	80	NC	101	DQ45	122	BA0	143	V_{DD}	164	NC
18	V_{DD}	39	NC	60	DQ20	81	WP	102	V_{DD}	123	NC	144	DQ52	165	SA0
19	DQ14	40	V_{DD}	61	NC	82	SDA	103	DQ46	124	V_{DD}	145	NC	166	SA1
20	DQ15	41	V_{DD}	62	NC	83	SCL	104	DQ47	125	CLK1	146	NC	167	SA2
21	NC	42	CLK0	63	CKE1/NC *	84	V_{DD}	105	NC	126	NC	147	NC	168	V_{DD}

Note : * : 2M x 64 version

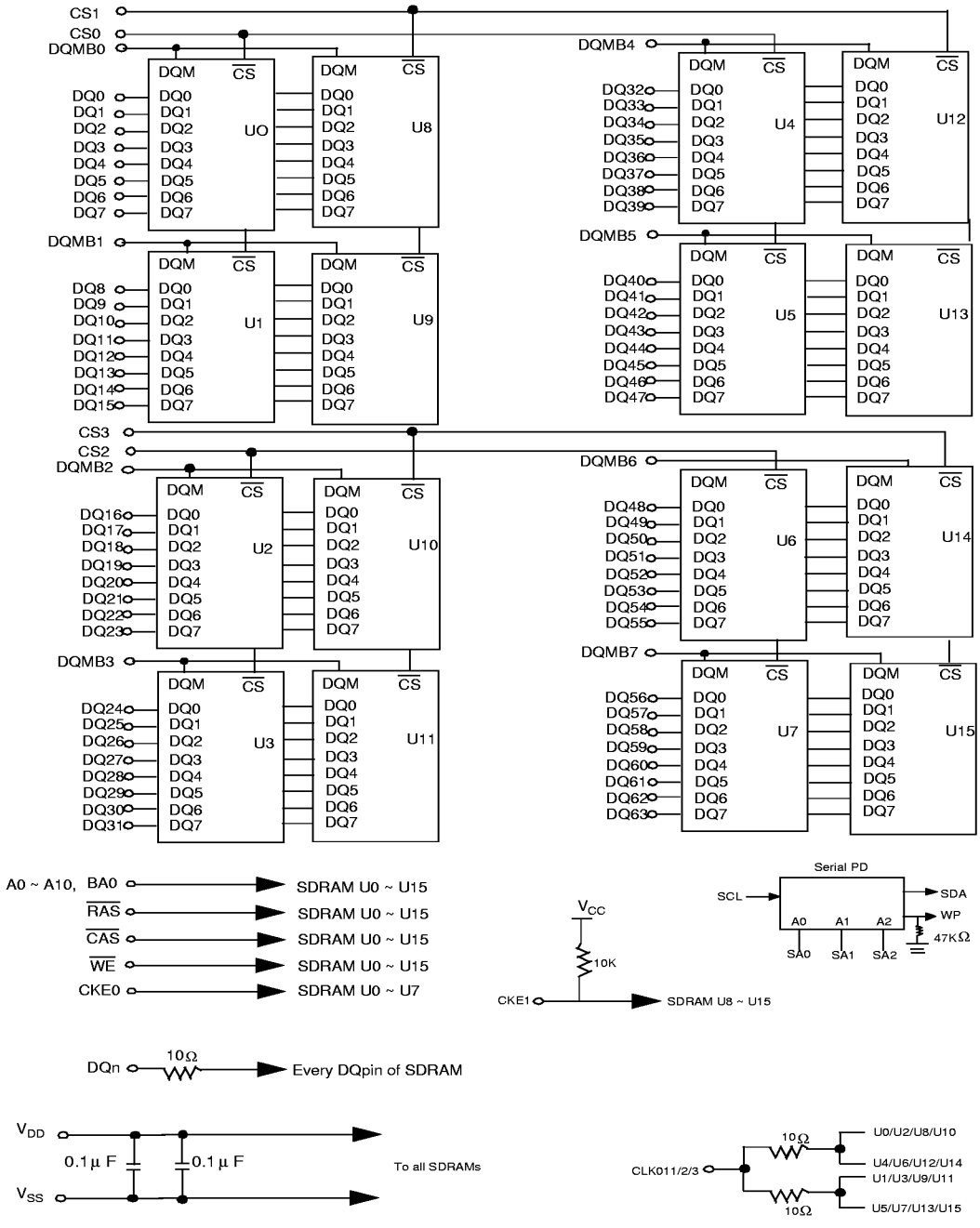
Pin Description

Pin Name	Function	Pin Name	Function
A0 ~ A10	Address input	DQMB0 ~ DQMB7	DQ mask enable
DQ0 ~ DQ63	Data-in/Data - out	CLK0 ~ CLK3	Clock input
$\overline{RAS}$	Row address strobe	VDD	power
$\overline{CAS}$	Column address strobe	VSS	Ground
$\overline{WE}$	Write enable	SA0 ~ SA2	Serial presence detect address
BA0	Bank address	SCL	Serial presence detect clock
CKE0, CKE1	Clock enable	SDA	Serial presence detect data
CS0 ~ CS3	Chip select	NC	No connect
WP	Write protect		

Block Diagram (2M x 64)



Block Diagram (4M x 64)



Command Truth Table

FUNCTION	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0	A10	A9 - A0
		n - 1	n							
Device deselect	DESL	H	X	H	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X
Mode rgister set	MRS	H	X	L	L	L	L	X	X	V
Bank activate	ACT	H	X	L	L	H	H	V	V	V
Read	READ	H	X	L	H	L	H	V	L	V
Read with auto precharge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with auto precharge	WRITA	H	X	L	H	L	L	V	H	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Burst stop	BST	H	X	L	H	H	L	X	X	X

Absolute Maximum Ratings

Parameter	Symbol	Value		Unit
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-1.0 to + 4.6		V
Supply voltage relative to Vss	V_{DD}	-1.0 to + 4.6		V
Short circuit iotput current	I_{OUT}	50		mA
Power dissipation	P_D	2Mx64	8	W
		4Mx64	16	
Operating temperature	T_{OPT}	0 to + 70		°C
Storage temperature	T_{STG}	-55 to + 125		°C

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Input High Voltage, all inputs	V_{IH}	2.0	-	V_{DD} + 0.3	V	1
Input Low Voltage, all inputs	V_{IL}	-0.3	-	0.8	V	2

Note 1. Overshoot limit: $V_{IH(max.)}$= V_{DD} + 2.0V with a pulse width < 3ns

2. Undershoot limit: V_{IL}=V_{SS} - 2.0V with a pulse < 3ns and -1.5V with a pulse < 5ns

Capacitance

Ta = 25°C,f = 1MHZ

Parameter	Symbol	Size	Type	Max	Unit
Input capacitance (Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C11	2M x 64 4M x 64	-	50 85	pF
Input capacitance (CS0 ~ CS3)	C12	2M x 64 4M x 64	-	25 25	pF
Input capacitance (CKE0, CKE1)	C13	2M x 64 4M x 64	-	50 50	pF
Input capacitance (CLK0~CLK3)	C14	2M x 64 4M x 64	-	25 30	pF
Input capacitance(DQMB0 ~ DQMB7)	C15	2M x 64 4M x 64	-	15 22	pF
Input capacitance(DQ0 ~ DQ63)	C16	2M x 64 4M x 64	-	14 20	pF

DC Characteristics(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test Conditions		VS26417801C						Unit	Notes
				-8H		-8L		-10			
				Min	Max	Min	Max	Min	Max		
Operating current	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC\ (MIN.)}$, Io = 0mA One bank active	CL = 3		720		720		680	mA	1,2
			CL = 2		680		680		640		
Precharge standby current in power down mode	$I_{CC2}P$	CKE ≤ $V_{IL(MAX.)}$ t_{CK} = 15ns			24		24		24	mA	
	$I_{CC2}PS$	CKE ≤ $V_{IL(MAX)}$ t_{CK} = ∞			16		16		16		
Precharge standby current in Nonpower down mode	$I_{CC2}N$	CKE ≥ $V_{IH(MIN.)}$ t_{CK} = 15ns CS ≥ $V_{IH(MIN.)}$ Input signals are changed. one time during 30ns.			300		300		300	mA	
	$I_{CC2}NS$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = ∞ CLK ≤ $V_{IL(MAX.)}$ Input signals are stable.			60		60		60		
Active standby current in power down mode	$I_{CC3}P$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = 15ns			36		36		36	mA	
	$I_{CC3}PS$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = ∞			32		32		32		
Active standby current in nonpower down mode	$I_{CC3}N$	CKE ≥ $V_{IH(MAX.)}$, t_{CK} = 15ns CS ≥ $V_{IH(MIN.)}$ Input signals are changed one time during 30ns			300		300		300	mA	
	$I_{CC3}NS$	CKE ≥ $V_{IH(MIN.)}$ t_{CK} = ∞ CLE ≤ $V_{IL(MAX.)}$ Input signals are stable.			150		150		150		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK\ (MIN.)}$, Io = 0mA Burst length = 4	CL = 3		960		960		840	mA	1,2
			CL = 2		920		840		800		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC(MIN.)}$	CL = 3		880		880		800	mA	2
			CL = 2		840		840		760		
Self refresh current	I_{CC6}	CKE ≤ 0.2V			16		16		16	mA	
Input leakage current	I_{LI}	$V_{IN} \geq 0$, $V_{IN} \leq V_{DD}$ + 0.3V Pins not under test = 0V		-40	40	-40	40	-40	40	uA	
Output leakage current	I_{LO}	$V_{OUT} \geq 0$, $V_{OUT} \leq V_{DD}$ + 0.3V DQ# in H - Z., Dout disabled		-5	5	-5	5	-5	5	uA	
Output Low Voltage	V_{OL}	I_{OL} = 2mA			0.4		0.4		0.4	V	
Output High Voltage	V_{OH}	I_{OH} = -2mA		2.4		2.4		2.4		V	

Notes 1. I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.

2. I_{CC} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

DC Characteristics(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test Conditions		VS46417801C						Unit	Notes
				-8H		-8L		-10			
				Min	Max	Min	Max	Min	Max		
Operating current	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC\ (MIN.)}$, Io = 0mA One bank active	CL = 3		880		880		840	mA	1,2
			CL = 2		840		840		800		
Precharge standby current in power down mode	$I_{CC2}P$	CKE ≤ $V_{IL(MAX.)}$ t_{CK} = 15ns			48		48		48	mA	
	$I_{CC2}PS$	CKE ≤ $V_{IL(MAX)}$ t_{CK} = ∞			32		32		32		
Precharge standby current in Nonpower down mode	$I_{CC2}N$	CKE ≥ $V_{IH(MIN.)}$ t_{CK} = 15ns CS ≥ $V_{IH(MIN.)}$ Input signals are changed. one time during 30ns.			600		600		600	mA	
	$I_{CC2}NS$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = ∞ CLK ≤ $V_{IL(MAX.)}$ Input signals are stable.			120		120		120		
Active standby current in power down mode	$I_{CC3}P$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = 15ns			72		72		72	mA	
	$I_{CC3}PS$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = ∞			64		64		64		
Active standby current in nonpower down mode	$I_{CC3}N$	CKE ≥ $V_{IL(MAX.)}$, t_{CK} = 15ns CS ≥ $V_{IL(MIN.)}$ Input signals are changed one time during 30ns			600		600		600	mA	
	$I_{CC3}NS$	CKE ≥ $V_{IH(MIN.)}$ t_{CK} = ∞ CLE ≤ $V_{IL(MAX.)}$ Input signals are stable.			300		300		300		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK\ (MIN.)}$, Io = 0mA Burst length=4	CL = 3		1120		1120		1000	mA	1,2
			CL = 2		1080		1080		960		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC\ (MIN.)}$	CL = 3		1760		1760		1600	mA	2
			CL = 2		1680		1680		1520		
Self refresh current	I_{CC6}	CKE ≤ 0.2V			32		32		32	mA	
Input leakage current	I_{LI}	$V_{IN} \geq 0$, $V_{IN} \leq V_{DD}$ + 0.3V Pins not under test = 0V		-80	80	-80	80	-80	80	uA	
Output leakage current	I_{LO}	$V_{OUT} \geq 0$, $V_{OUT} \leq V_{DD}$ + 0.3V DQ# in H - Z., Dout disabled		-10	10	-10	10	-10	10	uA	
Output Low Voltage	V_{OL}	I_{OL} = 2mA			0.4		0.4		0.4	V	
Output High Voltage	V_{OH}	I_{OH} = -2mA		2.4		2.4		2.4		V	

Notes 1. I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.

2. I_{CC} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

A.C Characteristics

Test Conditions : (Ta = 0 to 70°C V_{DD} = 3.3V±0.3V , V_{SS} = 0V)

AC input Levels(V_{IH}/V_{IL})	2.0/0.8V	Input timing reference level/ Output timing reference leveel	1.4v
Input and fall time	1ns	Output load condition	50pF

Parameter	CAS Latency	symbol	VS26417801C/VS46417801C						Unit
			-8H		-8L		-10		
			Min	Max	Min	Max	Min	Max	
CLK cycle time	3	t_{CK3}	10		10		10		ns
	2	t_{CK2}	10		13		15		ns
CLK to valid output delay	3	t_{AC3}		6		6		8	ns
	2	t_{AC2}		6		7		8	ns
CLK high pulse width		t_{CH}	3		3		4		ns
CLK low pulse width		t_{CL}	3		3		4		ns
CKE setup time		t_{CKS}	2		2		3		ns
CKE hold time		t_{CKH}	1		1		1		ns
Address setup time		t_{AS}	2		2		3		ns
Address hold time		t_{AH}	1		1		1		ns
Command setup time		t_{CMS}	2		2		3		ns
Command hold time		t_{CMH}	1		1		1		ns
Data - in setup time		t_{DS}	2		2		3		ns
Data - in hold time		t_{DH}	1		1		1		ns
Output data hold time		t_{OH}	3		3		3		ns
CLK to output on low - Z		t_{LZ}	0		0		0		ns
CLK to output in Hi - Z		t_{HZ}	3	8	3	8	3	8	ns
Row active to active delay		t_{RRD}	20		20		20		ns
RAS to CAS delay		t_{RCD}	20		20		26		ns
Row precharge time		t_{RP}	20		20		26		ns
Row active time		t_{RAS}	50	120,000	50	120,000	60	120,000	ns
Row cycle time		t_{RC}	70		70		86		ns
Last data in to burst stop		t_{BDL}	1CLK		1CLK		1CLK		ns
Data - in to ACT (REF) command (Auto Precharge)		t_{DAL}	1CLK + t_{RP}		1CLK + t_{RP}		1CLK + t_{RP}		ns
Data - in to precharge		t_{DPL}	1 CLK		1 CLK		1 CLK		ns
Transition time		t_{T}	1	10	1	10	1	10	ns
Mode reg. set cycle		t_{RSC}	2 CLK		2 CLK		2 CLK		ns
Power down exit setup time		t_{PDE}	8		8		8		ns
Self refresh exit time		t_{SRX}	8		8		8		ns
Refresh time		t_{REF}		32		32		32	ms

Serial presence detect information(VS26417801C)

Byte	Function described	Function Supported			HEX		
		-8H	-8L	-10	-8H	-8L	-10
0	Number of bytes used by Vanguard			128			80
1	Total SPD memory size			256			8
2	Memory Type			SDRAM			4
3	Number of Row addresses			11			B
4	Number of Column addresses			9			9
5	Number of Banks on module			1			1
6	Module data width			64			40
7	Module data width (continued)			0			0
8	Module voltage interface lelevls			LVTTL			1
9	SDRAM cycle time. CAS latency = 3	10ns	10ns	10ns	A0	A0	A0
10	SDRAM access time from clock. CAS latency = 3	6ns	6ns	8ns	60	60	80
11	Module configuration type			Non - Parity			0
12	Refresh Rate/Type			15.6us/self			80
13	SDRAM width, Primary SDRAM			8			8
14	Error checking SDRAM data width			N/A			0
15	Min. clock delay, Back to back random column address			1			1
16	Burst length supported			1,2,4,8,Page			8F
17	Number of banks on each SDRAM device			2			2
18	CAS latencies supported			CL=2,3			6
19	CS latency			0			1
20	Write latency			0			1
21	SDRAM module attributes			Non - buffered			0
22	SDRAM device attributes : general			0E			E
23	SDRAM cycle time. CAS latency = 2	10ns	13ns	15ns	A0	D0	F0
24	SDRAM access time from clock. CAS latency = 2	6ns	7ns	8ns	60	70	80
25	SDRAM cycle time. CAS latency = 1			N/A			0
26	SDRAM access time from clock CAS latency = 1			N/A			0
27	Min. row precharge time	20ns	20ns	26ns	14	14	1A
28	Min. row active to row active	20ns	20ns	20ns	14	14	14
29	Min. RAS to CAS delay	20ns	20ns	26ns	14	14	1A
30	Min. RAS pulse width	50ns	50ns	60ns	32	32	3C
31	Module bank density			16Mb			4
32	Command and address singnal input setup time	2ns	2ns	N/A	20	20	FF
33	Command and address singnal input hold time	1ns	1ns	N/A	10	10	FF
34	Data singnal input setup time	2ns	2ns	N/A	20	20	FF
35	Data singnal input hold time	1ns	1ns	N/A	10	10	FF
36 ~ 61	Superset Information			None			FF
62	SPD data revision code	Rev.1.2	Rev.1.2	Rev.1	12	12	1
63	Checksum for bytes 0-62			Checksum data	DC	1C	0D
64	Manufacturer's JEDEC ID code			Continuation code			7F
65	Manufacturer's JEDEC ID code			Vanguard			29
66 - 71	Manufacturer's JEDEC ID code			None			FF

Serial presence detect information (VS26417801C)

Byte	Function described	Function Supported			HEX		
		-8H	-8L	-10	-8H	-8L	-10
72	Manufacturing location	Manufacturing location			-		
73	Manufacturer's part number	V			56		
74	Manufacturer's part number	S			53		
75	Manufacturer's part number	2			32		
76	Manufacturer's part number	6			36		
77	Manufacturer's part number	4			34		
78	Manufacturer's part number	1			31		
79	Manufacturer's part number	7			37		
80	Manufacturer's part number	8			38		
81	Manufacturer's part number	0			30		
82	Manufacturer's part number	1			31		
83	Manufacturer's part number	C			43		
84	Manufacturer's part number	T			54		
85	Manufacturer's part number	G(Gold lead)			47		
86	Manufacturer's part number(PCB revision)	C			43		
87	Manufacturer's part number	"-"			2D		
88	Manufacturer's part number	8	8	1	38	38	31
89	Manufacturer's part number	H	L	0	48	4C	30
90	Manufacturer's part number	Blank			20		
91	Revision code for PCB	C			43		
92	Revision code	Blank			20		
93 ~ 94	Manufacturing date	Year/Week code			-		
95 ~98	Module serial number	Serial number			-		
99 ~ 125	Manufacturer specific data	Manufacturer specific data			FF		
126	Module supports clock frequency	100Mhz	100Mhz	66Mhz	64	64	66
127	Intel specification details	Intel specification details			A6	A4	6
128 ~ 255	For customer use	None			FF		

Serial presence detect information(VS46417801C)

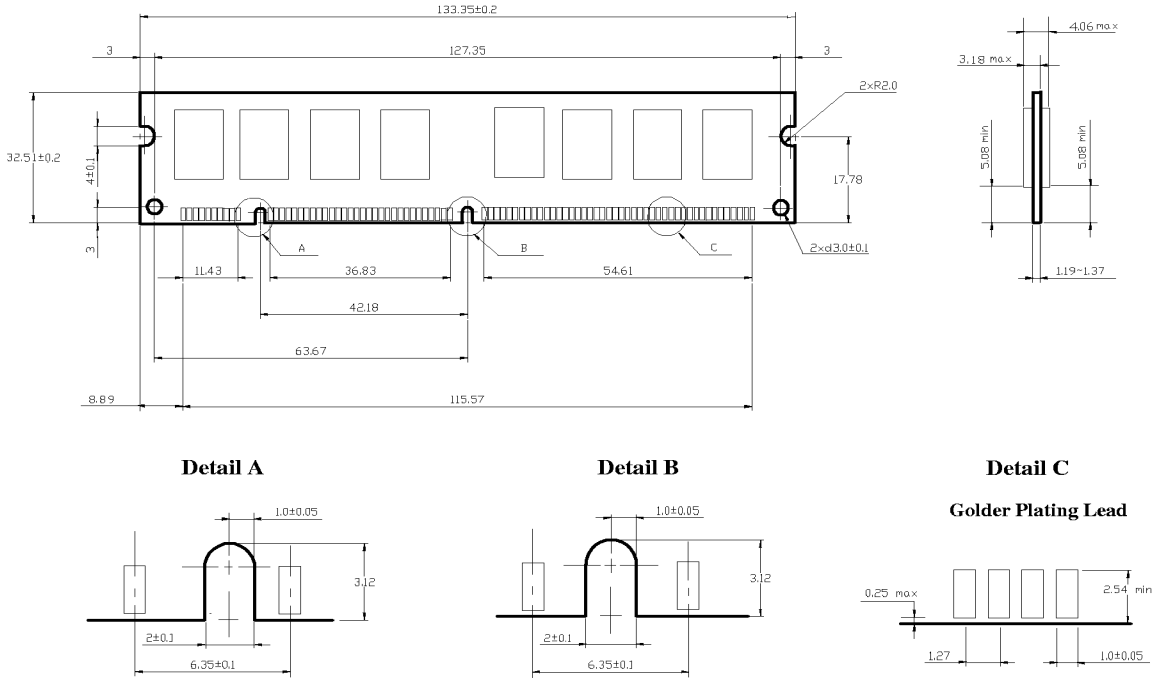
Byte	Function described	Function Supported			HEX		
		-8H	-8L	-10	-8H	-8L	-10
0	Number of bytes used by Vanguard	128			80		
1	Total SPD memory size	256			8		
2	Memory Type	SDRAM			4		
3	Number of Row addresses	11			B		
4	Number of Column addresses	9			9		
5	Number of Banks on module	2			2		
6	Module data width	64			40		
7	Module data width (continued)	0			0		
8	Module voltage interface lelevls	LVTTL			1		
9	SDRAM cycle time. CAS latency = 3	10ns	10ns	10ns	A0	A0	A0
10	SDRAM access from clock. CAS latency = 3	6ns	6ns	8ns	60	60	80
11	Module configuration type	Non - Parity			0		
12	Refresh Rate/Type	15.6us/self			80		
13	SDRAM width, Primary SDRAM	8			8		
14	Error checking SDRAM data width	N/A			0		
15	Min. clock delay, Back to back random column address	1			1		
16	Burst length supported	1,2,4,8,Page			8F		
17	Number of banks on each SDRAM device	2			2		
18	CAS latencies supported	CL=2,3			6		
19	CS latency	0			1		
20	Write latency	0			1		
21	SDRAM module attributes	Non - buffered			0		
22	SDRAM device attributes : general	0E			E		
23	SDRAM cycle time. CAS latency = 2	10ns	13ns	15ns	A0	D0	F0
24	SDRAM access from clock. CAS latency = 2	6ns	7ns	8ns	60	70	80
25	SDRAM cycle time. CAS latency = 1	N/A			0		
26	SDRAM access time from clock CAS latency = 1	N/A			0		
27	Min. row precharge time	20ns	20ns	26ns	14	14	1A
28	Min. row active to row active	20ns			14		
29	Min. RAS to CAS delay	20ns	20ns	26ns	14	14	1A
30	Min. RAS pulse width	50ns	50ns	60ns	32	32	3C
31	Module bank density	16Mb			4		
32	Command and address singnal input setup time	2ns	2ns	N/A	20	20	FF
33	Command and address singnal input hold time	1ns	1ns	N/A	10	10	FF
34	Data singnal input setup time	2ns	2ns	N/A	20	20	FF
35	Data singnal input hold time	1ns	1ns	N/A	10	10	FF
36 ~ 61	Superset Information	None			FF		
62	SPD data revision code	Rev.1.2	Rev.1.2	Rev.1	12	12	1
63	Checksum for bytes 0-62	Checksum data			DD	1D	0E
64	Manufacturer's JEDEC ID code	Continuation code			7F		
65	Manufacturer's JEDEC ID code	Vanguard			29		
66 - 71	Manufacturer's JEDEC ID code	None			FF		

Serial presence detect information (VS46417801C)

Byte	Function described	Function Supported			HEX		
		-8H	-8L	-10	-8H	-8L	-10
72	Manufacturing location	Manufacturing location			-		
73	Manufacturer's part number	V			56		
74	Manufacturer's part number	S			53		
75	Manufacturer's part number	4			34		
76	Manufacturer's part number	6			36		
77	Manufacturer's part number	4			34		
78	Manufacturer's part number	1			31		
79	Manufacturer's part number	7			37		
80	Manufacturer's part number	8			38		
81	Manufacturer's part number	0			30		
82	Manufacturer's part number	1			31		
83	Manufacturer's part number	C			43		
84	Manufacturer's part number	T			54		
85	Manufacturer's part number	G(Gold lead)			47		
86	Manufacturer's part number(PCB revision)	C			43		
87	Manufacturer's part number	"-"			2D		
88	Manufacturer's part number	8	8	1	38	38	31
89	Manufacturer's part number	H	L	0	48	4C	30
90	Manufacturer's part number	Blank			20		
91	Revision code for PCB	C			43		
92	Revision code	Blank			20		
93 ~ 94	Manufacturing date	Year/Week code			-		
95 ~98	Module serial number	Serial number			-		
99 ~ 125	Manufacturer specific data	Manufacturer specific data			FF		
126	Module supports clock frequency	100Mhz	100Mhz	66Mhz	64	64	66
127	Intel specification details	Intel specification details			F6	F4	6
128 ~ 255	For customer use	None			FF		

168 Pin DIMM Mechanical Dimension(Front Side)

UNITS : mm
Tolerances : 0.13 Unless otherwise specified



Detail A

Detail B

Detail C

Golder Plating Lead

Ordering Information

	1	2	3	4	5	6	7	8	9	10
V	X	X	XX	XXXXX	X	X	X	X	X	-XX

V : VIS Product
1 : RAM Family
S : SDRAM DIMM (168pin)
E : DRAM DIMM (168pin)

2 : Memory density (work)
1 : 1M
2 : 2M
4 : 4M

3 : I/O width
32 : X 32
64 : X 64

4 : Operation mode and refresh with different density
17801 : 2K ref.,2M X 8 SDRAM
17161 : 2K ref., 1M X 16 SDRAM

5 : Component revision
Blank : None
A : A revision
B : B revision
C : C revision

6 : Component Package
T : TSOP

7 : PC board finger plating
G : Gold
S : Tin/lead

8 : PC board revision
Blank : none
A : A revision
B : B revision
C : C revision

9 : Customer specific
Blank : none

10 : Module speed
-10 : 100MHz ; PC66, CL=2, t_{RP}=2, t_{RCD}=2
-8L : 100MHz ; PC100,CL=3, t_{RP}=2, t_{RCD}=2
-8H : 100MHz ; PC100,CL=2, t_{RP}=2, t_{RCD}=2