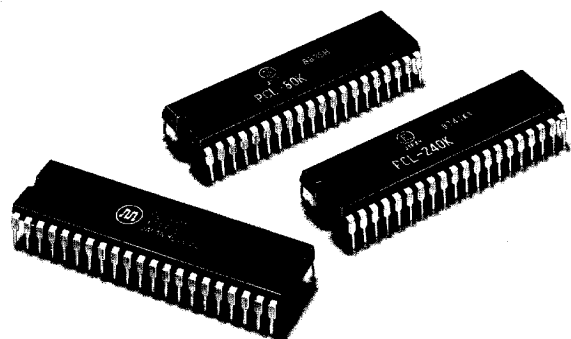# PROGRAMMABLE SINGLE-CHIP HIGH-SPEED PULSE GENERATORS
PCL SERIES

Outline

A variety of inputs and outputs are provided for sophisticated control through software. Three models (PCL-80K, PCL-240K, PCL-3M) with varying degrees of sophistication are offered to enable the system designer to choose the appropriate chip to do the job—no more, no less.

Features:
● Return to home—manually initiated.
● Ramp up/down: available on all the three models, to control the output frequency linearly.
●The PCL-3M chip has the following additional features: input/outputs: alarm and "servo ready" inputs; "servo-on" and deviation counter reset signal outputs; encoder A, B, and Z phase signal inputs; completed position output.
●The PCL-3M also has two multi-purpose counters. The user can utilize the counters for counting functions such as, counting a prevailing position, or measuring the deviation between command and feedback signals. In addition, the PCL-3M chip has a host of other features, some of which are: output interrupt based on a set of conditions, read-out of preset commands and the identification of the frequency output conditions. Detailed technical manuals are available on the PCL-80K, PCL-240K and PCL-3M.

The PCL series are motion control IC's which allow programming of output frequency with an external CPU. In addition, the PLC series are equipped with ramp up/down control which can vary the output frequency linearly.

Specifications

Items Models	PCL-80K	PCL-240K	PCL-3M
Operating Conditions			
Ambient Temperature Range, Ta °C	0~70		
Supply Voltage, VDD V	4.5~5.5	4.75~5.25	
Low Level Input Voltage, VIL V	0~0.8		0~0.8, 1.0
High Level Input Voltage, VIH V	2.0~VDD		2.0, 4.0~VDD
Clock Frequency, fclk Hz	4.9152M		9.8304M
Number of Dip Pins	40		42
Built-in Registers			
Down-Counter	FFFFFF		
Frequency Register 1	1FFF		3FFF
Frequency Register 2	1FFF		3FFF
Frequency Resister 3	1FFF		—
Ramping-up Rate Register	FFF	3FFF	FFFF
Ramping-down Rate Register	FFF	3FFF	—
Ramping-down Point Register	1FFF	FFFFF	FFFFFF
Multiplier Register	3FF		3FFF
Multi-purpose Counter 1	—		FFFFFF
Multi-purpose Counter 2	—		FFFFFF
Multi-purpose Counter Control Register	—		FF (high-place), FFFF (low-place)
Deviation Counter Imposition Register	—		FFFF
Timer Register	—		FFFF
Down-Counter Readout Register	—		Provided
Multi-purpose Counter-1 Read Register	—		Provided
Multi-purpose Counter-2 Read Register	—		Provided
Ramping-down Readout Register	—		Provided
Test Mode Register	—		Provided for internal operation check
Input/Output Signals	EXTP, INS, LT, ZERO, FUP, FDOWN, FKEEP		Input: Encoder's A-, B- and Z-phase signals, alarm signal, and pulse servo signal Output: Servo-on and deviation counter reset signals

## Block Diagram & Pin Assignment—PCL-80K/PCL-240K
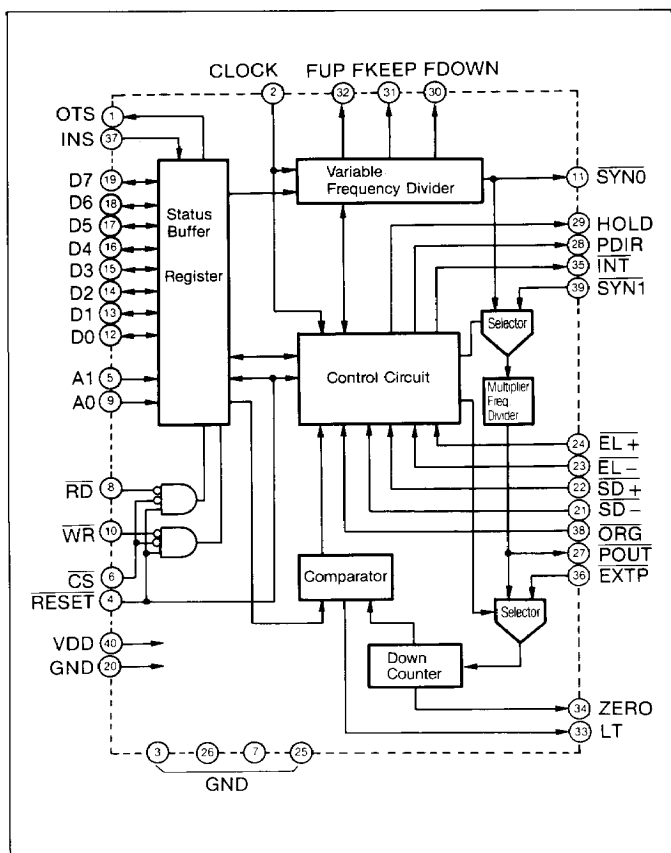
① OTS (Output Signal) ..... Output
It is a multi-purpose output signal and can be controlled through the CPU.

② CLOCK (Clock Signal) ..... Input usually 5MHz)
It is the reference clock for the output pulse. Accuracy of the output pulse does not include that of the reference clock.

④ RESET (Reset Signal) ..... Active low level input
It resets the internal counter and all registers when it is low level.

⑤ A1, ⑨ A0 (Address Bus) ..... Input
They are internal register select signals and usually connected to CPU addresses 1 and 0.

⑥ CS (Chip Select) ..... Active low level input
The low level signal places RD and WR signals in ENABLE condition, thereby making it possible for the CPU to read and write.

⑦, ㉕ (GND) ..... Input
These are test pins of the LSI and usually connected to the ground.

⑧ RD (Read) ..... Active low level input
The low level signal lets the status or counter content be output to the data bus.

⑩ WR (Write) ..... Active low level input.
The level level signal enables the counter and register to write.

⑪ SYNO (Synchro Out) ..... Active low level output
Synchronized clock is output for synchronized operation of multiple units of PCL-80K/PCL-240K.

⑫ D0 to ⑲ to D7 (Data Bus) ..... 3-state input/output
These are dual-direction data bus.

⑳ SD−, ㉒ SD+ (Slew Down) ..... Active low level inputs
When a signal of the same direction as that of output pulse is low level during operation in the high speed mode, the frequency ramps down.
If it is high level after then, the frequency ramps up.

㉓ EL−, ㉔ EL+ (End Limit) ..... Active low level inputs
When a signal of the same direction as that of the PDIR signal is low level during pulse output, pulse output stops immediately. During the low level, pulse cannot be output toward the direction but can be output toward the opposite direction.

㉗ POUT (Pulse Output) ..... Active low level output
It is the pulse output pin. Its duty cycle is approx. 50%.

㉘ PDIR (Pulse Direction) ..... Output
It gives the direction signal of output pulse. When it is low level, the minus direction signal is output.

㉙ HOLD (Hold) ..... Active high level output
It is high level when no pulse is output.

㉚ FDOWN (Frequency Down) ..... Active high level output
It is high level when frequency ramps down during operation in the high speed mode.

㉛ FKEEP (Frequency Keep) ..... Active high level output
It is high level when frequency is not ramping up nor down. It can be read in as a status signal.

㉜ FUP (Frequency Up) ..... Active high level output
It is high level while frequency is ramping up during operation in the high speed mode.

㉝ LT (Little) ..... Active high level output
It is high level when the counter content is smaller than the down-point register value.

㉞ ZERO (Zero) ..... Active high level output
It is high level when the counter content is 0.

㉟ INT (Interrupt Request) ..... Active low level output
It is low level when the output pulse stops. It can be masked by CPU command and read as a status signal.

㊱ EXTP (External Pulse) ..... Active low level input
When operating the counter through an external pulse, input the pulse to this pin. The counter counts the pulse at the edge of rise.

㊲ INS (Input Signal) ..... Input
It is a multi-purpose input and the CPU can read the signal as a status signal.

㊳ ORG (Origin) ..... Active low level input
When it is low level during return to the mechanical origin, pulse output stops immediately. The signal can be read as a status signal.

㊴ SYNI (Synchro In) ..... Active low level input
For synchronized operation, it inputs the synchronized clock.

PROGRAMMABLE SINGLE-CHIP HIGH-SPEED PULSE GENERATORS
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Block Diagram & Pin Assignment—PCL-3M
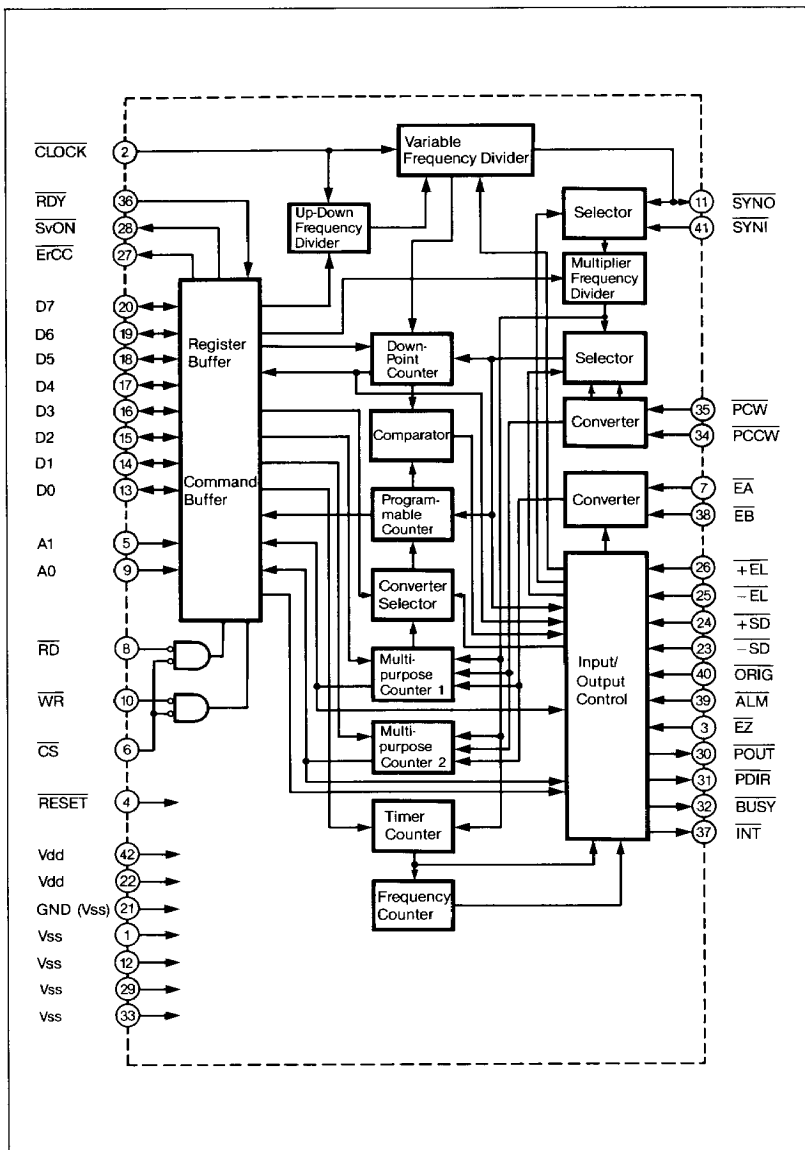
① , ⑫, ㉑, ㉙, ㉝ Vss 0V

② CLOCK (Clock Signal) ..... Input
It is the external reference clock.

③ EZ (Encoder Zero) ..... Input
It is the encoder marker signal.

④ RESET (Reset Signal) ..... Input
It resets all counters and registers.

⑤ A1, ⑨ A0 (Address Signals) ..... Input

⑥ CS (Chip Select) ..... Input

⑦ EA, ㊳ EB (Encoder's Aφ and Bφ Signals) ..... Input

⑧ RD (Read Signal) ..... Input

⑩ WR (Write Signal) ..... Input

⑪ SYNO (Syncho Out) ..... Output
For synchronized operation and interpolation.

⑬ D0 to ⑳ D7 (Data Bus) ..... Input/Output

㉓ −SD (CCW Slew Down) ..... Input
Limit of ramping-down in CCW direction.

㉔ +SD (CW Slew Down) ..... Input
Limit of ramping-down in CW direction.

㉕ −EL (CCW End Limit) ..... Input
End limit in CCW direction.

㉖ +EL (CW End Limit) ..... Input
End limit in CW direction.

㉗ ErCC ..... Output
Multi-purpose output signal.

㉘ SvON (Servo ON) ..... Output
Multi-purpose output signal.

㉚ POUT (Pulse Output) ..... Output
Pulse output or CW pulse output.

㉛ PDIR (Pulse Direction) ..... Output
Pulse direction or CCW pulse output signal.

㉜ BUSY (Busy) ..... Output
Indicates that pulses are being output.

㉞ PCCW (Pulse CCW) ..... Input
External pulse command input signal.

㉟ PCW (Pulse CW) ..... Input
External pulse command input signal.

㊱ RDY (Ready) ..... Input
Multi-purpose input signal.

㊲ INT (Interrupt Request) ..... Output
Operation completeness output signal.

㊳ ALM (Alarm) ..... Input
Stop alarm input signal.

㊵ ORGI (Origin Signal) ..... Input

㊶ SYNI (Synchro In) ..... Input
For synchronized operation.

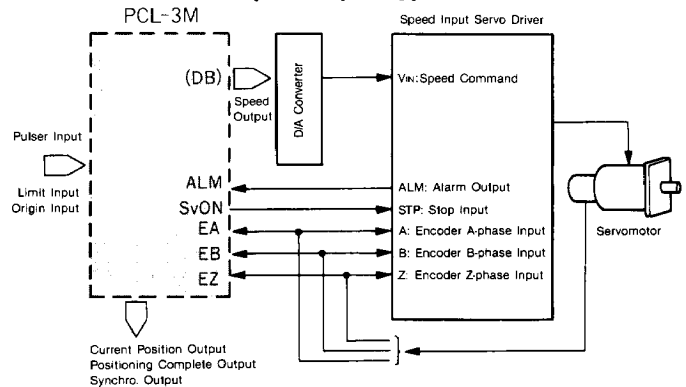㉒, ㊷ VDD 5V

Typical Applications

General Application
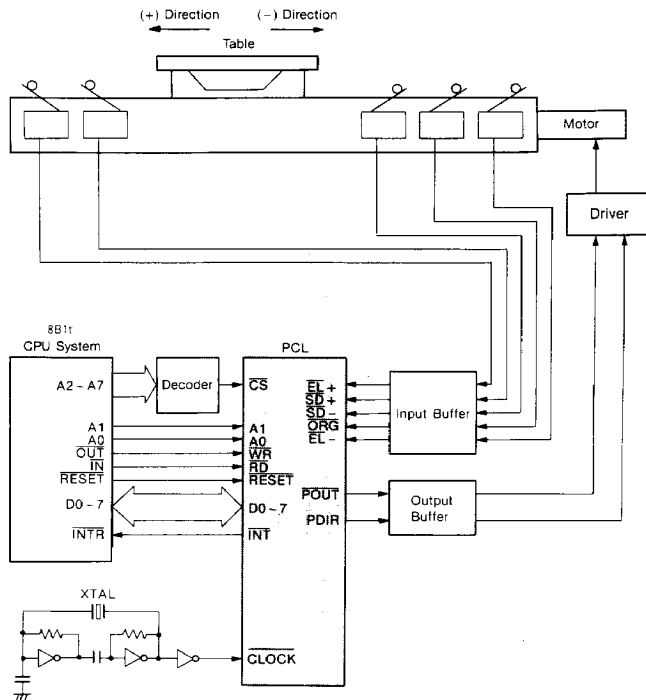
PCL-3M
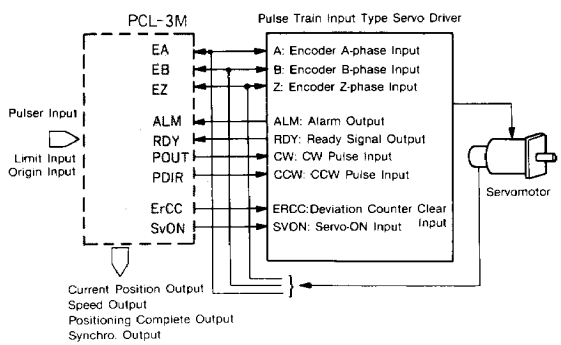#### Block Diagram of Typical Servomotor System
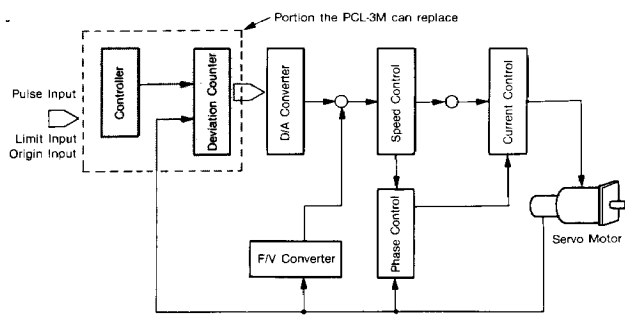
2. Connection to Speed Input Type Servo Driver

CONNECTION EXAMPLES
1. Connection to Pulse Train Input Type Servo Driver

3. Connection to Stepping Motor Driver

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