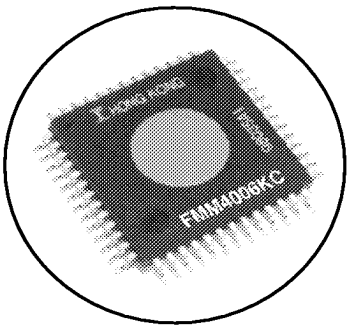
2.5Gb/s GaAs 16:1 Multiplexer IC

FMM4006KC-1

FEATURES



- High Speed Operation up to 2.5Gbps
- Integrated Frequency and Phase Detector
- Low Power Dissipation: 1.1W (Typ)
- Single Power Supply: VEE = -5.2V
- High Speed Differential I/O: 2.5GHz clock inputs and 2.5Gbps Serial Data Outputs
- ECL100K Compatible Parallel data I/O: Single-Ended 155Mbps parallel data inputs and 155MHz divided clock outputs
- Thermally Enhanced, 52-pin **Plastic** Mold Package: KC (14mm), Pin pitch: 1.0mm

DESCRIPTION

The FMM4006 is a STM-16/STS-48 compatible high speed 16:1 multiplexer IC for optical transmission systems and high speed test equipment. The FMM4006 converts 16-bit 155.5Mbps parallel data into 2.485Gbps high speed serial data. Also the FMM4006 has an internal phase frequency detector circuit for external phase lock loop (PLL) configuration.
The FMM4006 is designed with 0.5µm GaAs MESFET technology, and has high-speed performance with low power consumption. The FMM4006 is packaged in an industrial standard thermally enhanced plastic mold package.

ABSOLUTE MAXIMUM RATINGS (Ambient Temperature Ta = 25°C)

Parameter	Symbol	Values	Unit
Supply Voltage	V_{EE}	-7.0 ~ V_{TT}+0.5	V
Output Current	I_{OUT}	-50 ~ +50	mA
Input Voltage	V_{IN}	V_{EE}~+0.5	V
Maximum Input ESD (MIL-STD-883C)	V_{ESD}	1500*1	V
Case Temperature	T_C	-50 ~ +120	°C
Storage Temperature	T_{STG}	-50 ~ +150	°C

Note: (1) Human body model

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FUJITSU

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Values	Unit
Supply Voltage	V_{EE}	-5.2 ±5%	V
Output Termination Voltage	V_{TT}	-2.0	V
Output Termination Resistor	R_T	50	W
Ambient Temperature	T_A	0 ~ +70	°C
Junction Temperature	T_J	0 ~ +100	°C

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS FOR ECL I/O

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Output HIGH Voltage	V_{OHE}	50Ω to -2.0V V_{IH} = V_{IH}(max) or V_{IL}(min)	-1020	-850	-700	mV
Output LOW Voltage	V_{OLE}	50Ω to -2.0V V_{IH} = V_{IH}(max) or V_{IL}(min)	-2000	-	-1620	mV
Input HIGH Voltage	V_{IHE}	–	-1140	-	-650	mV
Input LOW Voltage	V_{ILE}	–	-2050	-	-1520	mV
Input HIGH Current	I_{IHE}	V_{IN}=V_{IH} (max)	-	-	200	µA
Input LOW Current	I_{ILE}	V_{IN}=V_{IL} (max)	-50	-	-	µA

DC CHARACTERISTICS FOR HIGH SPEED INPUT and OUTPUT

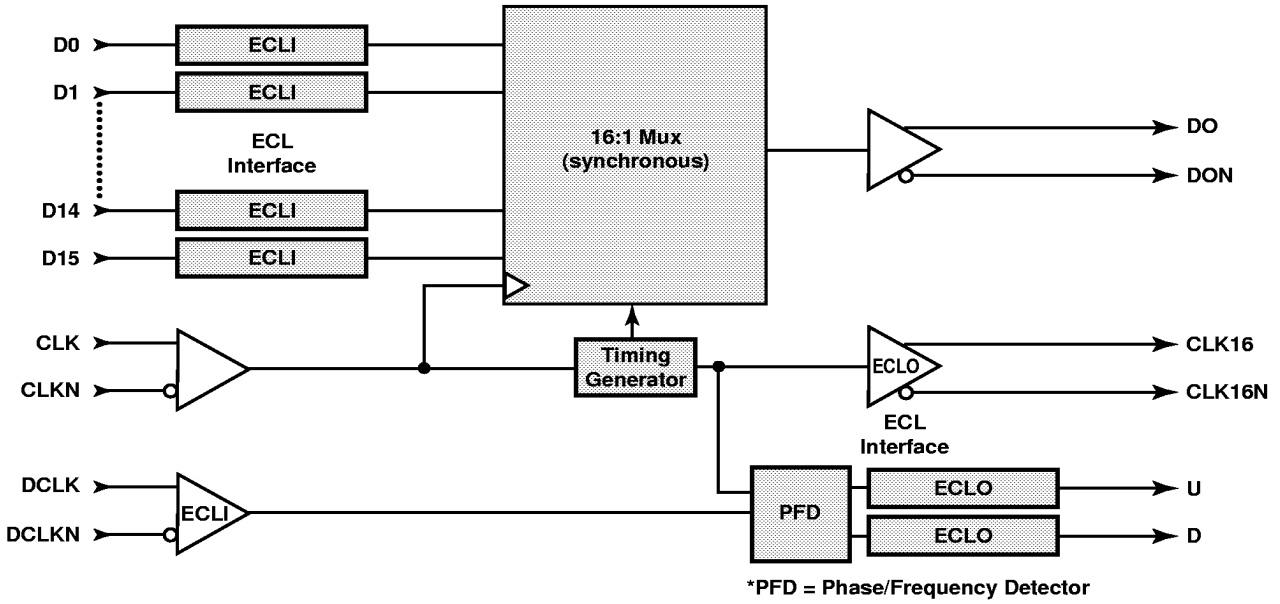
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
DO/DON Output Voltage Swing	V_{OSH}	50Ω to -2.0V 2.48832GHz	700	900	-	mVpp
CLK/CLKN Input Voltage Swing	V_{ISH}	AC-coupled and 2.48832Gbps	600	700	1200	mVpp

POWER DISSIPATION

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Power Dissipation	PD	V_{EE} = -5.46V, Output open	550	1100	1650	mW
		Output: 50Ω to -2.0V Typical Condition	620	1170	1720	mW

AC CHARACTERISTICS (V_{DD}=3.3V, T_A=25°C)

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Max.	Max.	
Maximum Operating Clock Frequency	f_{CLK}	–	2500	-	-	MHz
Setup Time of Parallel Data Inputs	t_{DS}	–	2.0	-	-	nsec
Hold Time of Parallel Data Inputs	t_{DH}	–	0.5	-	-	nsec
Divided Clock Duty Cycle	t_{DC}	–	40	-	60	%
Rise Time of Serial Data	$t_{r\ SDO}$	20% - 80%	-	-	160	psec
Fall Time of Serial Data	$t_{f\ SDO}$	20% - 80%	-	-	160	psec
Rise Time of Parallel Data	$t_{r\ PDI}$	10% - 90%	-	-	2000	psec
Fall Time of Parallel Data	$t_{f\ PDI}$	10% - 90%	-	-	2000	psec
Rise Time of Divided Data	$t_{r\ CKO}$	10% - 90%	-	500	1000	psec
Fall Time of Divided Data	$t_{f\ CKO}$	10% - 90%	-	-	1000	psec
Rise Time of Reference Clock	$t_{r\ DCK}$	10% - 90%	-	-	2000	psec
Fall Time of Reference Clock	$t_{f\ DCK}$	10% - 90%	-	-	2000	psec



16:1 Multiplexer

The 16-bit 155Mbps parallel data (D0)-D-15) is converted to 2.5Gbps serial data (DO/DON). The serial data is output through high speed differential output buffers. The internal synchronous circuits of the FMM4006 are triggered by the falling edge of a high speed clock (CLK).

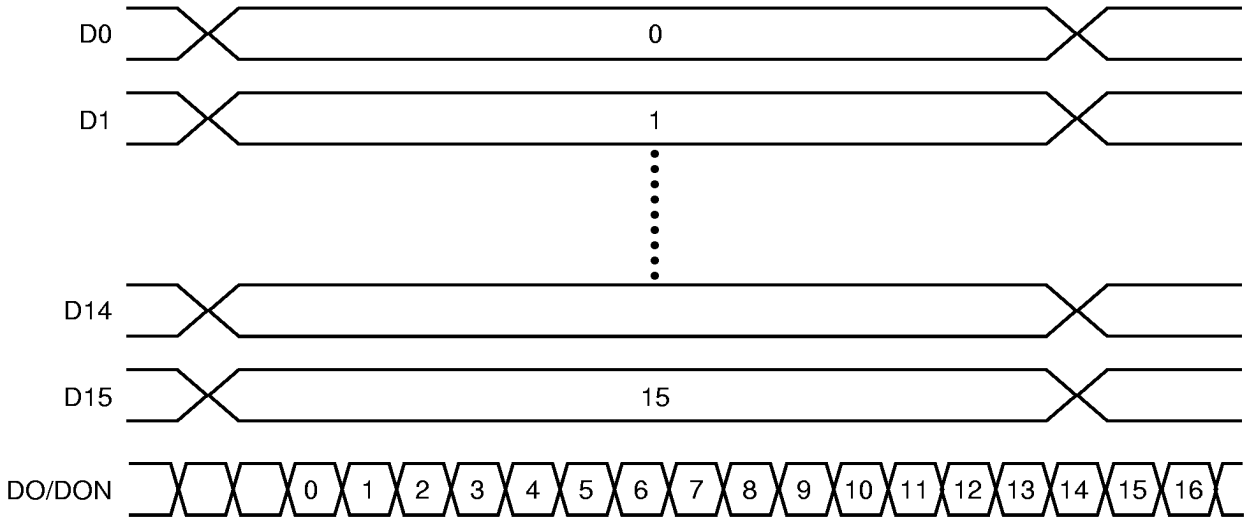


Figure 2: Timing Chart

Timing Generator

The timing generator circuit generates a divide-by-16 clock (CLK16/CLK16N) from the 2.5 GHz high speed clock to synchronize the parallel data and the divided clock. The CLK16 /CLK16N are output through ECL output buffers. The setup and hold time of parallel data

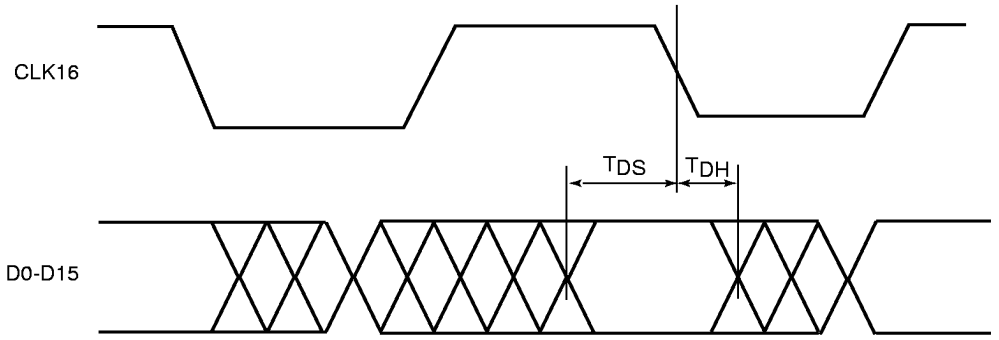


Figure 3: Setup and Hold Time definition for Parallel data

Phase Frequency Detector

The phase frequency detector detects the phase difference between the reference clock (DCLK) and the divide-by-16 clock (CLK16) generated by the timing generator. The outputs are up and down signals (U,D). The phase difference is detected on the rising edges of DCLK and CLK16. When the DCLK phase is prior to CLK16, a pulse signal is output to D for each divide-by-16 clock cycle and no signal to U (low state). When the DCLK phase is behind CLK16, a pulse signal is output to U (no signal to D). After CLK16 phase is locked to DCLK, short pulses are output to both of U and D. The output of the phase frequency detector can be used in a PLL (with external charge pump, low pass filter, and VCO) that connects to the CLCK/CLCKN input.

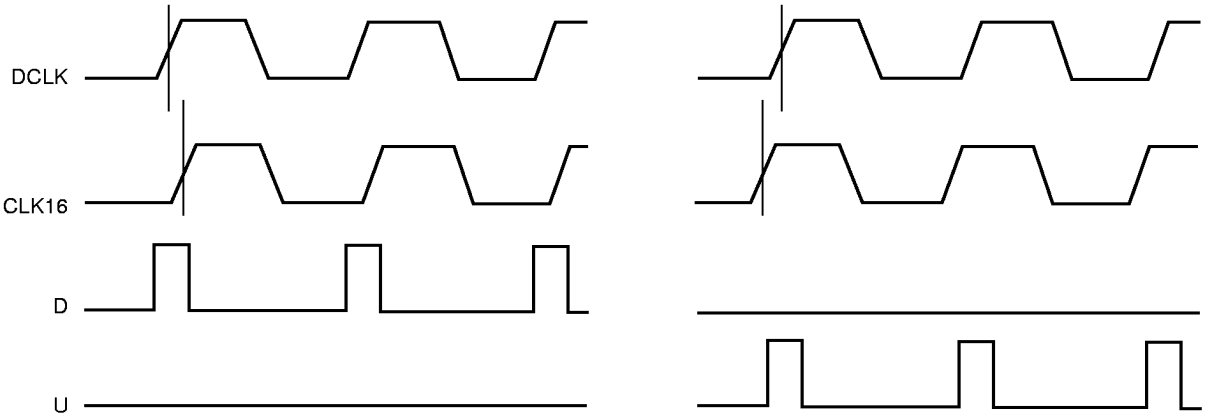
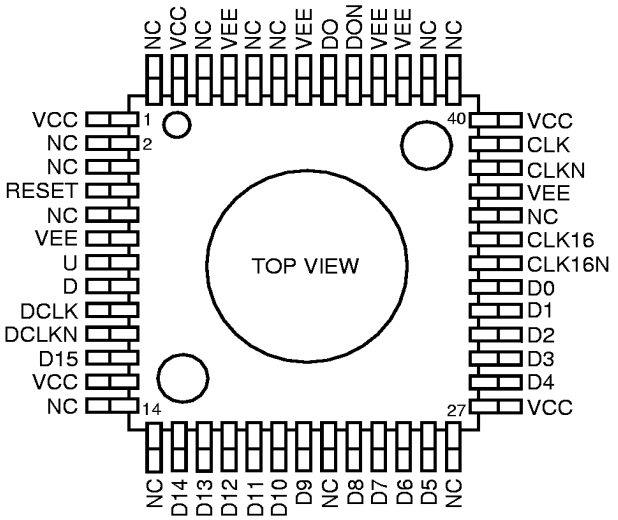


Figure 4: Timing chart for PFD outputs

Package Information

The FMM4006 is packaged in a thermally enhanced plastic mold QFP-52 pin package. The package body size is 14x14mm, and the pin pitch is 1mm.

Figure 5: Package Pin Assignment



NC: No Connection, leave open

Table 1: Pin Description

Pin Name	Pin No.	Type	Description	Pin Name	Pin No.	Type	Description
VCC	1	-	GND (0V)	**VCC**	27	-	GND (0V)
NC	2	-	Open	**D4**	28	ECL:I	Parallel data input
NC	3	-	Open	**D3**	29	ECL:I	Parallel data input
RESET	4	ECL:I	Open or 100K to V_{TT}	**D2**	30	ECL:I	Parallel data input
NC	5	-	Open	**D1**	31	ECL:I	Parallel data input
VEE	6	-	Power (-5.2V)	**D0**	32	ECL:I	Parallel data input
U	7	ECL:O	Up signal	**CLK16N**	33	ECL:O	Divided clock output (n)
D	8	ECL:O	Down signal	**CLK16**	34	ECL:O	Divided clock output (p)
DCLK	9	ECL:I	Ref. Clock (p)	**NC**	35	-	Open
DCLKN	10	ECL:I	Ref. Clock (n)	**VEE**	36	-	Power (-5.2V)
D15	11	ECL:I	Parallel data input	**CLKN**	37	HS:I	Clock input (n)
VCC	12	-	GND (0V)	**CLK**	38	HS:I	Clock input (p)
NC	13	-	Open	**VCC**	39	-	GND (0V)
NC	14	-	Open	**NC**	40	-	Open
D14	15	ECL:I	Parallel data input	**NC**	41	-	Open
D13	16	ECL:I	Parallel data input	**VEE**	42	-	Power (-5.2V)
D12	17	ECL:I	Parallel data input	**VEE**	43	-	Power (-5.2V)
D11	18	ECL:I	Parallel data input	**DON**	44	HS:O	Serial data output (n)
D10	19	ECL:I	Parallel data input	**DO**	45	HS:O	Serial data output (p)
D9	20	ECL:I	Parallel data input	**VEE**	46	-	Power (-5.2V)
NC	21	-	Open or GND	**NC**	47	-	Open
D8	22	ECL:I	Parallel data input	**NC**	48	-	Open
D7	23	ECL:I	Parallel data input	**VEE**	49	-	Power (-5.2V)
D6	24	ECL:I	Parallel data input	**NC**	50	-	Open
D5	25	ECL:I	Parallel data input	**VCC**	51	-	GND (0V)
NC	26	-	Open	**NC**	52	-	Open

AC coupling for high speed inputs

The FMM4006 has two high speed clock inputs (CLK, CLKN). AC coupling is recommended for the high speed inputs. Figure 6 shows a typical configuration for AC coupled differential inputs. Figure 7 shows an example for single-ended inputs.

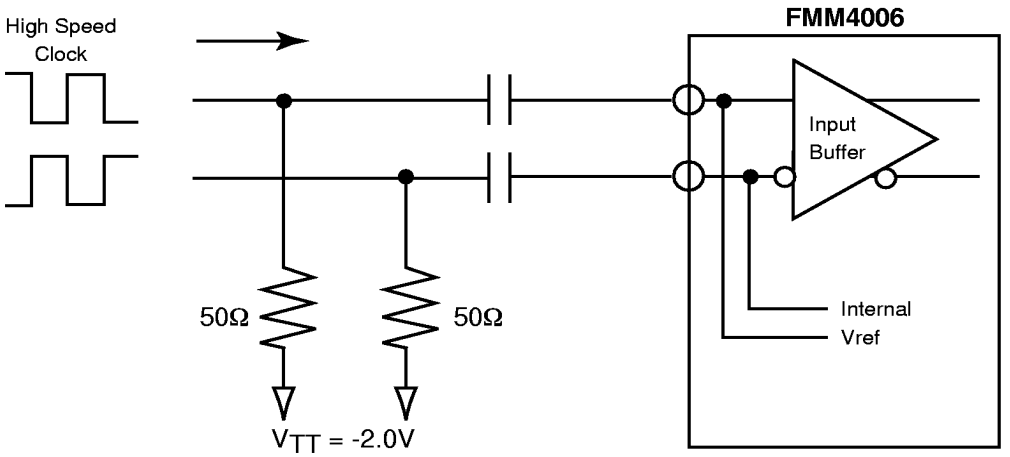


Figure 6: AC coupling for differential high speed inputs

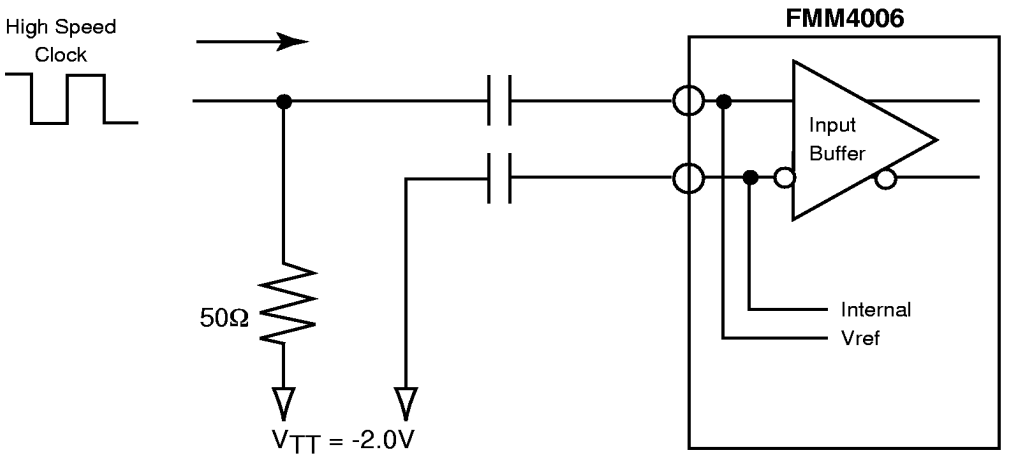
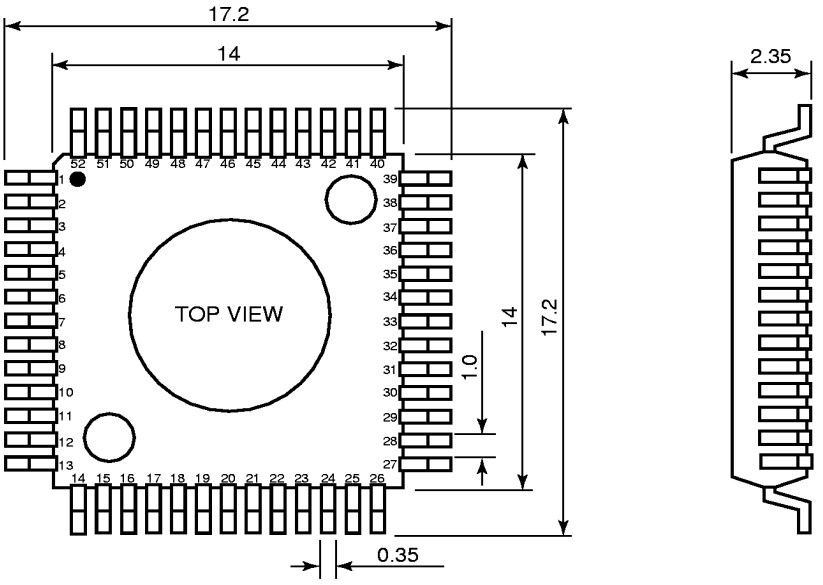


Figure 7: AC coupling for single-ended high speed inputs

Power Supply Circuit

To reduce power supply noise, the bypass capacitors should be used as close as possible to each power supply pin. Ferrite beads are recommended for reducing power supply noise. All bypass capacitors are 0.1µF ceramic chip capacitor.

"KC" PACKAGE **UNIT: mm**



Thermal Resistance of HQFP-52 pin package

		Air flow	0m/s	1m/s	2m/s
Thermal Resistance (Junction to ambient):		θja:	35	26	22°C/W
(Junction to case):		θjc:	2.1°C/W		