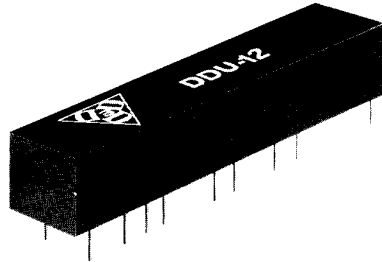


Digital Delay Units

SERIES DDU-12

10 Taps ECL Interfaced



Features:

- Input & Output ECL Buffered
- 10 Equally Spaced Taps
- PC Board Economy Achieved

Specifications:

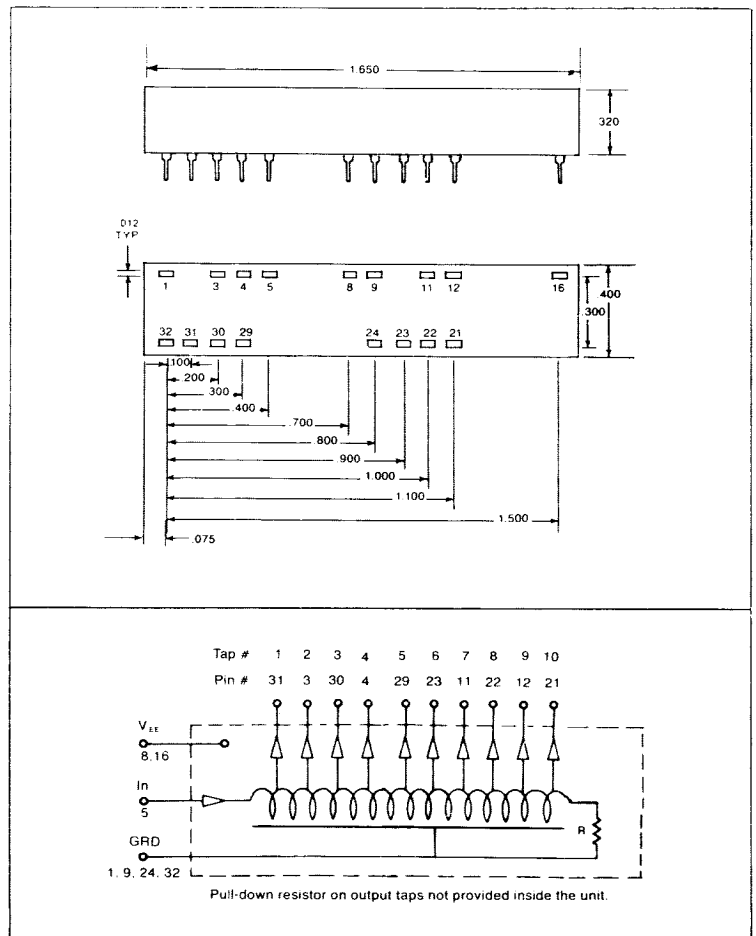
- **Total Delay Tolerance:** $\pm 5\%$ or better, or 2 NS whichever is greater.
- **No. Taps:** 10 equally spaced
- **Rise-Time:** 2 ns typical
- **Logic 1 input voltage:** $-.96V$
- **Logic 1 input current:** .52MA
- **Logic 0 input voltage:** $-1.65 V$
- **Logic 0 input current:** $1.0\mu A$
- **Supply Voltage:** $-5.2V$
- **Operating Temperature:** $-30^{\circ}C$ to $85^{\circ}C$
- **Power Dissipation:** 400 MW typ. (no load)
- **Temperature Coefficient:** 100 PPM/ $^{\circ}C$

Test Conditions:

- Input pulse-width: 150% of total delay.
- Input pulse rise-time: ≤ 6 ns
- Input pulse voltage: $-.7V$
- Rise-time measured from 20% to 80% of leading edge
- Delay time measured at 50% of leading edge.
- All measurements taken @ $V_{EE} = -5.2V$ and $T_A = 25^{\circ}C$
- Unless otherwise specified, all time-delays are referenced to the input pin.

| Part No. | Total Delay NS | Delay Tap NS |
|-------------|----------------|---------------|
| *DDU-12-10 | 9 | 1 \pm .3 |
| *DDU-12-20 | 18 | 2 \pm .4 |
| *DDU-12-25 | 22.5 | 2.5 \pm .4 |
| *DDU-12-40 | 36 | 4 \pm .5 |
| *DDU-12-50 | 45 | 5 \pm 1.0 |
| DDU-12-75 | 75 | 7.5 \pm 1.5 |
| DDU-12-100 | 100 | 10 \pm 2.0 |
| DDU-12-150 | 150 | 15 \pm 2.0 |
| DDU-12-200 | 200 | 20 \pm 2.0 |
| DDU-12-250 | 250 | 25 \pm 2.0 |
| DDU-12-300 | 300 | 30 \pm 2.0 |
| DDU-12-400 | 400 | 40 \pm 2.0 |
| DDU-12-500 | 500 | 50 \pm 2.5 |
| DDU-12-750 | 750 | 75 \pm 4.1 |
| DDU-12-1000 | 1000 | 100 \pm 5.0 |
| DDU-12-1500 | 1500 | 150 \pm 7.0 |

*Time delay measurements referenced to 1st tap.
3.5 NS \pm 1 NS inherent delay.



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