CSC™ CHERRY SEMICONDUCTOR

2, 4, 6-CHANNEL HIGH PERFORMANCE

READ/WRITE CIRCUIT

CS-514/
514R ™

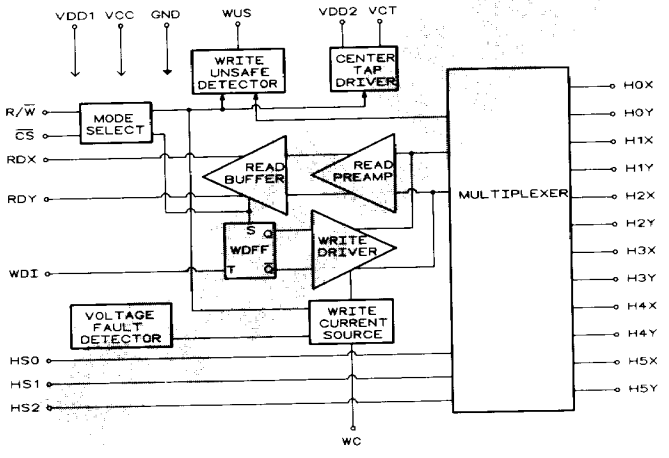
DESCRIPTION

The CS-514/514R Read/Write devices are bipolar monolithic integrated circuits designed for use with center-tapped ferrite recording heads. They provide a low noise read amplifier, write current control and data protection circuitry for as many as six channels. The CS-514R option provides internal 750Ω damping resistors. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. The CS-514 is available in a variety of package and channel configurations.

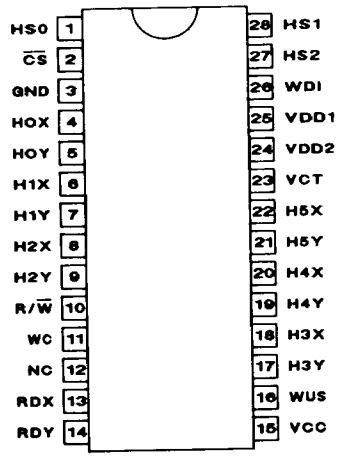
FEATURES:

- High Peformance:
  - -Read mode gain = 150 V/V
  - -Input noise = 1.5 nV/$\sqrt{Hz}$ max.
  - -Input capacitance = 20 pF max.
  - -Write current range = 10 mA to 40 mA
- Enhanced system write to read recovery time
- Power supply fault protection
- Plug compatible to the CS-117 & CS-510A
- Designed for center-tapped ferrite heads
- Programmable write current source
- Write unsafe detection
- TTL compatible control signals
- +5V, +12V power supplies

BLOCK DIAGRAM



PIN CONNECTIONS
28 LEAD SO



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CIRCUIT OPERATION

The CS-514 addresses up to six center-tapped ferrite heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$, and R/$\overline{W}$, as shown in tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$, will force the device into a non-writing condition if either control line is opened accidentally.

TABLE 1: MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 2: HEAD SELECT

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	X	None

0=Low level 1=High level X=Don't care

WRITE MODE

The write mode configures the CS-514 as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI).

The magnitude of the write current (0-pk) is programmed by an external resistor RWC, connected from pin WC to ground and is given by:

$$Iw = \frac{K}{RWC}$$

where K is the Write Current Constant. In multiple device applications, a single RWC resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag.

- Head open
- WDI frequency too low
- Device not selected
- Head center tap open
- Device in Read mode
- No write current

To reduce internal power dissipation, an optional external resistor, RCT, given by RCT≤ 130Ω x 40/Iw (Iw in mA), is connected between pins VDD1 and VDD2. Otherwise connect pin VDD1 to VDD2.

To initialize the Write Data Flip Flop (WDFF) to pass current through the X-side of the head, pin WDI must be low when the previous read mode was commanded.

READ MODE

The read mode configures the CS-514 as a low noise differential amplifier and deactivates the write current generator and write unsafe circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent pulse detection circuitry.

IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector, and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0-HS2	I	Head Select
$\overline{CS}$	I	ChipSelect: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects Read Mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
WDI	I	Write Data In: negative transition toggles direction of head current
H0X-H5X/H0Y-H5Y	I/O	X, Y head connections
RDX, RDY	O*	X, Y Read Data: Differential read signal out
WC	*	Write Current: used to set the magnitude of the write current
VCT	—	Voltage Center Tap: voltage source for head center tap
VCC	—	+5V
VDD1	—	+12V
VDD2	—	Positive power supply for the center-tap voltage source
GND	—	Ground

* When more than one R/W device is used, these signals can be wire OR'ed.

ABSOLUTE MAXIMUM RATINGS (All voltages referenced to GND. Currents into device are positive.)

PARAMETER		VALUE	UNITS
DC Supply Voltage	(VDD1)	-0.3 to +14	VDC
	(VDD2)	-0.3 to +14	VDC
	(VCC)	-0.3 to +6	VDC
Digital Input Voltage Range (VIN)		-0.3 to VCC +0.3	VDC
Head Port Voltage Range (VH)		-0.3 to VDD1 +0.3	VDC
WUS Pin Voltage Range (Vwus)		-0.3 to +14	VDC
Write Current (O-pk)	Iw	60	mA
Output Current	RDX, RDY (Io)	-10	mA
	VCT	-60	mA
	WUS	+12	mA
Storage Temperature Range (Tstg)		-65 to 150	°C
Lead Temperature PDIP (10 sec Soldering)		260	°C
Package Temperature PLCC, SO (20 Sec Reflow)		215	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC Supply Voltage	(VDD1)		10.8	12.0	13.2	VDC
	(VCC)		4.5	5.0	5.5	VDC
Head Inductance (Lh)			5		15	μH
Damping Resistor (RD) (514 Only)			500		2000	ohms
RCT Resistor (RCT)*(¼ Watt)		Iw=40mA	123	130	138	ohms
Write Current (IW)			10		40	mA
Junction Temperature Range (Tj)			+25		+125	°C

* For Iw=40mA, At other Iw levels refer to Applications Information that follows this specification.

DC CHARACTERISTICS: Unless otherwise specified, VDD1=VDD2=12V±10%, VCC=5V±10%, +25°C≤Tj≤+135°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
VCC Supply Current	Read/Idle	Read/Idle Mode			35	mA
	Write	Write Mode			30	mA
VDD Supply Current	Idle	Idle Mode			20	mA
(sum of VDD1 and VDD2)	Read	Read Mode			35	mA
	Write	Write Mode			20+Iw	mA
Power Dissipation		Tj=+125°C				
	Idle	Idle Mode			400	mW
	Read	Read Mode			600	mW
	Write	Write Mode, IW=40mA, RCT=0Ω			800	mW
	Write	Write Mode, IW=40mA, RCT=130Ω			600	mW

DC CHARACTERISTICS (Continued)

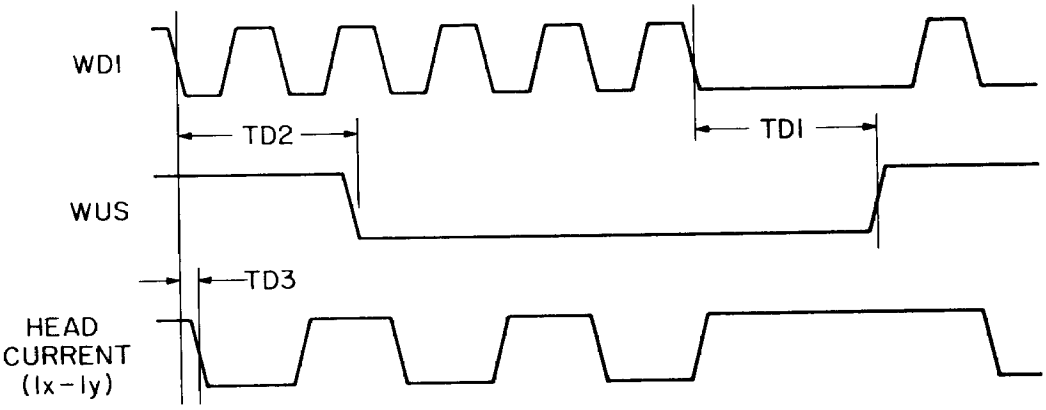
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL I/O					
VIL, Input Low Voltage				0.8	VDC
VIH, Input High Voltage		2.0			VDC
IIL, Input Low Current	VIL=0.8V	-0.4			mA
IIH, Input High Current	VIH=2.0V			100	μA
VOL, WUS Output, Low Voltage	IOL=8mA			0.5	VDC
IOH, WUS Output High current	VOH=5.0V			100	μA
WRITE MODE					
Center Tap Voltage (VCT)	Write Mode		6.7		VDC
Head Current (per side)	Write Mode, 0≤VCC≤3.7V 0≤VDD1≤8.7V	-200		200	μA
Write Current Range		10		40	mA
Write Current Constant "K"		2.375		2.625	
Iwc to Head Current Gain			0.99		mA/mA
Unselected Head Leakage Current				85	μA
RDX, RDY Output Offset Voltage	Write/Idle Mode	-20		+20	mV
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		5.3		VDC
RDX, RDY Leakage	RDX, RDY=6V Write/Idle Mode	-100		100	μA
READ MODE					
Center Tap Voltage	Read Mode		4.0		VDC
Head Current (per side)	Read or Idle Mode 0≤VCC≤5.5V 0≤VDD1≤13.2V	-200		200	μA
Input Bias Current (per side)				45	μA
Output Offset Voltage	Read Mode	-615		+615	mV
Common Mode Output Voltage	Read Mode	4.5		6.5	VDC

DYNAMIC CHARACTERISTICS AND TIMING: Unless otherwise specified, VDD1=VDD2=12V±10%, VCC=5V±10%, +25°C≤Tj≤125°C, IW=35mA, Lh=10μH, Rd=750Ω, f(WDI)=5MHz, CL (RDX, RDY)≤20pF.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
WRITE MODE						
Differential Head Voltage Swing			7.0			V(pk)
Unselected Head Transient Current					2	mA(pk)
Differential Output Capacitance					15	pF
Differential Output Resistance		514	10K			Ω
		514R	600		960	Ω
WDI Transition Frequency	WUS=low		250			KHz
READ MODE						
Differential Voltage Gain	Vin=1mVpp@300kHz ZL(RDX), ZL(RDY)=1KΩ		125		175	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%. Vin=Vi+0.5mVpp@300kHz		-2		+2	mV

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
READ MODE (Cont'd.)					
Bandwidth (-3db)	Zs<5Ω, Vin=1mVpp	30			MHz
Input Noise Voltage	BW=15MHz, Lh=0 Rh=0			1.5	nV/$\sqrt{Hz}$
Differential Input Capacitance	f=5MHz			20	pF
Differential Input Resistance	f=5MHz 514	3.2K			Ω
	514R	500		1000	Ω
Common Mode Rejection Ratio	Vcm=VCT+100mVpp @5MHz	50			db
Power Supply Rejection Ratio	100mVpp @ 5MHz on VDD1, VDD2, or VCC	45			db
Channel Separation	Unselected Channels: Vin=100mVpp@ 5MHz & Selected Channel: Vin=0mVpp	45			db
Single Ended Output Resistance	f=5MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	±2.1			mA
SWITCHING CHARACTERISTICS					
R/$\overline{W}$ to Write	Delay to 90% of Write Current			1.0	μS
R/$\overline{W}$ to Read	Delay to 90% of 100mV, 10MHz Read Signal Envelope or to 90% decay of Write Current			1.0	μS
$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100mV 10MHz Read Signal Envelope			1.0	μS
$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current			1.0	μS
HS0-HS2 to any Head	Delay to 90% of 100mV 10MHz Read Signal Envelope			1.0	μS
WUS: Safe to Unsafe-TD1	Iw=35mA	1.6		8.0	μS
Unsafe to Safe-TD2				1.0	μS
Head Current Lh=0μH, Rh=0Ω					
Prop. Delay-TD3	From 50% Points			25	nS
Assymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall Time			2	nS
Rise/Fall Time	10%-90% Points			20	nS



WRITE MODE TIMING DIAGRAM

APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representaive of actual performance.

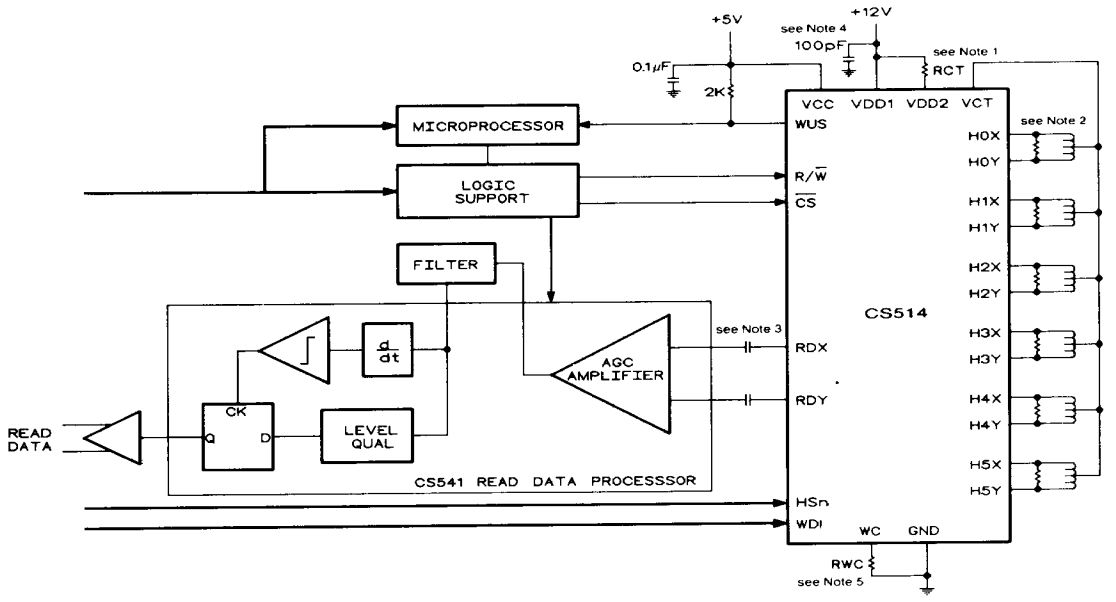
TABLE 3: KEY PARAMETERS UNDER WORST CASE INPUT NOISE CONDITIONS

PARAMETER		Tj=25°C	Tj=135°C	UNITS
Inputs Noise Voltage (max.)		1.1	1.5	nV/√Hz
Differential Input Resistance (min.)	514R	850	1000	Ω
	514	15.4	29.4	KΩ
Differential Input Capacitance (max.)		11.6	10.8	pF

TABLE 4: KEY PARAMETERS UNDER WORST CASE INPUT IMPEDANCE CONDITIONS

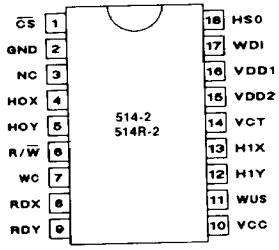
PARAMETER		Tj=25°C	Tj=135°C	UNITS
Inputs Noise Voltage (max.)		0.92	1.2	nV/√Hz
Differential Input Resistance (min.)	514R	500	620	Ω
	514	3.2	6.1	KΩ
Differential Input Capacitance (max.)		10.1	10.3	pF

APPLICATIONS INFORMATION (continued)

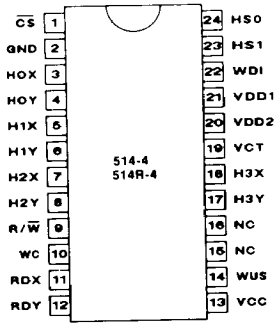


NOTES:
1. An external resistor, RCT, given by; RCT≤130 (40/Iw) where Iw is the zero peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. Damping resistors not required on CS-514R versions.
3. Limit DC current from RDX and RDY to 100 μA and load capacitance to 20pF. In multi-chip application these outputs can be wire-or'd.
4. The power bypassing capacitor must be located close to the device with its ground returned directly to device ground, with as short a path as possible.
5. To reduce ringing due to stray capacitance this resistor should be located close to the device. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

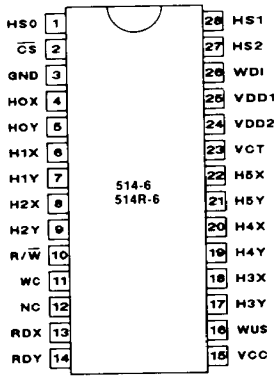
PIN CONNECTIONS



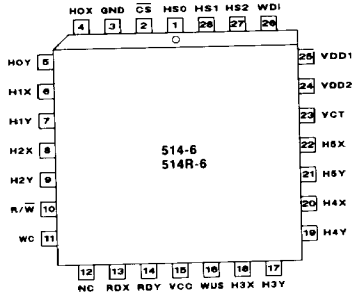
18-LEAD SO



24-LEAD SO



28-LEAD SO



28-LEAD PLCC

THERMAL CHARACTERISTICS

PACKAGE		Øja
18-LEAD	SO	100°C/W
24-LEAD	SO	85°C/W
28-LEAD	SO	80°C/W
28-LEAD	PLCC	65°C/W

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
CS-514-2DW	18 lead SO
CS-514-4DW	24 lead SO
CS-514-6DW	28 lead SO
CS-514-6FN	28 lead PLCC
with internal damping resistors	
CS-514-2RDW	18 lead SO
CS-514-4RDW	24 lead SO
CS-514-6RDW	28 lead SO
CS-514-6RFN	28 lead PLCC

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