CAT5412

Preliminary

12-BIT, 2MHz SELF-CALIBRATING A/D CONVERTER

DESCRIPTION

The CAT5412 is a 12-bit BiMOS A/D converter utilizing a self-calibration technique and digital error correction. This self-calibration circuitry ensures 12-bit accuracy over operating life and temperature range of the device, eliminating any manual calibration requirements.

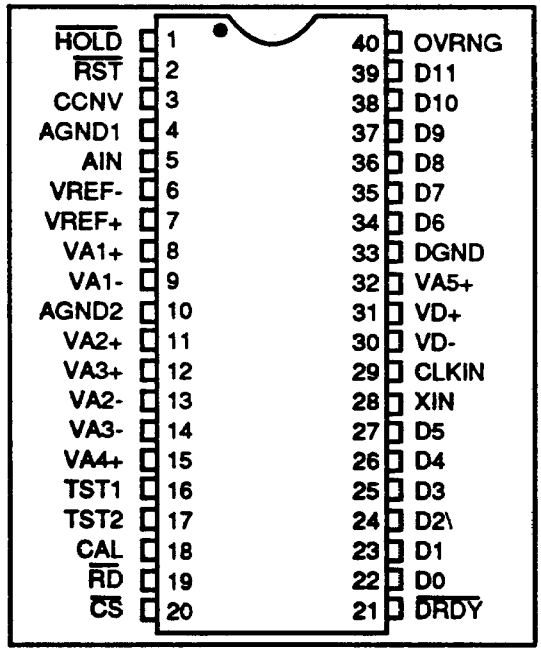
The high throughput is achieved by using a 2-step flash A/D conversion technique in addition to two track-and-hold amplifiers.

The CAT5412 uses an advanced BiMOS process which provides both low power consumption (700mW) and an increased reliability inherent to monolithic devices.

FEATURES

- Resolution: 12 bits
- Maximum non-linearity: 1/2 LSB
- Throughput rates to 2MHz
- Total harmonic distortion: 0.02%
- Dynamic range: 72dB
- No missing codes to 12 bits
- Self-calibrating for accuracy over time and temperature
- Fast recovery from input overdrive
- Low power dissipation: 700mW
- Monolithic BiMOS sampling ADC
  - on chip track-and-hold amplifier
  - microprocessor interface

PIN CONFIGURATION



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PIN DESCRIPTIONS

Power Supply Connections

VD+: Positive Digital Power, PIN 31
Positive digital supply voltage. Nominally +5V.

VD-: Negative Digital Power, PIN 30
Negative digital supply voltage. Nominally -5V.

DGND: Digital Ground, PIN 33
Digital ground reference.

VA+: Positive Analog Power, PINS 8,11, 12,15,32
Positive analog supply voltage. Nominally +5V.

VA-: Negative Analog Power, PINS 9,13,14
Negative analog supply voltage. Nominally -5V.

AGND: Analog Ground, PIN 4,10
Analog ground reference.

Oscillator

CLKIN; XIN: Clock In, PIN 29; Crystal In, PIN 28
Used to generate the internal master clock. A crystal can be tied across the two pins or an external CMOS-compatible clock can be driven into CLKIN if XIN is left floating.

Digital Inputs

$\overline{\text{HOLD}}$: Hold Input, PIN 1
A negative transition on $\overline{\text{HOLD}}$ puts the track-and-hold amplifier into the hold state and initiates the conversion sequence. Conversions must be synchronized with the master clock at $f_{CLK}/8N$ where N=1,2,3. The $\overline{\text{HOLD}}$ input is CMOS-compatible.

CCNV: Continuous Convert, PIN 3
When held high with the $\overline{\text{HOLD}}$ input high or low, throughput will proceed at 1/8th the master clock frequency.

$\overline{\text{CS}}$: Chip Select, PIN 20
Activates the $\overline{\text{RD}}$ and CAL inputs. When $\overline{\text{CS}}$ is high, these inputs have no effect and the data bus (D0 through D11) is held in a high impedance state.

$\overline{\text{RD}}$: Read, PIN 29
When held low with $\overline{\text{CS}}$ also low, enables D0-D11.

$\overline{\text{RST}}$: Reset, PIN 2
When taken low, all internal logic is reset to its cleared or default state. When brought high again a full calibration results. The CAT5412 will not operate while $\overline{\text{RST}}$ is low nor during the resulting full calibration cycle.

CAL: Calibrate, PIN 18
Same as $\overline{\text{RST}}$, but logically inverted and enabled by $\overline{\text{CS}}$.

Analog Inputs

VREF+: Positive Voltage Reference, PIN 7
Represents positive full scale voltage. Typically +1.5V with respect to AGND (bipolar system) or +3V with respect to AGND and VREF- (unipolar system).

VREF-: Negative Voltage Reference, PIN 6
Represents negative full scale voltage. typically -1.5V with respect to AGND (bipolar system) or tied to AGND (unipolar system).

AIN: Analog Input, PIN 5
Analog input to the track-and-hold amplifier.

Digital Outputs

OVRNG: Overrange, PIN 40
Goes high if the sampled analog input voltage exceeds VREF+ or VREF-. OVRNG also goes high during reset and calibration cycles and can therefore be used to indicate end of calibration.

$\overline{\text{DRDY}}$: Data Ready, PIN 21
Falls when new data is becoming available at the outputs. Returns high three master clock cycles later.

PIN CONFIGURATIONS, continued

Digital Input/Outputs

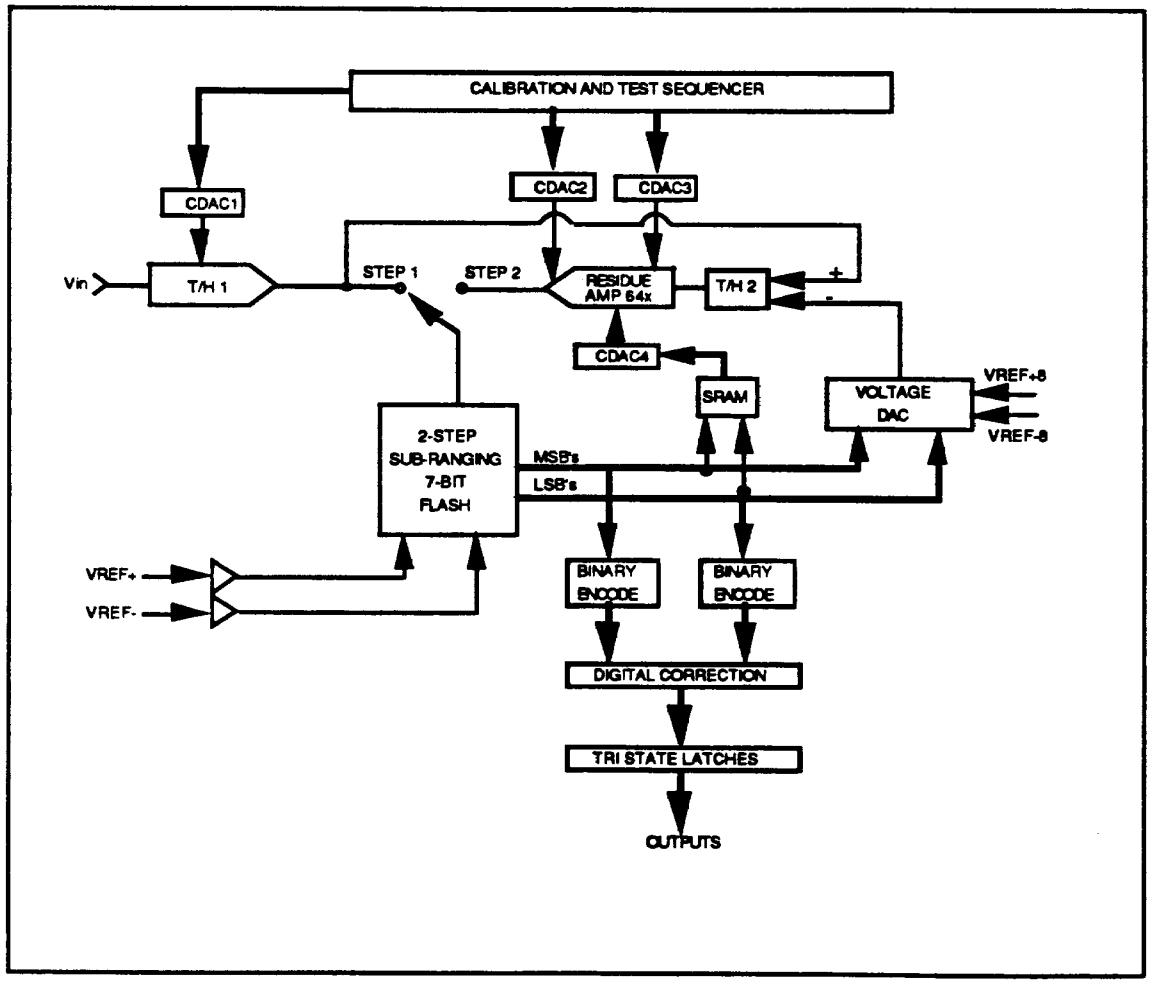
D0 through D11: Data Bus, PINS 22 through 27, 34 through 39
Three-state data bus.

Miscellaneous Pins

TST1: Test, PIN 16
Reserved for factory use. Must be tied to DGND for proper device operation.

TST2: Test, PIN 17
Reserved for factory use. Must be tied to DGND for proper device operation.

BLOCK DIAGRAM



APPLICATIONS

- High Speed Measurement Systems
- Board Level DAS for Computers
- Automatic Test Equipment
- Analytic and Medical Instruments
- Signal Processing
- Vibration Analysis
- Image Enhancement Systems
- Radar Systems
- Digital Oscilloscopes
- Electro-Optics Systems
- Computer Aided Tomography and Magnetic Resonance Systems

THEORY OF OPERATION

To achieve high speed and high accuracy, the CAT5412 implements a standard 2-step flash A/D conversion using self-calibration and digital error correction. Throughput is further maximized by the addition of a second T/H. This allows the next input to be acquired while the previous sample is being converted.

DIGITAL ERROR CORRECTION

The use of digital correction decreases the conversion time because the flash converter comparators do not need to be auto-zeroed. This time savings is significant because the auto-zero offset voltage must be allowed to settle to 12 bits of accuracy. Other advantages obtained by not auto-zeroing include less dynamic noise on the ladder, simpler clock timing and fast recovery from input overload.

The digital error correction is capable of correcting comparator errors from the first flash conversion step. These errors can be as large as 1/128 of full scale. The first flash provides the top seven MSB's. The second flash step provides the bottom six bits. The one bit of overlap is used to correct the errors in the seventh MSB that might have occurred during the first flash ADC.

Flash step #1	1	0	1	0	1	0	1					
Flash step #2							0	1	0	1	0	1
Resulting Code	1	0	1	0	1	0	1	0	0	1	0	1
Bit Position	12	11	10	9	8	7	6	5	4	3	2	1

2-STEP A/D CONVERSION

A/D conversion speed is optimized by using a single step flash technique where an N-bit conversion compares the analog input signal to 2^{n-1} graduated voltage levels. The correct binary output is generated by processing and encoding the 2^{n-1} comparator outputs. One drawback to this approach is that for each additional bit of resolution the number, as well as the accuracy requirement of the comparator doubles. This limitation makes single step flash converters impractical for resolution greater than 8- or 10-bits.

The 2-step technique that the CAT5412 uses employs slightly more complex sub-circuit blocks to achieve high resolution and results in negligible speed degradation. As shown in the block diagram, the CAT5412 consists of two track-and-hold amplifiers, a 7-bit flash ADC, a 7-bit DAC (the resistor ladder), and a residue amplifier. When the command is issued, T/H-1 holds the analog input signal and the flash ADC does a 7-bit conversion to determine the seven MSB's. The MSB's, once decoded are latched into the digital error correction logic. The flash converter's outputs are also loaded into the DAC. The DAC voltage is then subtracted from the analog input and the difference is multiplied to create the input for the second flash conversion. The six bits of data from the second flash conversion and the seven bits from the first flash conversion are used by the digital correction to calculate a 12-bit accurate result.

ANALOG CHARACTERISTICS (T_A = 25°C (Note 1); All VA+ pins, VD+ = 5V; All VA- pins, VD- = -5V; VREF- = -1.5V; f_{CLK} =16MHz for -1, 8MHz for -2; 100kHz Full Scale Input Sinewave; Continuous Convert Mode unless otherwise specified.)

Parameter		CAT5412-C min	CAT5412-C typ	CAT5412-C max	CAT5412-I min	CAT5412-I typ	CAT5412-I max	CAT5412-M min	CAT5412-M typ	CAT5412-M max	Units
Resolution		12			12			12			Bits
Specified Temperature Range		0 to 70			-40 to +85			-55 to +125			°C
Dynamic Performance											
Peak Harmonic or Spurious Noise											
25°C	-J	74	76		74	76		74	76		dB
	-K	77	79		77	79		77	79		
100kHz Input											
T_{min} to T_{max} (Note 1)	-J	TBD	75		TBD	75		TBD	75		
	-K	TBD	75		TBD	75		TBD	75		
490kHz Input	-J		72			72			72		
	-K		72			72			72		
Total Harmonic Distortion	-J		0.02			0.02			0.02		%
	-K		0.02			0.02			0.02		
Signal-to-(Noise plus Distortion)											
25°C	-J	65	67		65	67		65	67		dB
	-K	68	70		68	70		68	70		
0dB Input (Full Scale)											
T_{min} to T_{max} (Note 1)	-J	TBD	67		TBD	67		TBD	67		
	-K	TBD	70		TBD	70		TBD	70		
-40dB Input	-J		32			32			32		
	-K		32			32			32		
dc Accuracy											
Linearity Error (Note 1)											LSB
-J T_{min} to T_{max}			±1	±2.5		±1	±2.5		±1	TBD	
-K T_{min} to T_{max}			±3/4	±1.5		±3/4	TBD		±3/4	TBD	
Differential Linearity		No Missing Codes Guaranteed									LSB
-J T_{min} to T_{max}											
-K T_{min} to T_{max} (Note 1)				±0.9			±0.9			TBD	
Full Scale Error T_{min} to T_{max}			±1/2			±1.5			±3		LSB
Offset Error			±1/2			±1/2			±2		LSB

Notes: 1. All Tmin to Tmax specifications apply after calibration at the temperature of interest. Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

ANALOG CHARACTERISTICS (continued)

Parameter	CAT5412 min	CAT5412 typ	CAT5412 max	CAT5412I min	CAT5412I typ	CAT5412I max	CAT5412M min	CAT5412M typ	CAT5412M max	Units
Analog Input										
Aperture Time		35			35			35		nS
Aperture Jitter		50			50			50		ps,rms
Input Bandwidth (Note 3) Small Signal, -3dB Full Power, -3dB		4 3			4 3			4 3		MHz
Analog Input Impedance at dc		10			10			10		MΩ
Input Capacitance VREF-pin AIN, VREF+ pins		50 10			50 10			50 10		pF
Conversion and Throughput										
Conversion Time -1 (Notes 5,6) -2		625 1.25	688 1.375		625 1.25	688 1.375		625 1.25	688 1.375	nS µS
Throughput Rate -1 (Note 6) -2		2 1			2 1			2 1		MHz
Acquisition Time		300			300			300		nS
Power Supplies										
Power Supply Current (Note 8) I_{A+} I_{A-} I_{D+} I_{D-}		 70 -70 5 -5	 90 -90 10 -10		 70 -70 5 -5	 90 -90 10 -10		 70 -70 5 -5	 90 -90 10 -10	mA
Power Dissipation (Note 8)		750	1000		750	1000		750	1000	mW
Power Supply Rejection Positive Supplies Negative Supplies		50 50			50 50			50 50		dB

Notes:
3. Input 40dB below full scale.
4. Measured from falling transition on $\overline{\text{HOLD}}$ to falling transition on $\overline{\text{DRDY}}$.
5. Applies for conversions triggered externally. In Continuous Convert mode throughput proceeds at one-eighth the master clock frequency with a fixed 10 clock cycle conversion time at full throughput.
6. All outputs unloaded. All inputs CMOS levels.

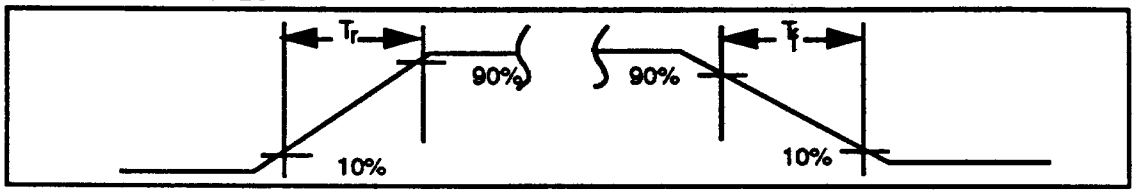
SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; All VA+ pins, VD+ = 5V ± 5%; All VA- pins, VD- = 5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF.)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency: -1 -2	f_{CLK}	 3 3	 - -	 16 8	MHz
Master Clock Duty Cycle	-	40	-	60	%
Rise Times: Any Digital Input (Note 7) Any Digital Output	t_{rise}	- -	- 20	1.0 -	µS nS
Fall Times: (Note 7) Any Digital Input Any Digital Output	t_{fall}	- -	- 20	1.0 -	µS nS
$\overline{HOLD}$, CLKIN Relationship State 7 to $\overline{HOLD}$ Low $\overline{HOLD}$ Low to State 0 State 0 to $\overline{HOLD}$ High $\overline{HOLD}$ High to State 7	 t_{ha} t_{hb} t_{hc} t_{hd}	 62.5 0.0 75 30	 - - - -	 - - - -	 nS
Conversion Time (Note 8)	t_c	10	-	11	MCC*
$\overline{DRDY}$ Pulse Width	t_{dpw}	-	3	-	MCC*
Data Delay Time	t_{dd}	-	40	TBD	nS
Access Times: $\overline{CS}$ Low to Data Valid (Note 9) $\overline{RD}$ Low to Data Valid	t_{csa} t_{rda}	- -	90 90	90 90	nS
Output Float Delay $\overline{CS}$ or $\overline{RD}$ High to Output High-Z	t_{fd}	-	50	TBD	nS
Hold Times: $\overline{CS}$ High to CAL Invalid (Note 10)	t_{ch}	TBD	20	-	nS
Cal Pulse Width: CAL & $\overline{CS}$ Low	t_{csh}	2	-	-	MCC*
$\overline{RST}$ Pulse Width	t_{rpw}	2	-	-	MCC*

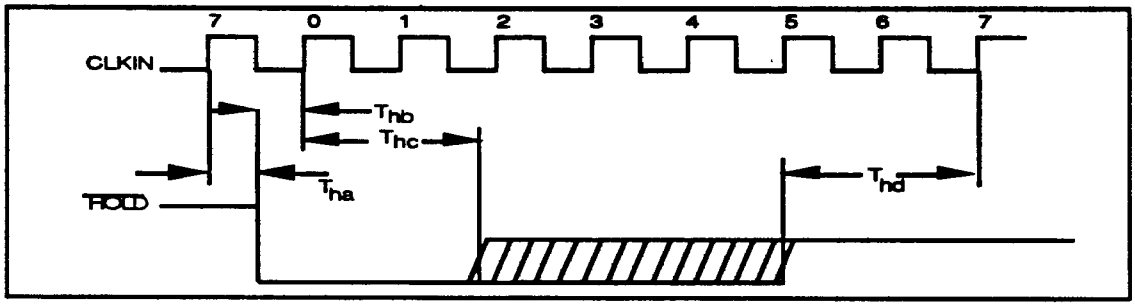
Notes:
7. $\overline{HOLD}$ and CLKIN should be driven with signals which have rise and fall times of at least 25ns.
8. Conversion time in the Continuous Convert mode is a fixed 10 clock cycles.
9. Data goes valid when both $\overline{CS}$ and $\overline{RD}$ are low simultaneously. Each access time assumes the other control input is already low or falls concurrently.
10. If CAL is brought low while $\overline{CS}$ is low, a calibration cycle will be initiated.

*MCC = Master Clock Cycles

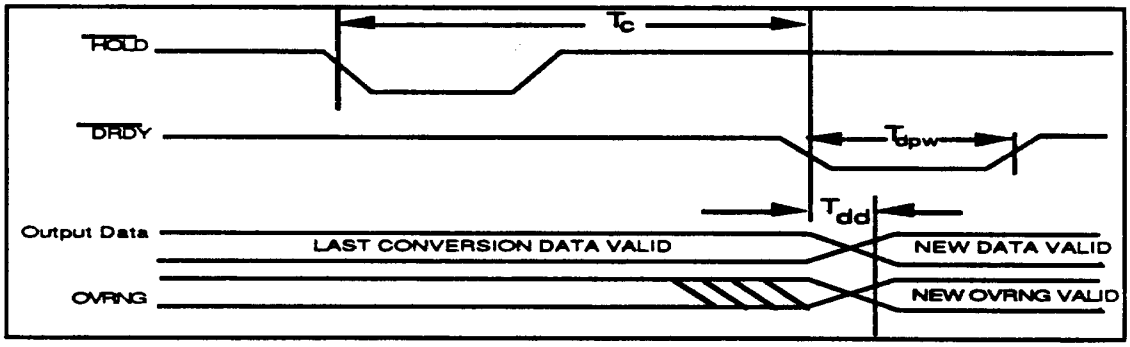
RISE AND FALL TIMES



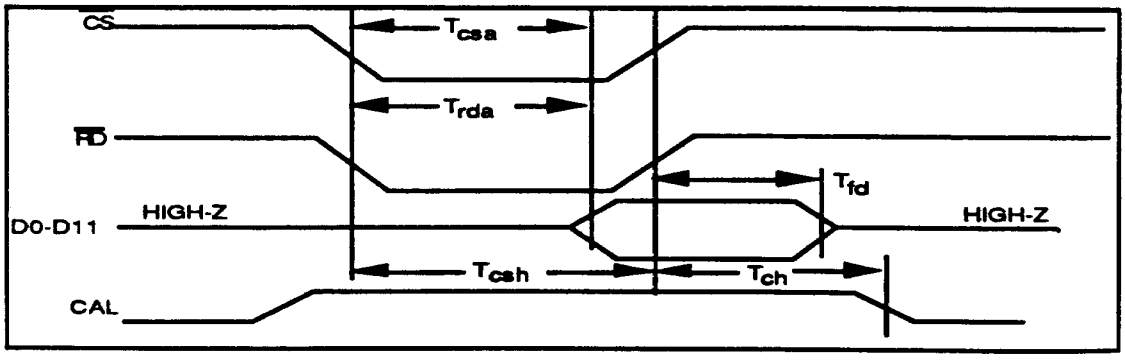
HOLD/MASTER CLOCK PHASE RELATIONSHIP



CONVERSION TIMING



READ AND CALIBRATION CONTROL TIMING



DIGITAL CHARACTERISTICS (TA = Tmin to Tmax; All VA+ pins, VD+ = 5V ±5%; All VA- pins, VD- = -5V±5%.) All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Note 12)	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Note 12)	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 13)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage I_{out} = 1.6MA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-10	-	+10	µA
3-State Leakage Current	I_{OZ}	-10	-	+10	µA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Notes: 12. All pins except $\overline{HOLD}$ and CLKIN which accept only CMOS-compatible inputs (V_{IL} = 0.5V and V_{IH} = VD+ - 0.5V).

13. I_{out} = -100µA. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{out} = -40µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 14.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies	Positive Digital	VD+	4.75	5.0	VA2+, VA5+	V
	Negative Digital	VD-	-4.75	-5.0	-5.25	V
	Positive Analog	VA1+ - VA5+	4.75	5.0	5.25	V
	Negative Analog	VA1- - VA3-	-4.75	-5.0	-5.25	V
Analog Input Voltage		V_{AIN}	VREF-	-	VREF+	V
Analog Reference Voltages						
	Unipolar Input Range	VREF+	2.0	-	3.0	V
		VREF-	-	AGND	-	V
	Bipolar Input Range	VREF+	1.0	-	1.5	V
		VREF-	-1.0	-	-1.5	V

Notes: 14. All voltages with respect to ground.

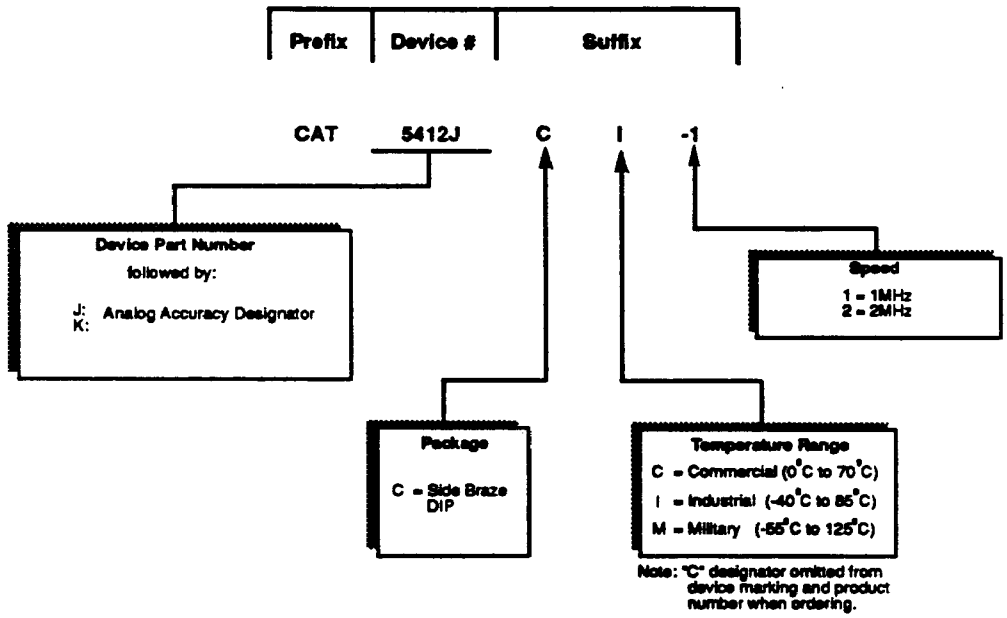
ABSOLUTE MAXIMUM RATINGS (A_{GND}, D_{GND} = 0V, all voltage with respect to ground.

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	-0.3	VA2+,VA5+ +0.3	V
	Negative Digital	VD-	0.3	-6.0	V
(Note 15)	Positive Analog	VA1+ - VA5+	-0.3	6.0	V
	Negative Analog	VA1- - Va3-	0.3	-6.0	V
Input Current, Anyu Pin Except Supplies (Note 16		I_{in}	-	+10	mA
Analog Input Voltage (AIN and VREF pins)		V_{ina}	VA1- - VA3- - 0.3	VA2+,VA5+ +0.3	V
Digital Input Voltage		V_{ind}	-0.3	VA2+, VA5+ +0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 15. VA1+, VA3+, VA4+ must never exceed VA2+ and VA5+ by more than 0.3V.
16. Transient currents of up to 100mA will not cause SCR latch-up.

WARNING: Operating at or beyond these limits may result in permanent damage to tthe device. Normal operation is not guaranteed at these extremes.

ORDERING INFORMATION



The device used in the example above is a CAT5412JCI-1 (Side Braze DIP, Industrial temperature, 1MHz).

Ordering Guide

Model	Throughput	Signal to (Noise plus Distortion	Linearity Error	Temp. Range	Package
CAT5412JC-1	1MHz	65 dB	±1 LSB	0 to 70°C	40-pin Ceramic SB DIP
CAT5412KC-1	1MHz	68 dB	±1/2 LSB	0 to 70°C	40-pin Ceramic SB DIP
CAT5412JC-2	2MHz	65 dB	±1 LSB	0 to 70°C	40-pin Ceramic SB DIP
CAT5412KC-2	2MHz	68 dB	± 1/2 LSB	0 to 70°C	40-pin Ceramic SB DIP
CAT5412JCI-1	1MHz	65 dB	±1 LSB	-40 to +85°C	40-pin Ceramic SB DIP
CAT5412KCI-1	1MHz	68 dB	±1/2 LSB	-40 to +85°C	40-pin Ceramic SB DIP
CAT5412JCI-2	2MHz	65 dB	±1 LSB	-40 to +85°C	40-pin Ceramic SB DIP
CAT5412KCI-2	2MHz	68 dB	±1/2 LSB	-40 to +85°C	40-pin Ceramic SB DIP
CAT5412JCM-1	1MHz	65 dB	TBD	-55 to +125°C	40-pin Ceramic SB DIP
CAT5412KCM-1	1MHz	68 dB	±1 LSB	-55 TO +125°C	40-pin Ceramic SB DIP

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Catalyst Semiconductor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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