



**PRELIMINARY**

**CY62148**

# 512K x 8 Static RAM

## Features

- 4.5V–5.5V operation
- CMOS for optimum speed/power
- Low active power  
— 660 mW (max.)
- Low standby power (L version)  
— 2.75 mW (max.)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with CE and OE options

## Functional Description

The CY62148 is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ), an active LOW output enable ( $\overline{OE}$ ), and three-state drivers. This device has

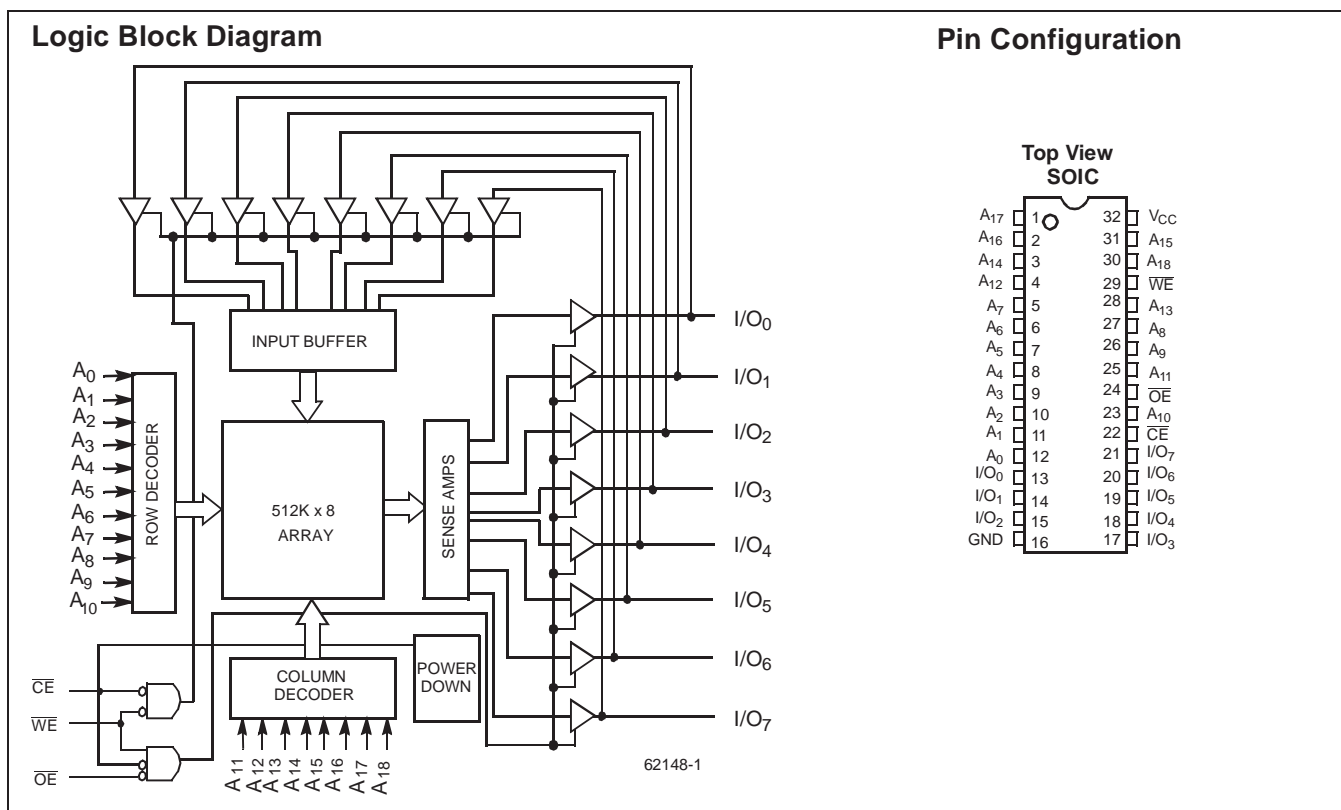
an automatic power-down feature that reduces power consumption by more than 99% when deselected.

Writing to the device is accomplished by taking chip enable one ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>).

Reading from the device is accomplished by taking chip enable one ( $\overline{CE}$ ) and output enable ( $\overline{OE}$ ) LOW while forcing write enable ( $\overline{WE}$ ). Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY62148 is available in a standard 450-mil-wide body width SOIC package.



## Selection Guide

		CY62148-55	CY62148-70
Maximum Access Time (ns)		55	70
Maximum Operating Current	Commercial	120 mA	120 mA
Maximum CMOS Standby Current	Commercial	2 mA	2 mA
	L	0.5 mA	0.5 mA

Shaded areas contain advance information



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[1]</sup> .... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State<sup>[1]</sup>..... -0.5V to V<sub>CC</sub> +0.5V

DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> +0.5V

Current into Outputs (LOW) ..... 20 mA

**Operating Range**

Range	Ambient Temperature <sup>[2]</sup>	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range<sup>[3]</sup>

Parameter	Description	Test Conditions	62148-55		62148-70		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -1 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 2.1 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> +0.3	2.2	V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.3	0.8	-0.3	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		120		120	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		15		15	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f=0		2		2	mA
			L	500		500	μA

Shaded areas contain advance information

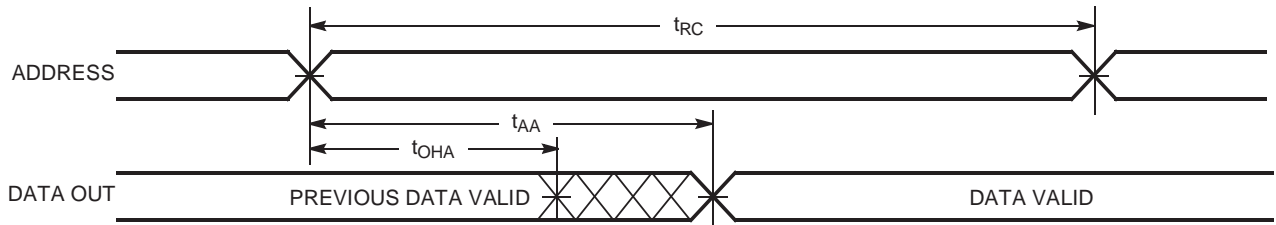
**Capacitance<sup>[5]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

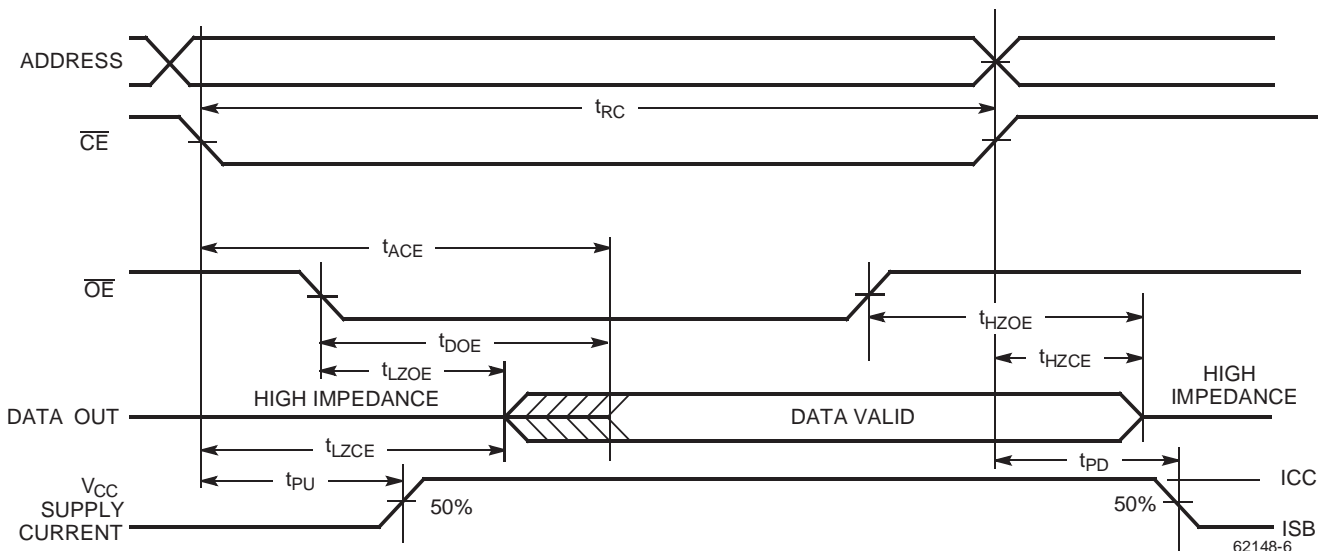
**Notes:**

- V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

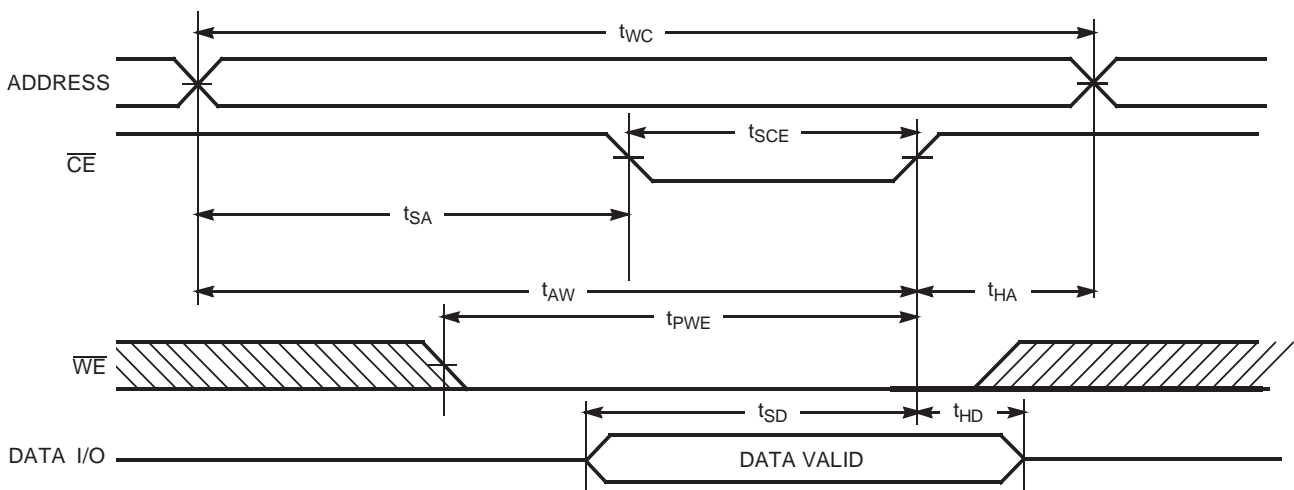


**Switching Waveforms**
**Read Cycle No.1<sup>[10,11]</sup>**


62148-5

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[11,12]</sup>**


62148-6

**Write Cycle No. 1 ( $\overline{CE}$  Controlled)<sup>[13,14]</sup>**


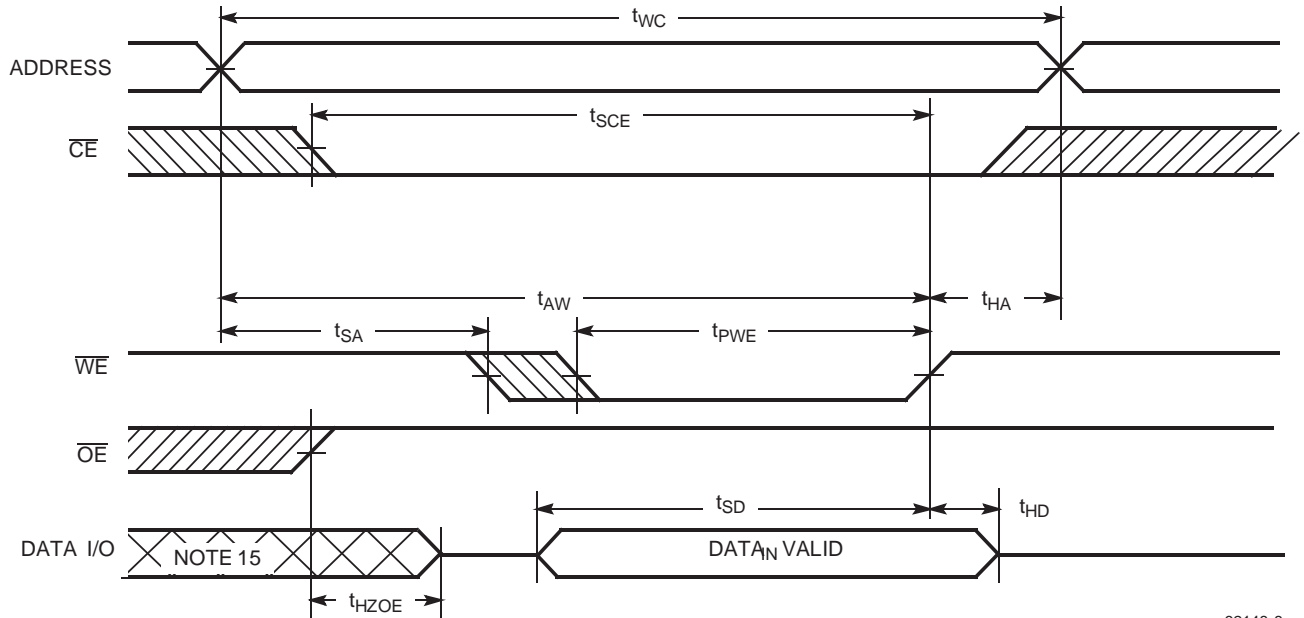
62148-7

**Notes:**

10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  =  $V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
13. Data I/O is high impedance if  $\overline{OE}$  =  $V_{IH}$ .
14. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

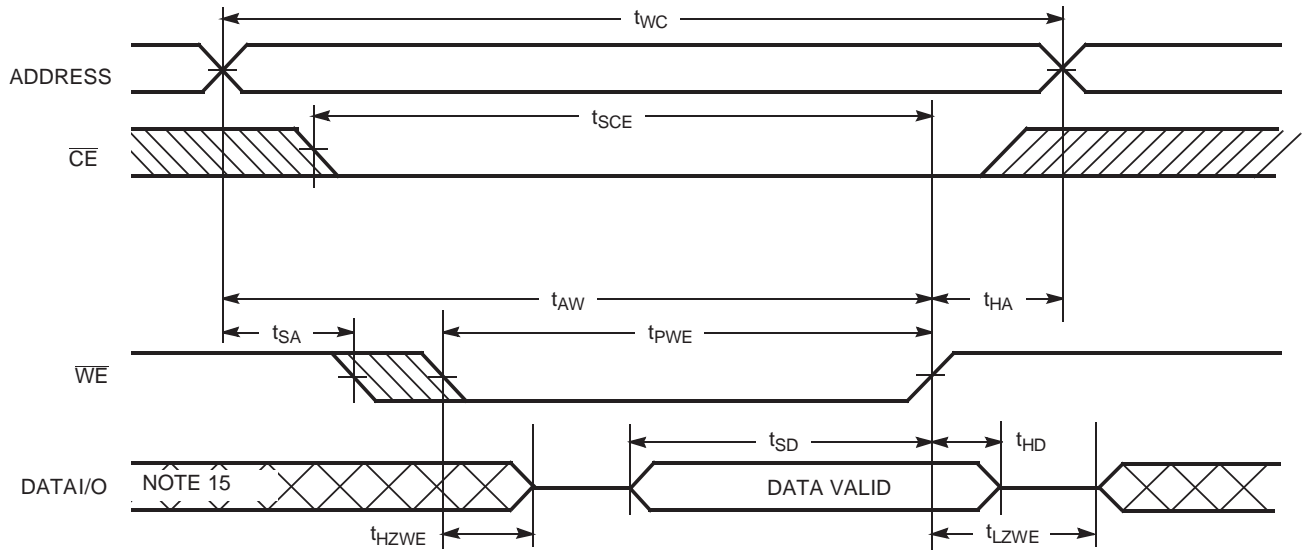
**Switching Waveforms** (continued)

**Write Cycle No. 2 (WE Controlled, OE HIGH During Write)<sup>[13,14]</sup>**



62148-8

**Write Cycle No.3 (WE Controlled, OE LOW)<sup>[13,14]</sup>**



62148-9

**Note:**

15. During this period the I/Os are in the output state and input signals should not be applied



**Truth Table**

CE <sub>1</sub>	OE	WE	I/O <sub>0</sub> –I/O <sub>7</sub>	Mode	Power
H	X	X	High Z	Power-Down	Standby (I <sub>SB</sub> )
X	X	X	High Z	Power-Down	Standby (I <sub>SB</sub> )
L	L	H	Data Out	Read	Active (I <sub>CC</sub> )
L	X	L	Data In	Write	Active (I <sub>CC</sub> )
L	H	H	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

**Data Retention Characteristics** Over the Operating Range

Parameter	Description	Conditions	Min.	Max	Unit	
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	No input may exceed V <sub>CC</sub> + 0.5V V <sub>CC</sub> = V <sub>DR</sub> = 2.0V, CE ≥ V <sub>CC</sub> – 0.3V V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.3V or V <sub>IN</sub> ≤ 0.3V	2.0		V	
I <sub>CCDR</sub>	Data Retention Current		(Com'l)	200		μA
			(Ind'l)	500		μA
			(Mil)	2		mA
t <sub>CDR</sub>	Chip Deselect to Data Retention Time			0		ns
t <sub>R</sub>	Operation Recovery Time		t <sub>RC</sub>		ns	

**Ordering Information**

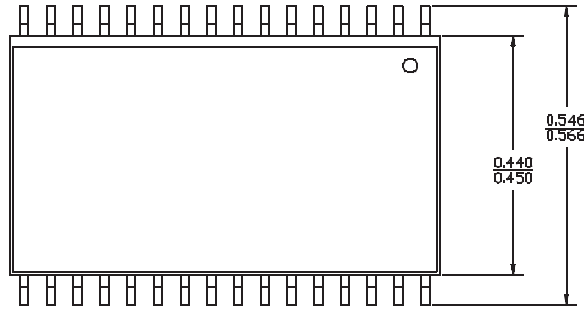
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62148–55SC	S34	32-Lead (450-Mil) Molded SOIC	Commercial
55	CY62148L–55SC	S34	32-Lead (450-Mil) Molded SOIC	Commercial
70	CY62148–70SC	S34	32-Lead (450-Mil) Molded SOIC	Commercial
70	CY62148L–70SC	S34	32-Lead (450-Mil) Molded SOIC	Commercial
70	CY62148-70SI	S34	32-Lead (450-Mil) Molded SOIC	Industrial
70	CY62148L-70SI	S34	32-Lead (450-Mil) Molded SOIC	Industrial

Shaded areas contain advance information.

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**Package Diagrams**

**32-Lead (450 Mil) Molded SOIC S34**



DIMENSIONS IN INCHES MIN. MAX.

