SONY

CXA1392Q/R

Encoder for CCD Color Camera

Description

The CXA1392Q/R is a bipolar IC developed as an encoder for CCD color cameras.

Color difference and luminance signals are input to be output as composite video and Y/C separation signals.

Features

- Carrier balance adjustment unnecessary (Carrier leak above 36dB against burst)
- High S/N
- Low power consumption (140mW)

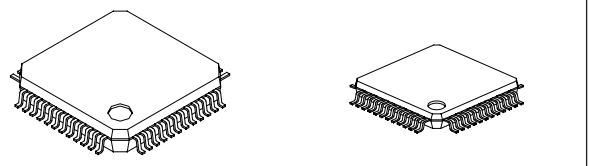
Appications

CCD camera

Structure

Bipolar silicon monolithic IC

CXA1392Q	CXA1392R
48 pin QFP (Plastic)	48 pin LQFP (Plastic)



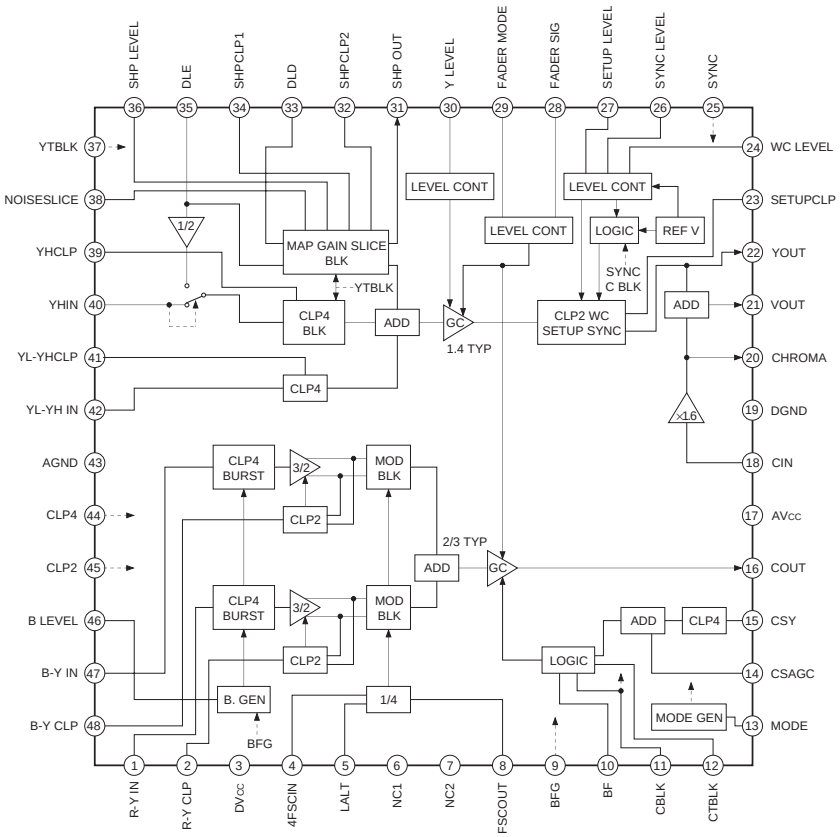
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	7	V
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	600	mW

Operating Conditions

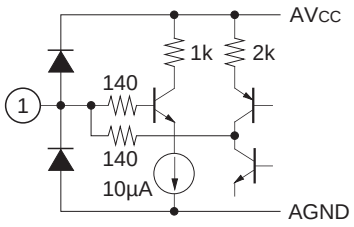
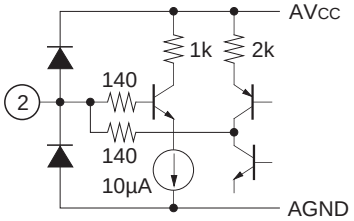
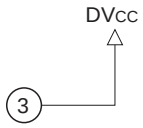
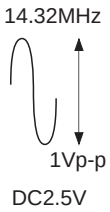
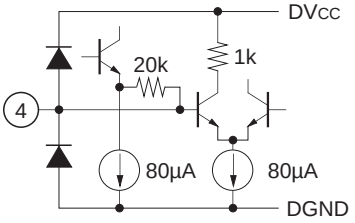
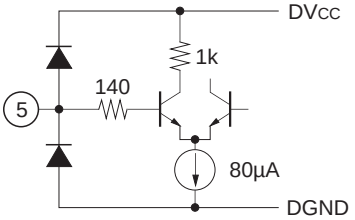
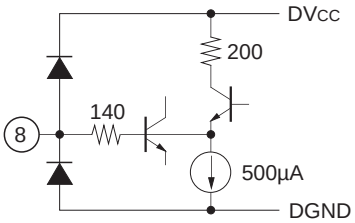
• Supply voltage	Vcc	4.75 to 5.25	V
• Ambient temperature	Topr	–20 to +75	°C

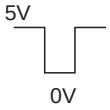
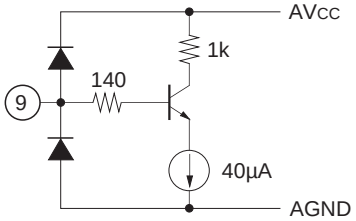
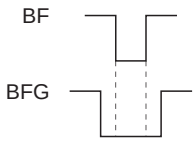
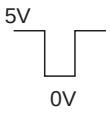
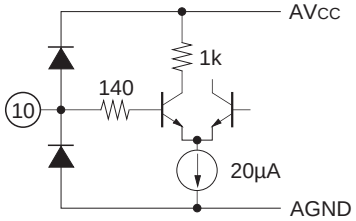
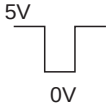
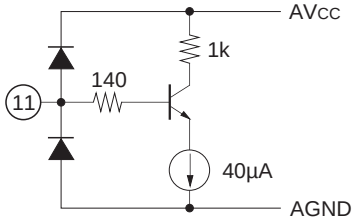
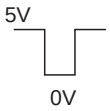
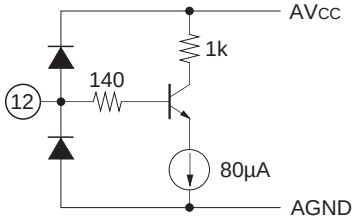
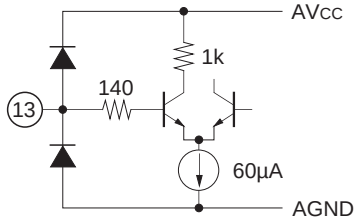
Block Diagram and Pin Configuration

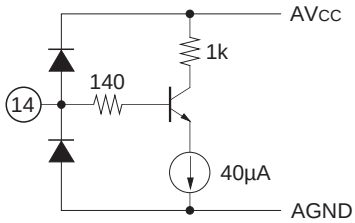
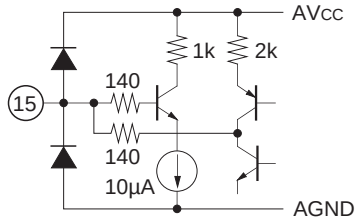
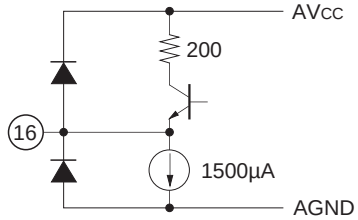
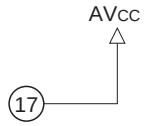
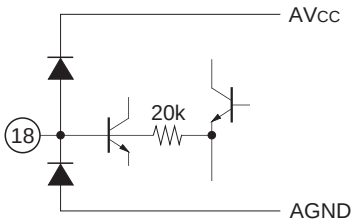
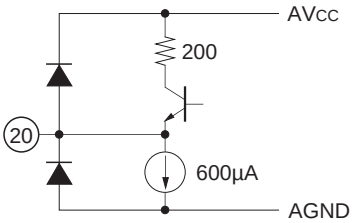


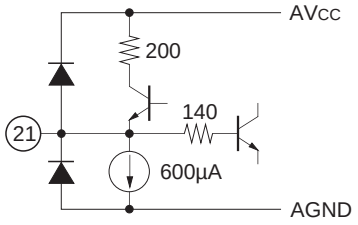
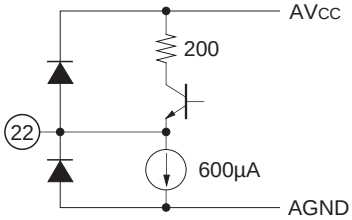
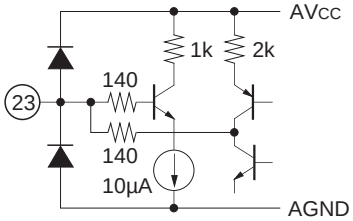
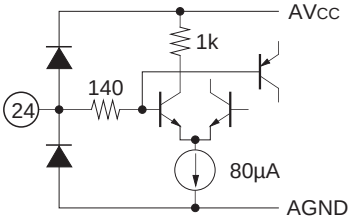
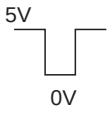
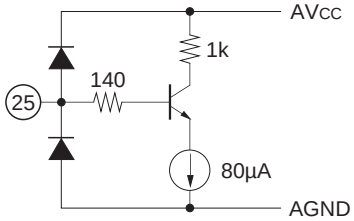
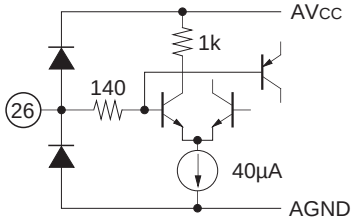
E89Z08B79-PS

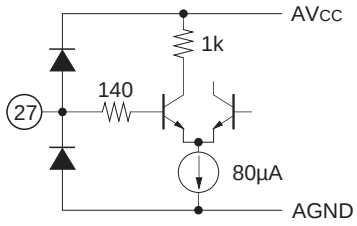
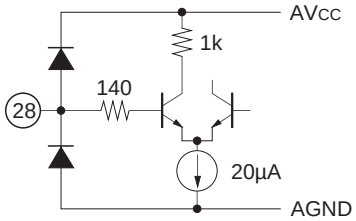
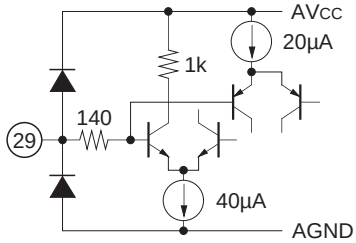
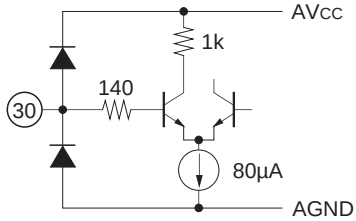
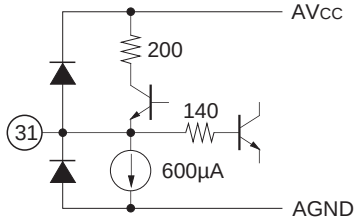
Pin Description

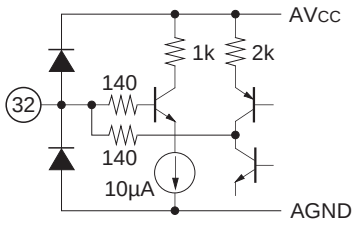
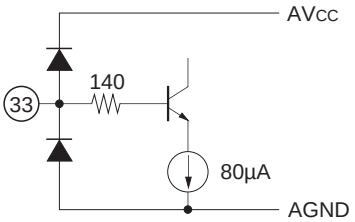
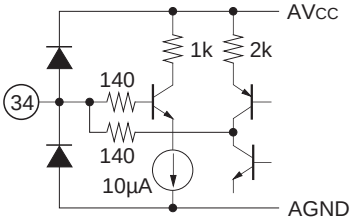
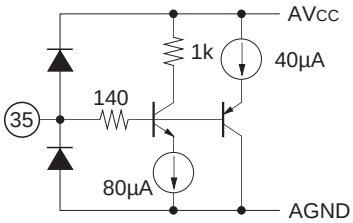
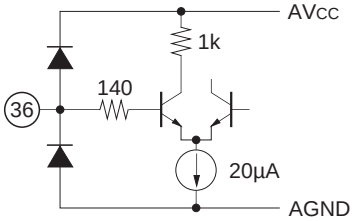
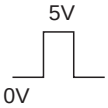
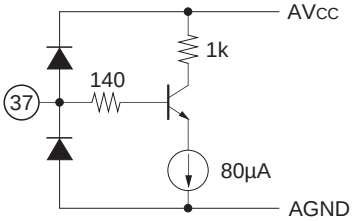
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	R-Y IN	3V		R-Y signal input pin. Inputs through capacitor. Clamped internally.
2	R-Y CLP	3.4V		Pin connecting the capacitor for R-Y modulator clamp. Setting the capacitance to too small a value will enlarge the carrier leak. 0.1µF and above is recommended.
3	DVcc	5V		Power supply pin for the 1/4 counter block.
4	4FSCIN			Input pin for the 4FSC used to make up the Sub Carrier. Input through capacitor. Set amplitude to over 500mVp-p.
5	LALT	0V		Input pin for Line Alternate signal during PAL mode. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than $V_{TH} \pm 0.5V$. Set to GND during NTSC mode.
6	NC1	—		Not for use. Leave this pin open.
7	NC2	—		Not for use. Leave this pin open.
8	FSCOUT	5V		Outputs a sub carrier with the same phase as B-Y. When not in use, connection to Vcc prevents output and allows for 600µA of current saving. Determining phase to 4FSC is impossible.

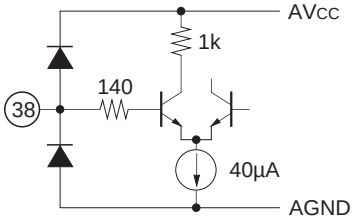
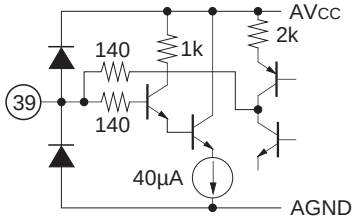
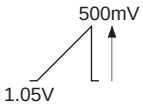
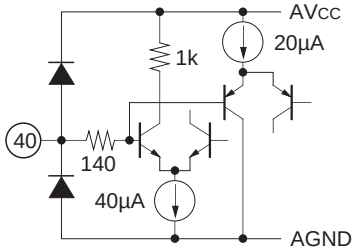
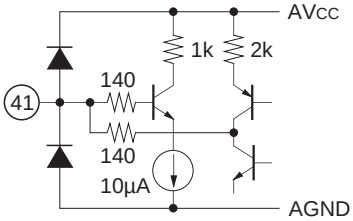
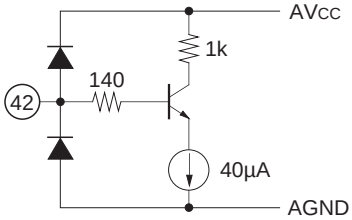
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
9	BFG			Inserts a pulse slightly larger than BF on both ends.  V_{TH} is at 2.5V. Input a pulse with an amplitude larger than $V_{TH} \pm 0.5V$.
10	BF			Inputs BF (burst flag) pulse. During analog burst, the input pulse smoothens the waveform. The input pulse waveform becomes the envelope of the analog burst waveform.  During the usual burst, be sure to input the pulse.
11	CBLK			Inputs CBLK (composite blanking) pulse. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than $V_{TH} \pm 0.5V$.
12	CTBLK			Inputs CT (chroma titler) pulse. This signal prevents the application of chroma suppress during the titler signal period. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than $V_{TH} \pm 0.5V$.
13	MODE	0V		Selects NTSC, PAL or NTSC × 2, PAL × 2 modes. 0V: NTSC × 1 2.5V: NTSC × 2 3.5V: PAL × 2 5V: PAL × 1

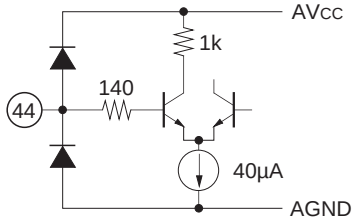
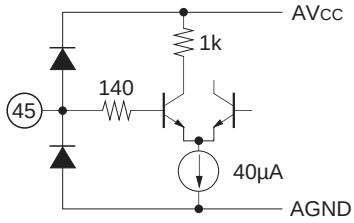
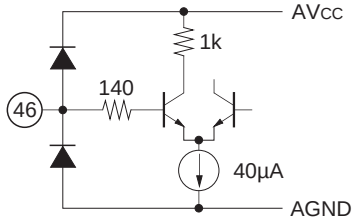
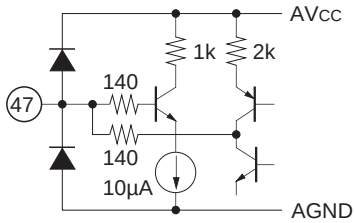
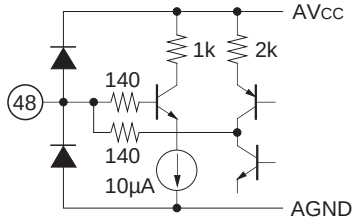
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
14	CSAGC	0V		Suppresses chroma signal at the AGC gain control signal. 3V (100%) to 4.2V (50%)
15	CSY	2.4V		Suppress chroma signal at the Y signal. 200mV (100%) to 700mV (0%) Inputs through capacitor. Clamped internally.
16	COUT	2.8V		Chroma signal output pin. Output as rectangular waves.
17	AVCC	5V		Power supply pin for other than 1/4 counter block.
18	CIN	2.5V		Input pin for chroma signal passed through BPF. Internally biased with a 20kΩ resistance. Input through capacitor.
19	DGND	0V		GND pin for 1/4 counter block.
20	CHROMA	2V		Signals input from CIN are amplified and output through this pin. Chroma signal output pin when used for Y/C separation output.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
21	VOUT	1.8V		Output pin of composite video signal. When not in use, connection to Vcc allows for 900µA of current saving.
22	YOUT	2.4V		Y signal output pin when used for Y/C separation output.
23	SETUPCLP	3.3V		Connecting pin for the white clip clamp capacitor. Over 0.1µF is recommended.
24	WC LEVEL	3.4V		White clip level control pin. 1.6V (550mV) to 5V (1110mV)
25	SYNC			Sync pulse input pin. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than V_{TH} ± 0.5V.
26	SYNC LEVEL	0V		Sync level control pin. 1.6V (180mV) to 5V (380mV) 0V (287mV) preset

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
27	SETUP LEVEL	3.5V		Setup level control pin. 2.4V (0mV) to 5V (120mV)
28	FADER SIG	0V		Controls the signal suppress level during Black Fader. Controls the signal suppress level during White Fader and at the same time controls the setup level. Signal suppress control: 2V (100%) to 2.9V (0%) Setup level control: 2V (0%) to 2.9V (100%) BIack Fader/White Fader mode selection executed through Fader Mode pin.
29	FADER MODE	3.5V		BIack Fader and White Fader mode select pin. Also controls the final value (100%) of White Fader white level (setup level) . 0V (Black Fader) 1.8V (100mV) to 5V (630mV) (White Fader)
30	Y LEVEL	3.4V		Y signal level control pin. 1.6V (–3.5dB) to 5V (9dB)
31	SHP OUT	3V		Aperture signal output pin. When not in use, connection to Vcc allows for 700µA of current saving.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
32	SHPCLP2	3.2V		Connects the clamp capacitor used for the slice of the aperture signal.
33	DLD	2.1V		Connects the delay line drive side of the aperture signal.
34	SHPCLP1	3.2V		Connects the clamp capacitor used for the slice of the aperture signal.
35	DLE	2.1V		Connects the delay line end side of the aperture signal. When this pin signals are used as Y_H signals, YHIN pin is connected to Vcc.
36	SHP LEVEL	3.5V		Control pin of the aperture signal level. 2.6V (14dB) to 4.2V (–25dB)
37	YTBLK			Inputs Y_T (Y titler) pulse. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than $V_{TH} \pm 0.5V$.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
38	NOISESLICE	3.5V		Controls the slice level of the aperture signal. 1.8V (0mV) to 5V (150mV)
39	YHCLP	2.7V		Connects the capacitor for Y_H input clamp.
40	YHIN			Y_H signal input pin. When DLE pin signal is set as Y_H signal, connect this pin to Vcc. The input signal DC clamp range stands at 1.05V ± 0.65V. The standard signal level is at 500mV.
41	YL-YHCLP	3.4V		Connects the capacitor for Y_L-Y_H input clamp.
42	YL-YH IN	2.8V		Inputs V aperture signals, titler signals and Y_L-Y_H signals. The input signal DC clamp range stands at 2.8V ± 1.1V.
43	AGND	0V		GND pin for other than 1/4 counter block.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
44	CLP4	5V 0V		CLP4 pulse input pin. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than V_{TH} ± 0.5V.
45	CLP2	5V 0V		CLP2 pulse input pin. V_{TH} is at 2.5V. Input a pulse with an amplitude larger than V_{TH} ± 0.5V.
46	B LEVEL	3.5V		Controls the burst level. 1.6V (95mVp-p) to 5V (280mVp-p) (NTSC pulse burst mode)
47	B-Y IN	3V		R-Y signal input pin. Inputs through capacitor. Clamped internally.
48	B-Y CLP	3.4V		Connects the capacitor for B-Y modulator clamp. Setting the capacitance to too small a value will enlarge the carrier leak. Over 0.1µF is recommended.

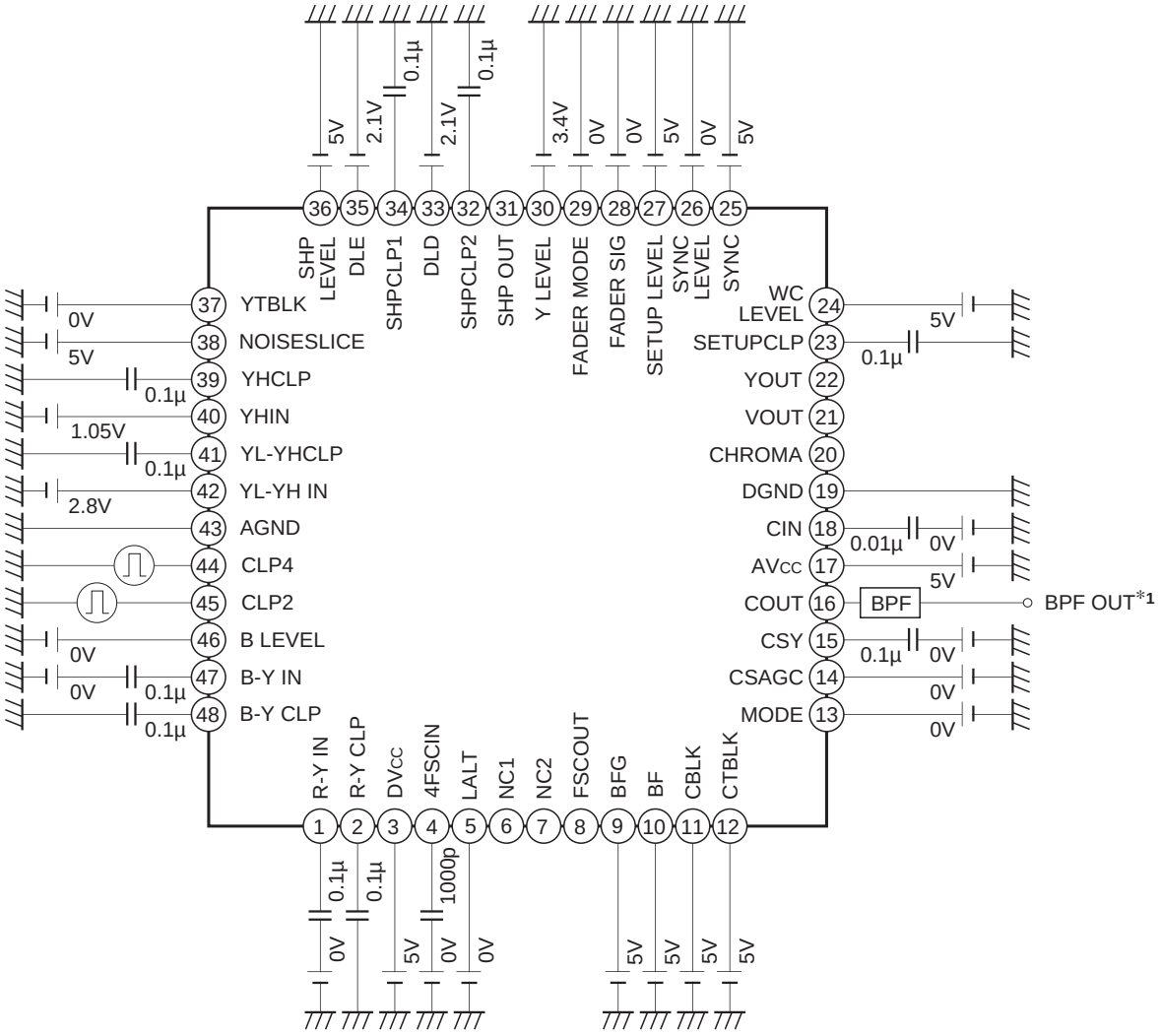
Electrical Characteristics (V_{CC} = 5V, Ta = 25°C)

No.	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
1	Supply Current	Icc	AV_{CC} + DV_{CC}	19	28	38	mA
2	YH GAIN TYP	YHTYP	FSCOUT = 5V VOUT = 5V SHPOUT = 5V YHIN (500mV pulse) → YOUT	1.8	2.8	3.8	dB
3	YH GAIN MIN	YHMIN	YHIN (500mV pulse) → YOUT YLEVEL = 1.6V	—	–4	–2	dB
4	YH GAIN MAX	YHMAX	YHIN (250mV pulse) → YOUT YLEVEL = 5V	8	9.1	—	dB
5	YL-YH GAIN	YL-YH	Y_L-Y_HIN (500mV pulse) → YOUT	1.8	2.8	3.8	dB
6	DLE GAIN	DLE	DLE (1V pulse) → YOUT YHIN = 5V	–4.3	–3.3	–2.3	dB
7	VOUT GAIN	VOUT	YHIN (500mV pulse) → VOUT	1.3	2.3	3.3	dB
8	WHITE FADER MIN	WFMIN	CBLK pulse FADERMODE = 1.6V WFMIN = YOUT output level – SETMAX (No.13)	68	86	104	mV
9	WHITE FADER MAX	WFMAX	CBLK pulse FADERMODE = 5V WFMAX = YOUT output level – SETMAX (No.13)	527	620	713	mV
10	WHITE CLIP MIN	WCMIN	YHIN (500mV pulse) → YOUT CBLK pulse WCLEVEL = 1.6V	522	550	578	mV
11	WHITE CLIP MAX	WCMAX	YHIN (500mV pulse) → YOUT CBLK pulse WCLEVEL = 5V	1056	1112	1168	mV
12	WHITE CLIP PRESET	WCPRE	YHIN (500mV pulse) → YOUT CBLK pulse WCLEVEL = 0V	796	838	880	mV
13	SETUP MAX	SETMAX	CBLK pulse → YOUT SETUPLEVEL = 5V	113	126	139	mV
14	SYNC MIN	SYNCMIN	SYNC pulse → YOUT SYNCLEVEL = 1.6V	165	180	195	mV
15	SYNC MAX	SYNCMAX	SYNC pulse → YOUT SYNCLEVEL = 5V	363	383	403	mV
16	SYNC PRESET	SYNCPRE	SYNC pulse → YOUT SYNCLEVEL = 0V	272	287	302	mV
17	SHP-YOUT GAIN	SHPYOUT	DLD (40mV pulse) → YOUT SHPLEVEL = 2.6V YHIN (500mV pulse)	12	14	16	dB
18	SHP DOWN MIN	SHPMIN	DLD (40mV pulse) → SHPOUT SHPLEVEL = 4.2V	—	–25	–5.5	dB
19	SHP DOWN TYP	SHPTYP	DLD (40mV pulse) → SHPOUT SHPLEVEL = 3.4V	5.5	7	8.5	dB
20	SHP DOWN MAX	SHPMAX	DLD (40mV pulse) → SHPOUT ⋯ (DOWNMAX) SHPLEVEL = 2.6V	11.7	13.2	14.7	dB
21	SHP DOWN/ UP	SHPD/U	DLE (40mV pulse) → SHPOUT ⋯ (UPMAX) SHPLEVEL = 2.6V SHPD/U = DOWNMAX/UPMAX	2.4	2.8	3.2	times
22	SHP SLICE MAX	SLICEMAX	DLD (40mV pulse) → SHPOUT ⋯ (SLMAX) SHPLEVEL = 2.6V SLICEMAX = DOWNMAX – SLMAX	135	150	165	mV
23	B-Y GAIN	B-Y	B-YIN (300mV pulse) → BPFOUT 4FSCIN = SIN 1Vp-p 14.32MHz B-Y = 20 log {BPFOUT (mVp-p)/300mV}	0.4	1.6	2.8	dB

No.	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
24	R-Y GAIN	R-Y	R-YIN (300mV pulse) → BPFOUT ··· (R-Y level) 4FSCIN = SIN 1Vp-p 14.32MHz R-Y = 20 log {BPFOUT (mVp-p)/300mV}	0.4	1.6	2.8	dB
25	CARRIER LEAK 3.58MHz	L358	4FSCIN = SIN 1Vp-p 14.32MHz L358 = 20 log {286mVp-p/BPFOUT level (mVp-p)} BURST (Typ.)	36	48	—	dB
26	CARRIER LEAK 500kHz	L500	4FSCIN = SIN 1Vp-p 2MHz L500 = 20 log {286mVp-p/BPFOUT level (mVp-p)} BURST (Typ.)	36	58	—	dB
27	COUT DRANGE	COUTD	R-YIN (600mV pulse) → BPFOUT 4FSCIN = SIN 1Vp-p 14.32MHz	670	730	—	mV
28	CS AGC MAX	CSAGCMAX	R-YIN (300mV pulse) → BPFOUT 4FSCIN = SIN 1Vp-p 14.32MHz CSAGC = 4.2V CSAGCMAX = (BPFOUT level/R-Y level) × 100%	47	52	57	%
29	FSCOUT amplitude	FSC	FSCOUT DC amplitude at 4FSCIN = 2V, 3V	585	673	760	mV
30	BURST NTSC MIN	NTMIN	BFG pulse → BPFOUT BLEVEL = 1.6V 4FSCIN = SIN 1Vp-p 14.32MHz	80	95	110	mV
31	BURST NTSC MAX	NTMAX	BFG pulse → BPFOUT BLEVEL = 5V 4FSCIN = SIN 1Vp-p 14.32MHz	250	280	312	mV
32	BURST PAL MIN	PALMIN	BFG pulse → BPFOUT BLEVEL = 1.6V MODE = 5V 4FSCIN = SIN 1Vp-p 14.32MHz	89	105	120	mV
33	BURST PAL MAX	PALMAX	BFG pulse → BPFOUT BLEVEL = 5V MODE = 5V 4FSCIN = SIN 1Vp-p 14.32MHz	283	316	350	mV
34	BURST NTSC × 2 MIN	NT2MIN	BFG pulse → BPFOUT BLEVEL = 1.6V MODE = 2.5V 4FSCIN = SIN 1Vp-p 14.32MHz	153	180	207	mV
35	BURST NTSC × 2 MAX	NT2MAX	BFG pulse → BPFOUT BLEVEL = 5V MODE = 2.5V 4FSCIN = SIN 1Vp-p 14.32MHz	468	520	572	mV
36	BURST PAL × 2 MIN	PAL2MIN	BFG pulse → BPFOUT BLEVEL = 1.6V MODE = 3.5V 4FSCIN = SIN 1Vp-p 14.32MHz	171	202	232	mV
37	BURST PAL × 2MAX	PAL2MAX	BFG pulse → BPFOUT BLEVEL = 5V MODE = 3.5V 4FSCIN = SIN 1Vp-p 14.32MHz	535	595	655	mV
38	CIN-VOUT GAIN	CINVOUT	CIN (SIN 400mVp-p 3.58MHz) → VOUT	2.5	3.5	4.5	dB
39	CIN-CHROMA GAIN	CINCHROMA	CIN (SIN 400mVp-p 3.58MHz) → CHROMA	2.1	3.1	4.1	dB

Ref) YHIN → YOUT Frequency characteristics gain 10MHz, –2.3dB (Typ.)

Electrical Characteristics Measurement Circuit



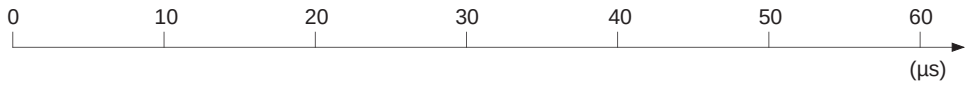
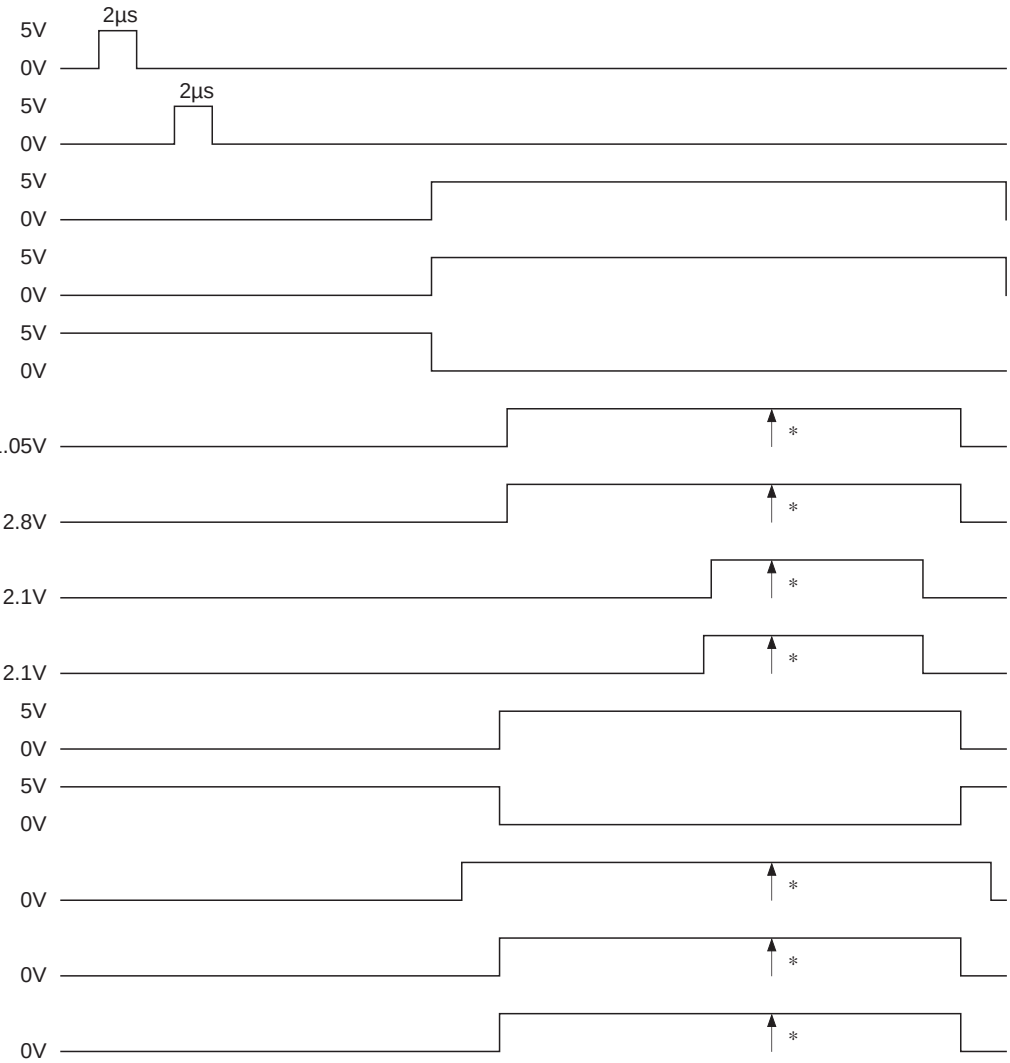
Above conditions are given as the typical setting. The individual conditions of each item are indicated in the chart.

*1 For BPF characteristics proceed as follows.

(1) When 4FSC IN = 14.32MHz, use a 3.58MHz band-pass filter where through the input of a 3.58MHz sine wave a ratio of 2 to 1 is obtained for the input vs. output.

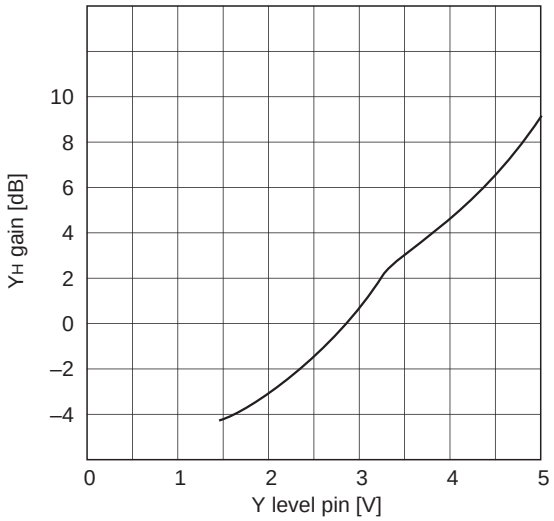
(2) When 4FSC IN = 2MHz, use a 500kHz band-pass filter where through the input of a 500kHz sine wave a ratio of 2 to 1 is obtained for the input vs. output.

Input Signal Timing Chart

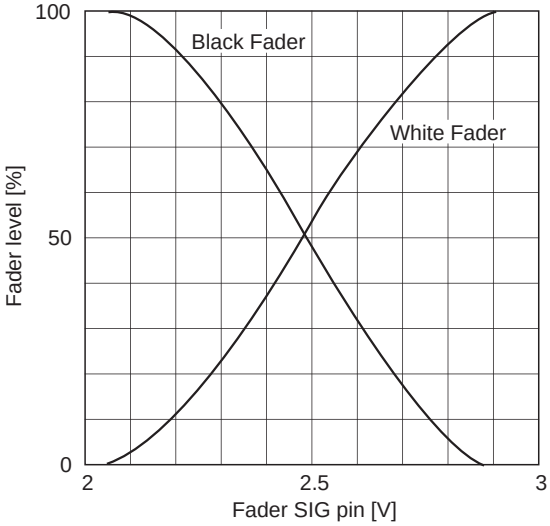
Pin name	Input signal
	
45. CLP2	
44. CLP4	
11. CBLK	
25. SYNC	
9. BFG	
40. YH	
42. YL-YH	
33. DLD	
35. DLE	
37. YTBLK	
12. CTBLK	
15. CSY	
1. R-Y	
48. B-Y	

Note) Level of * is indicated in the conditions shown in the chart.

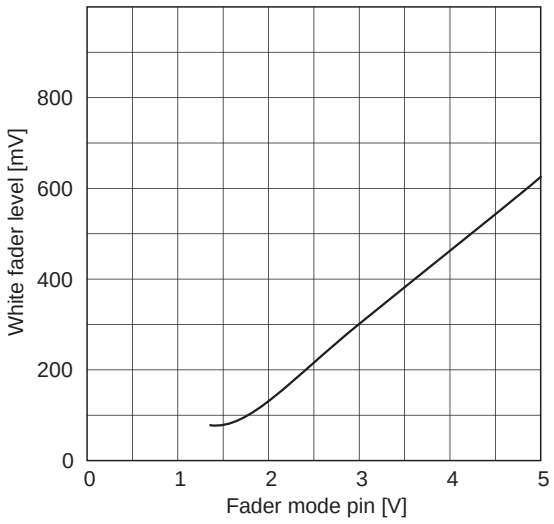
Y_H gain control characteristics



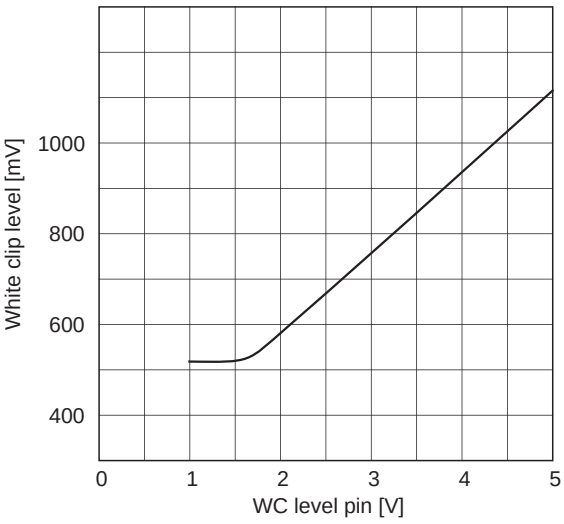
Y fader control characteristics



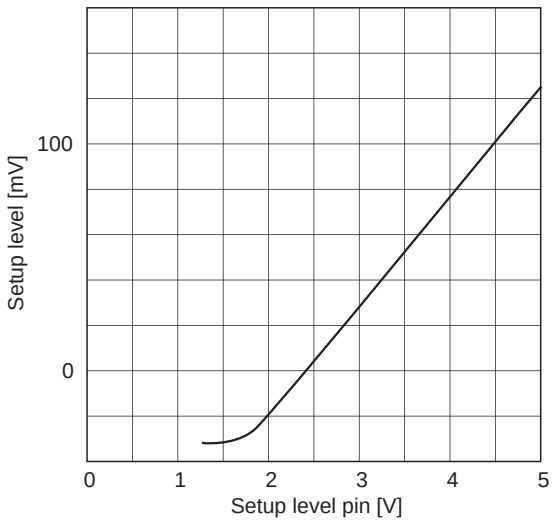
White fader control characteristics



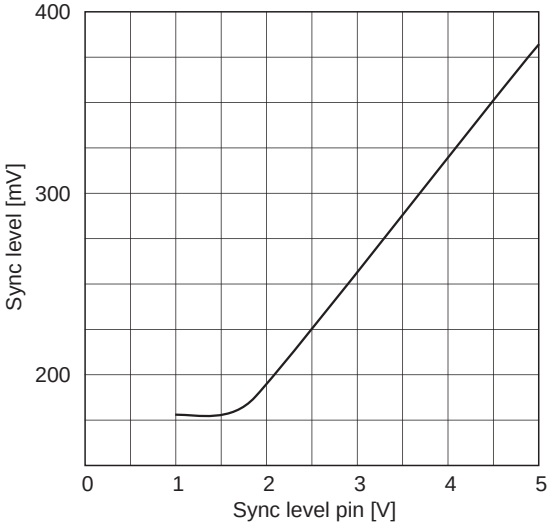
White clip control characteristics



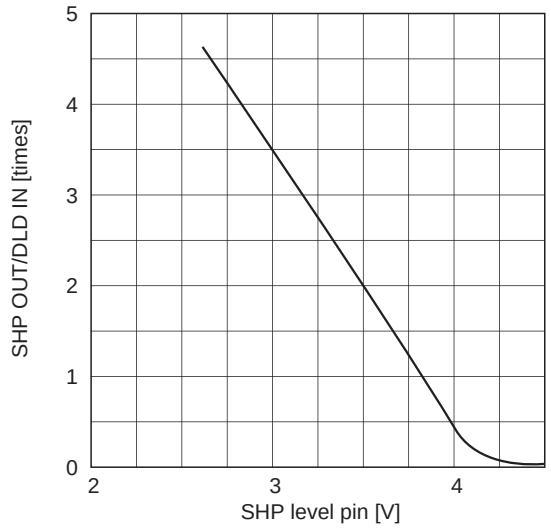
Setup level control characteristics



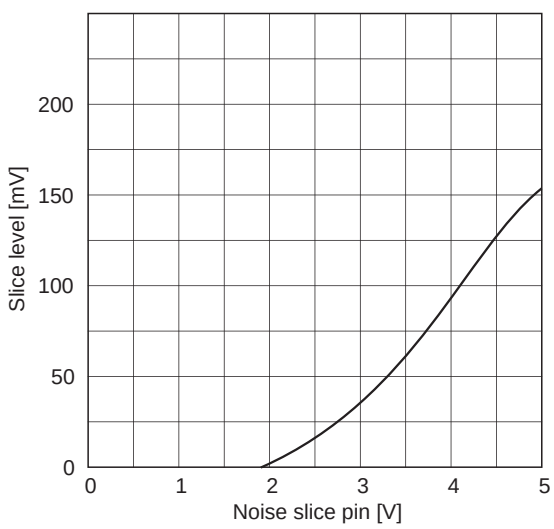
Sync level control characteristics



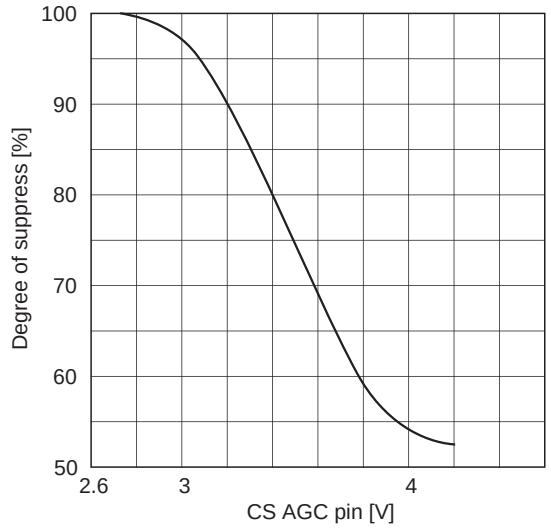
SHP gain control characteristics



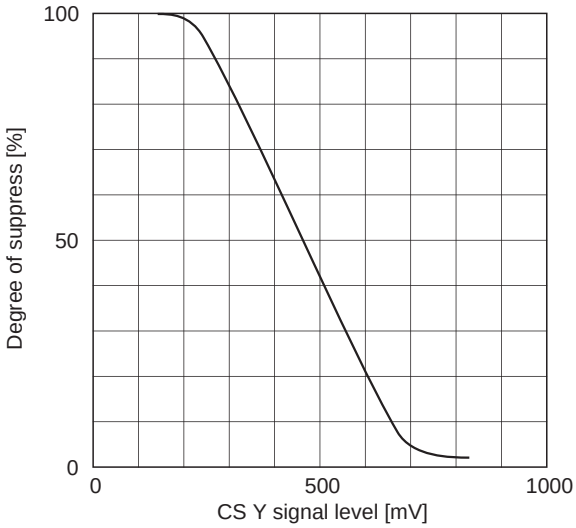
SHP noise slice characteristics



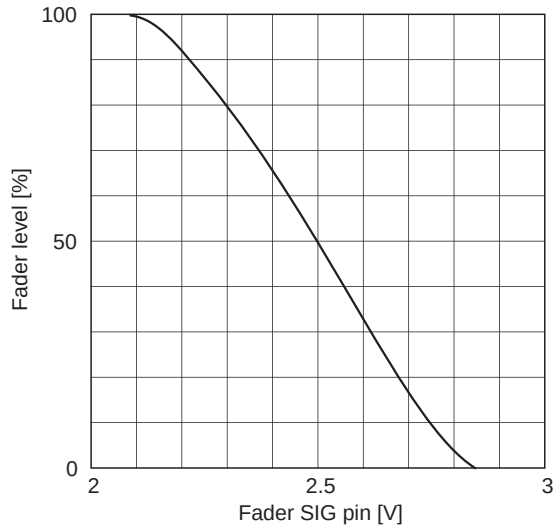
CS AGC control characteristics



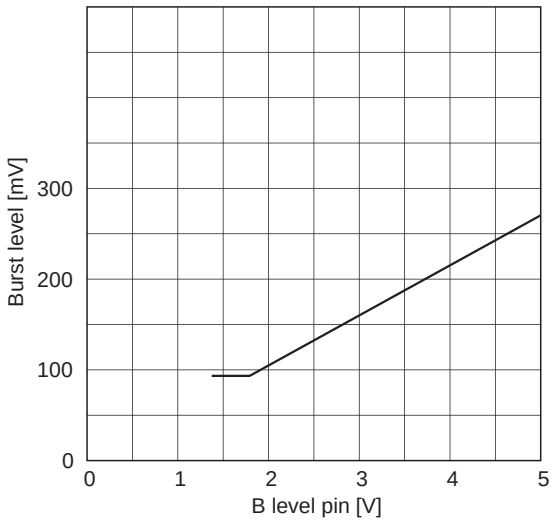
CS Y control characteristics



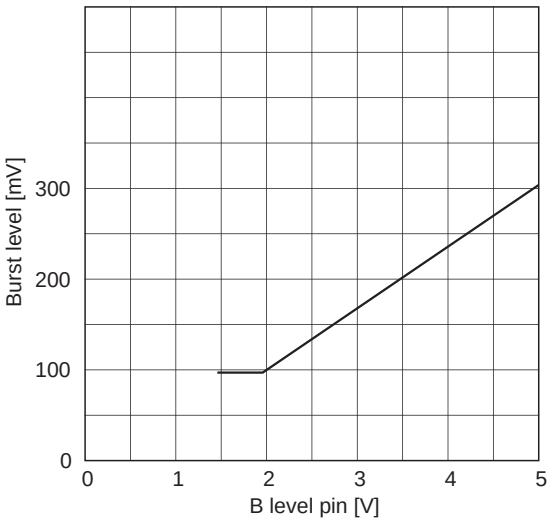
Chroma fader control characteristics



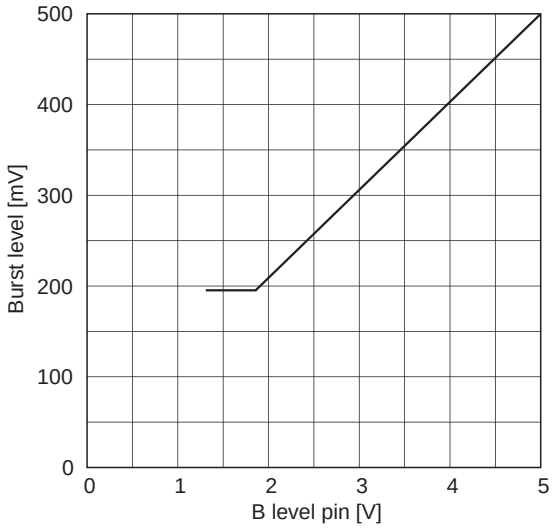
Burst level control characteristics (NTSC pulse mode)



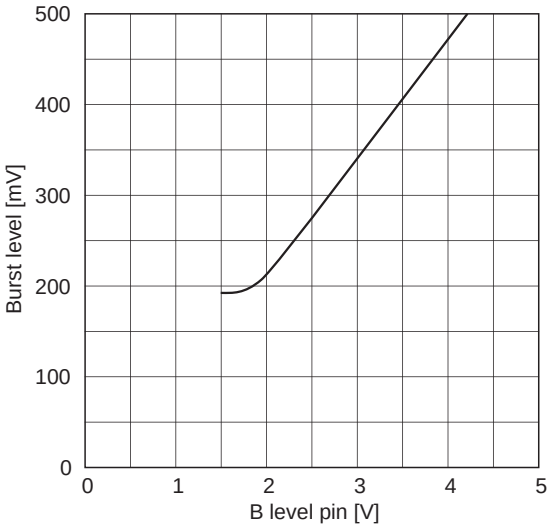
Burst level control characteristics (PAL pulse mode)



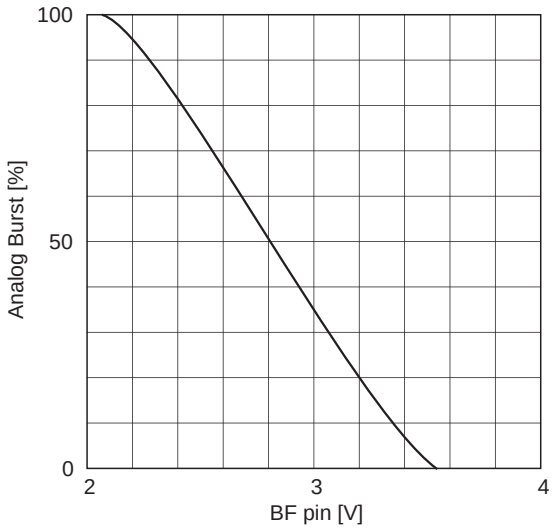
Burst level control characteristics (NTSC analog mode)



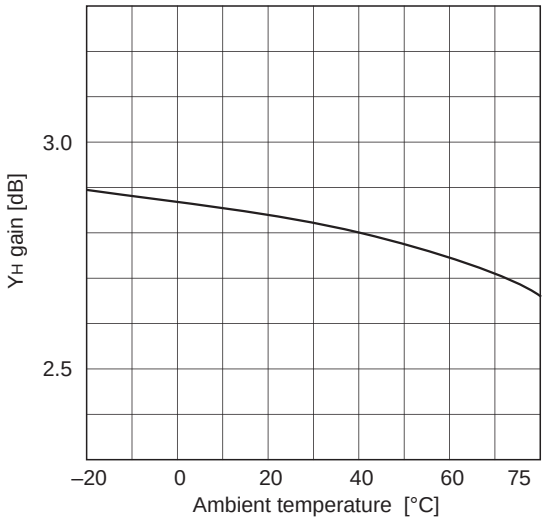
Burst level control characteristics (PAL analog mode)



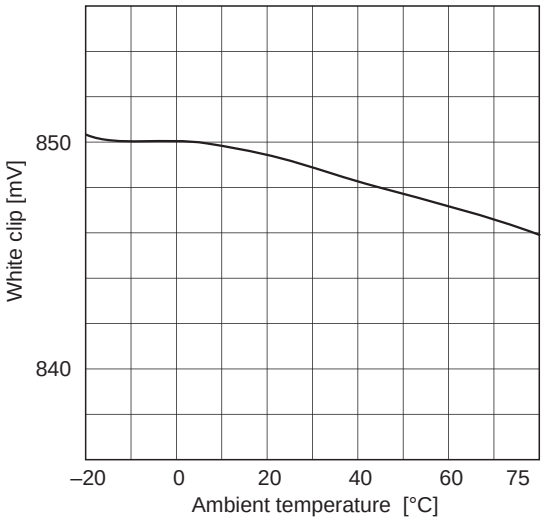
Analog burst control



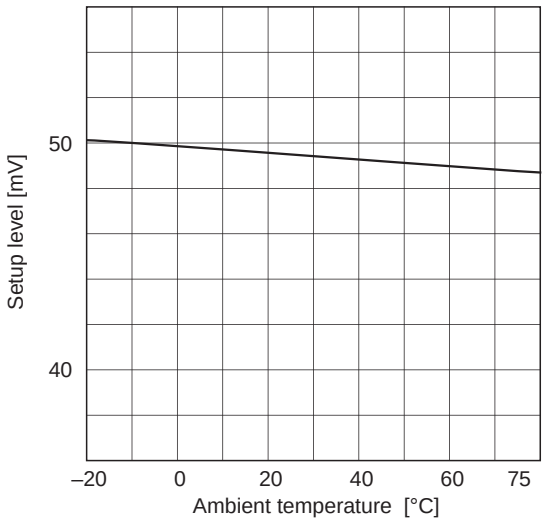
Y_H gain typical temperature characteristics



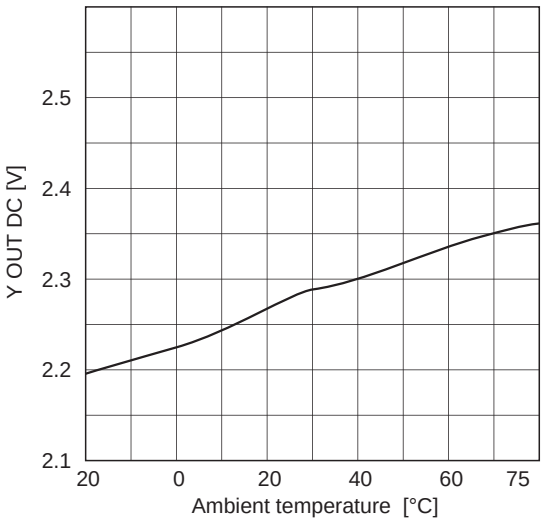
White clip preset temperature characteristics



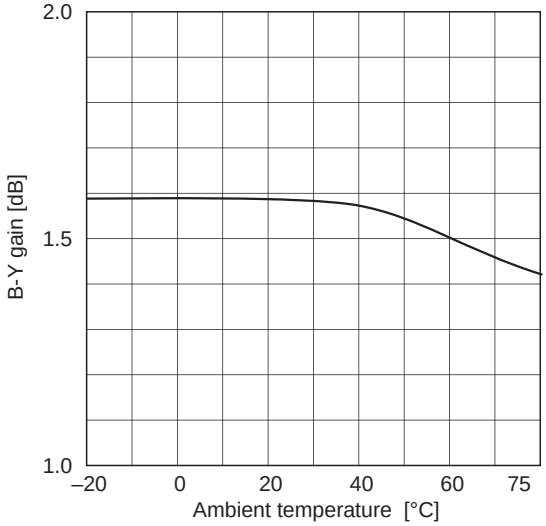
Setup level temperature characteristics (Setup level = 3.4V)



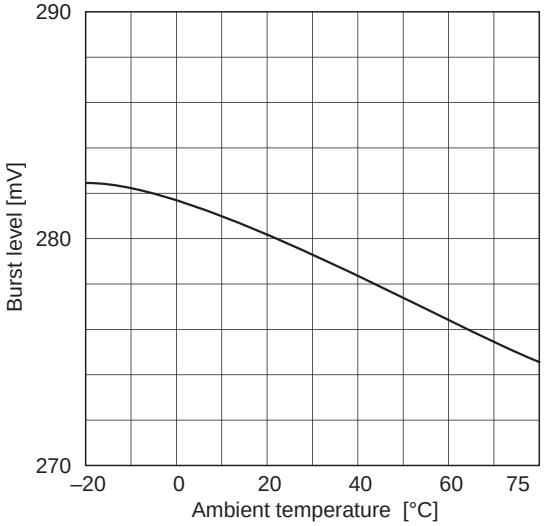
Y OUT DC temperature characteristics



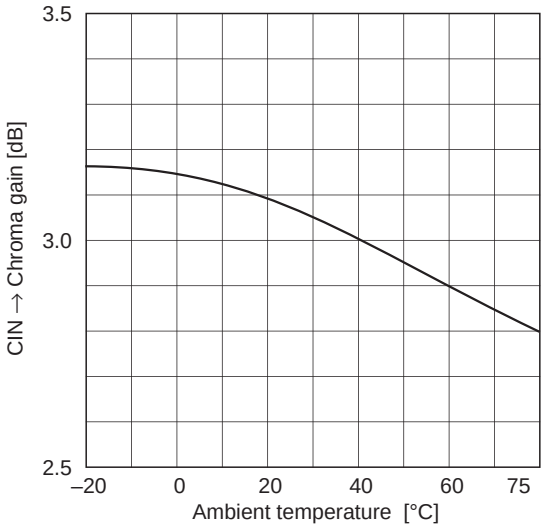
B-Y gain temperature characteristics



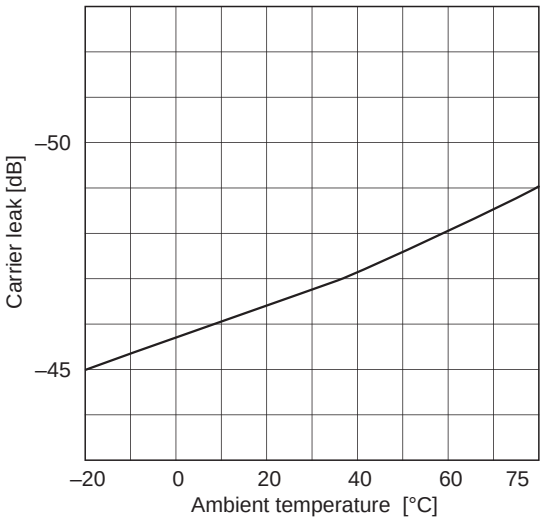
Burst NTSC maximum temperature characteristics (NTSC pulse mode) Burst level = 5.0V



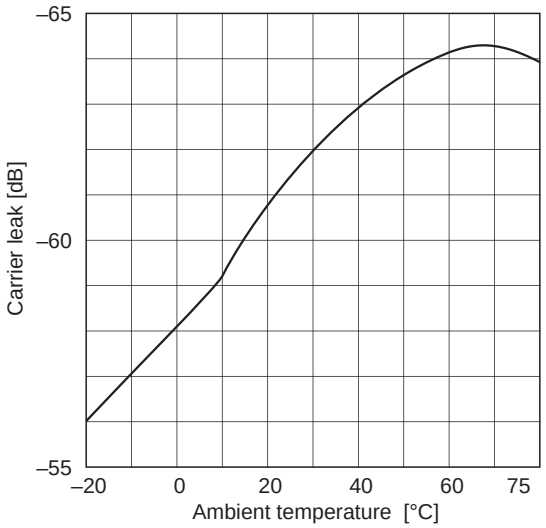
CIN → Chroma gain temperature characteristics



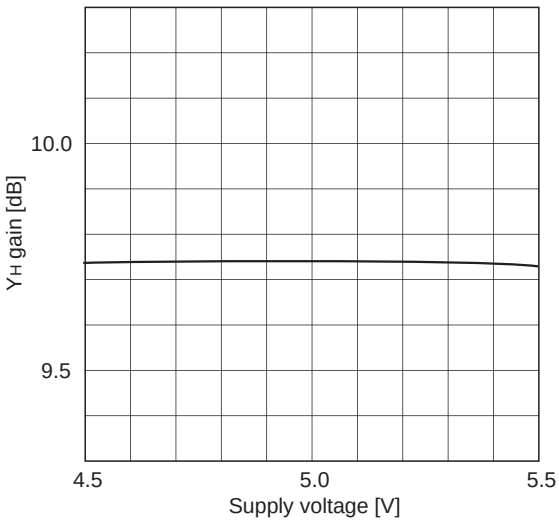
Carrier leak 3.58MHz temperature characteristics



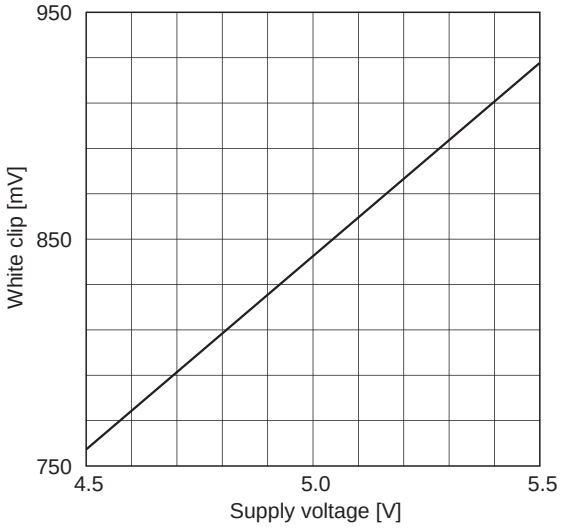
Carrier leak 500kHz temperature characteristics



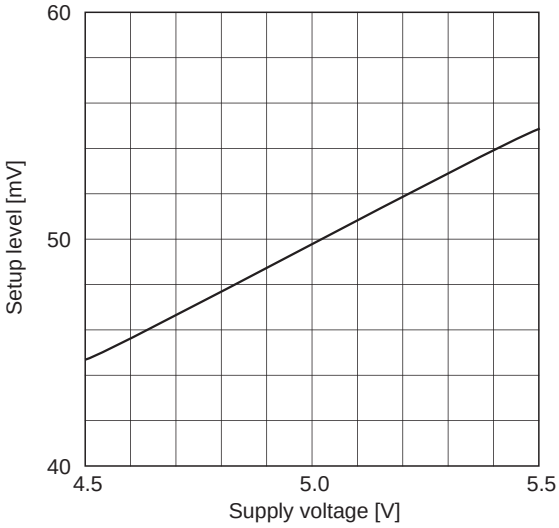
Y_H gain maximum supply voltage characteristics



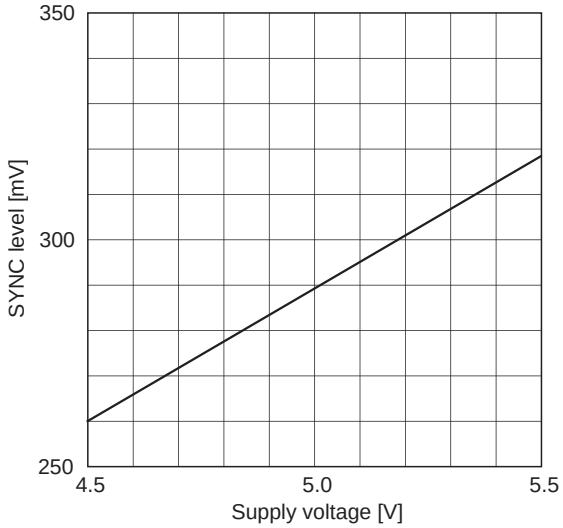
White clip preset supply voltage characteristics



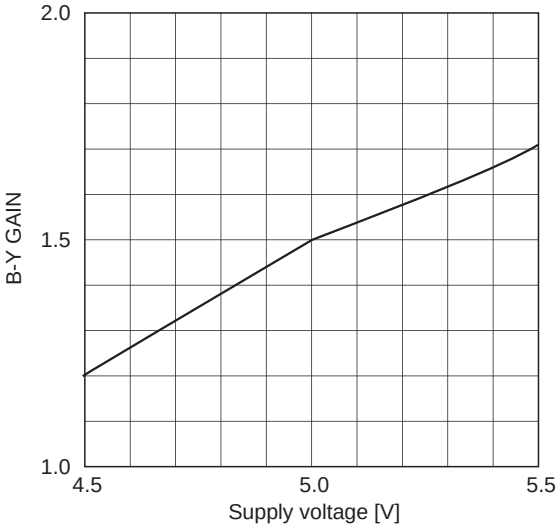
Setup level supply voltage characteristics (Setup level = 3.4/5Vcc)



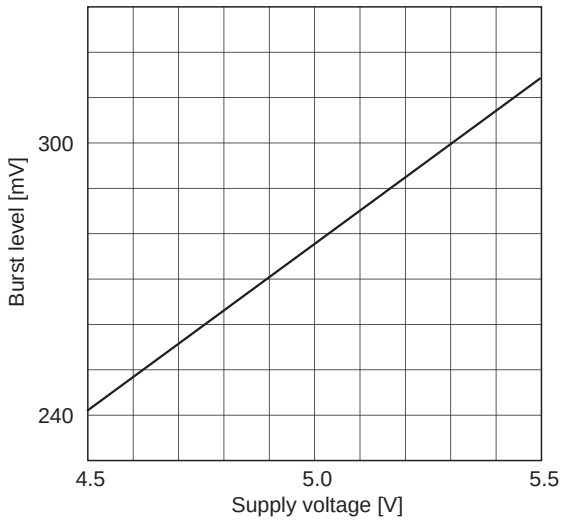
SYNC level preset supply voltage characteristics



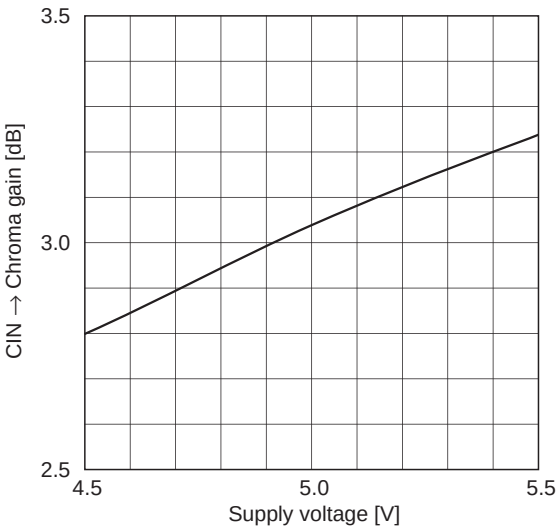
B-Y gain supply voltage characteristics



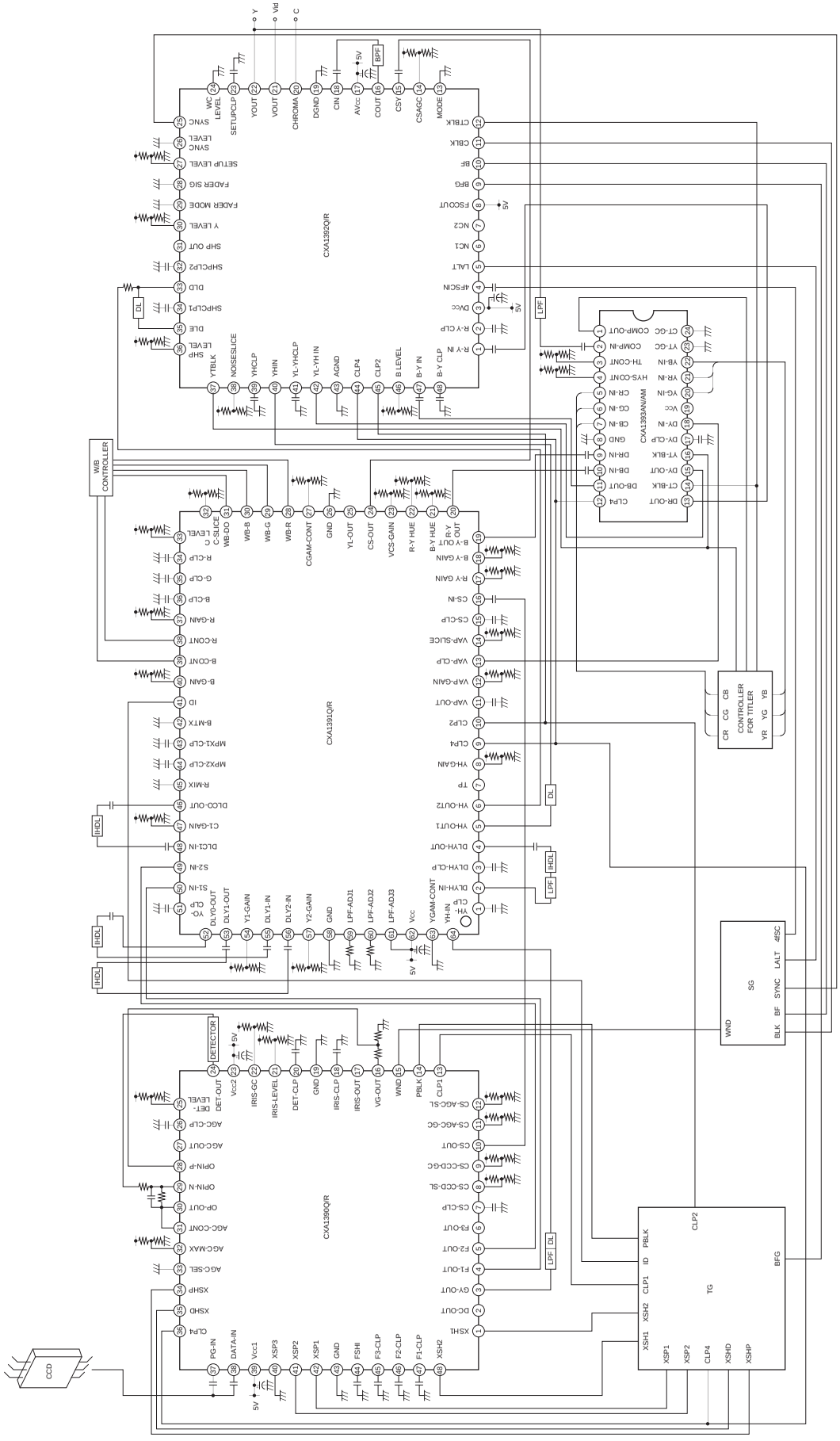
Burst level supply voltage characteristics (NTSC pulse mode) Burst level = V_{CC}



CIN → Chroma gain supply voltage characteristics



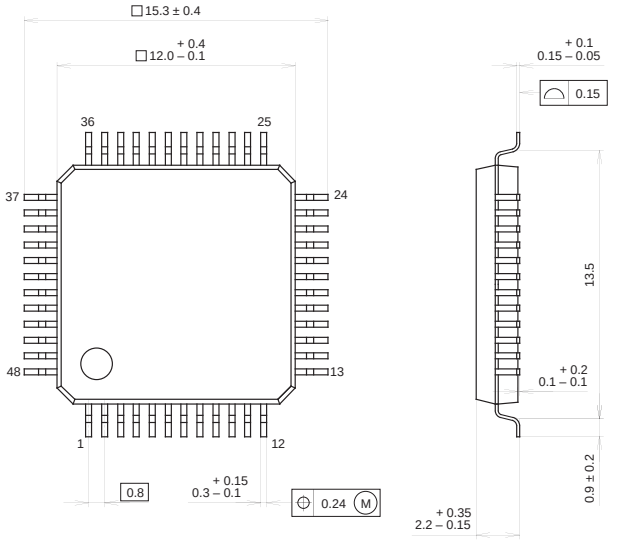
CXA1390 Series System Diagram



Package Outline Unit: mm

CXA1392Q

48PIN QFP (PLASTIC)



PACKAGE STRUCTURE

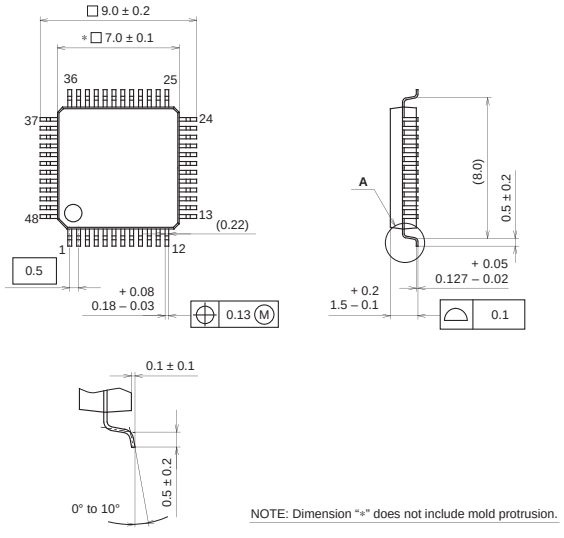
SONY CODE	QFP-48P-L04
EIAJ CODE	QFP048-P-1212
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.7g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).

CXA1392R

48PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

DETAIL **A**

PACKAGE STRUCTURE

SONY CODE	LQFP-48P-L01
EIAJ CODE	LQFP048-P-0707
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g