ADMtek Incorporated

ADM 8511

Pegasus II **USB / Fast Ethernet with MII Interface**

General Description

The ADM 8511, USB based chipset, provides desktop, notebook and computer peripherial with greater connectivity to ethernet and home network. In the meantime, the ADM 8511 also combined a low power and small package design which is ideal for power and space constrained environment. Then, it can reduced the external component BOM cost to a minimum.

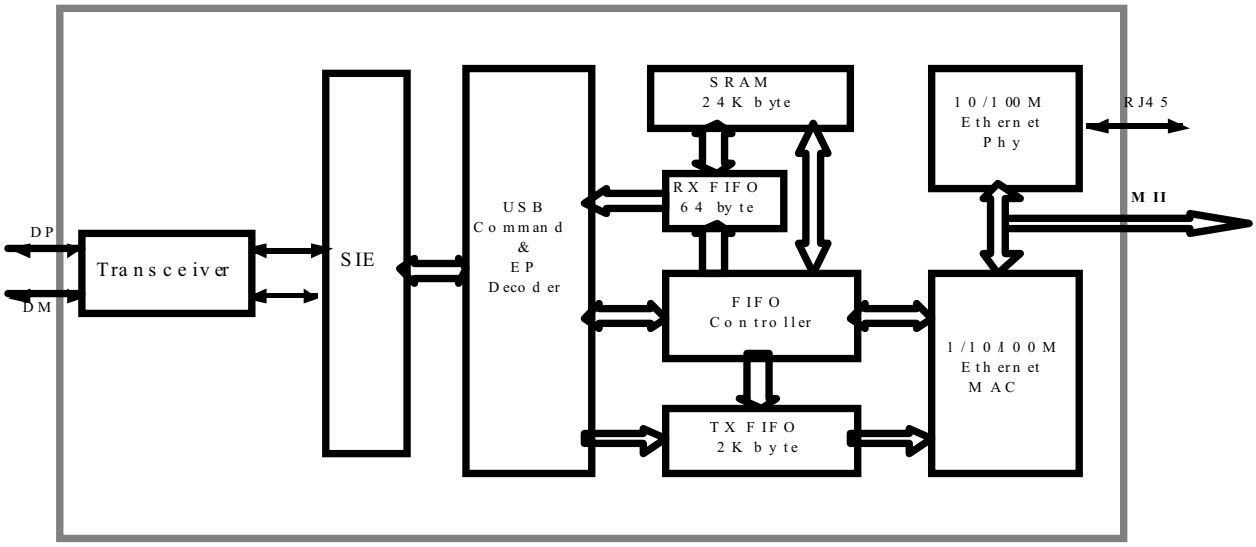
The ADM 8511 device combines a on-chip USB command & EP decoder used for USB interface through SIE (Series Interface Engine) , FIFO controller with 24 K SRAM, 64 byte and 2K byte buffers, 10/100 Mbps ethernet physical layer (PHY) and 10M HomePNA interface 10M8. The10M HomePNA interface is MII is the same as the ethernet MAC interface. The ADM8511 is fully compliant with the IEEE 802.3u

The ADM 8511 is capable of providing a easy, universal connectivity to computer peripherals with USB. The transfer rate of USB interface is 12 Mbps belonging to a high speed USB device. The ADM 8511 supports all USB commands, 4 endpoints and suspend/resume function.

The ADM 8511's LAN PHY supports 100 Base TX (100 Mbps mode) and 10 Base T (10Mbps mode) full-duplex operations. It uses the auto-negotiation function to optimize the network traffic and the built-in 24K bytes SRAM for receiving buffer, especially for 100Mbps. Through FIFO controller, data can communicate influ rently between buffers and external device. To obtain the better signal quality, the PHY provides wave-shaper, filter and adaptive equalizer to reach. By using diagnostic mechanism (loop-back mode), the data correctness will be increased. The Lan PHY supports external transmit/receive transformer turn ratio 1:1. The ADM8511 chipset can be programmed MAC analysis and provides MII interface for external PHY, such as 10M8 interface for 10Mbps HomePNA. In system application, EEPROM is essential that it needs to load device ID , vendor ID automatically. So for ADM 8511, serial interface is applied for EEPROM communication including read/write function. Furthermore, system statuses are reported by some LED pins.

ADM 8511 is ideally suited for USB adapter and intelligent networked peripheral design. By fiber media, ADM 8511 can associate with fiber tranceiver & PHY through MII interface to network in fiber network. In HomePAN application, ADM 8511 can provide 10M8 (MII interface)associated with external 10M Home PHY for 10Mbps network. ADM 8511 can't apply only in LAN(Local Area Network) but also in WAN(Wide Area Network), such as xDSL, Cable Modem, and router … e.t.c.. In IA (Information Appliance) application, Set-Top box is an example of ADM 8511 application. ADM 8511 also provide serial interface for

Block Diagram



EEPROM storing default values, e.g. vendor ID, Product ID, …e.t.c.(EEPROM Access Program). Specially, ADM 8511 can be tested by test program (MFG) in the less time for mass production of system board level. This chip provides 3.3V/5V I/Otolerance, and 100 pin LQFP package

In software, ADM 8511 provides a fully software support, NDIS 5 driver, Linux driver, WinCE 4.0, EEPROM burn-in program and MFG program. The NDIS 5 and Linux drivers are windows netware drivers. EEPROM burn-in program is convenient for customers to implement. The MFG program is a powerful tool in mass – production.

Features

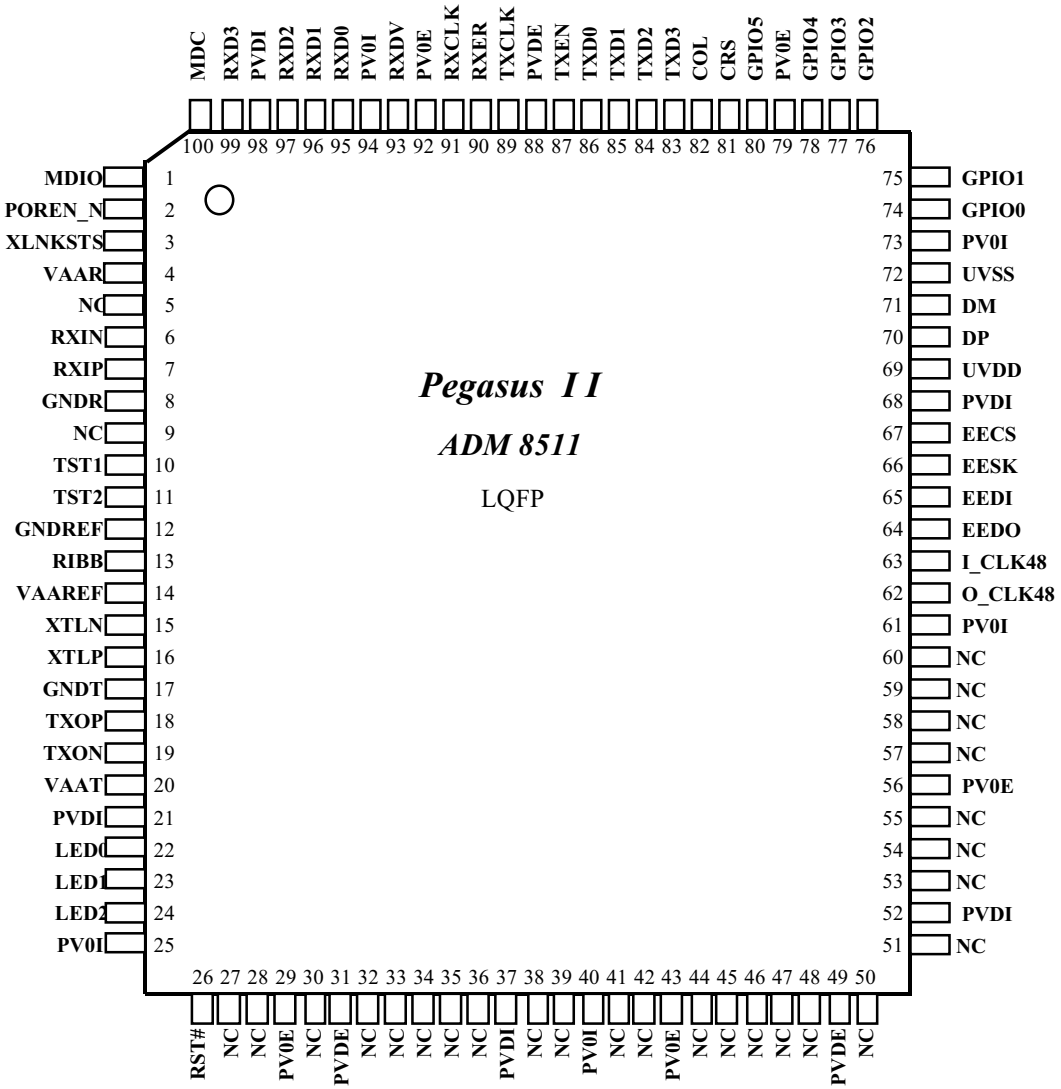
- **Industry Standard**
  - IEEE802.3u 100BASE-TX and IEEE802.3 10BASE-T compliant
  - Support for IEEE 802.3x flow control
  - IEEE802.3u Auto-Negotiation support for 10BASE-T and 100BASE-TX
  - USB specification 1.0 and 1.1 compliant
- **USB I/F**
  - Full-Speed USB Device
  - Supports 1 USB configuration and 1 interface
  - Supports all USB standard commands
  - Supports two vendor specific commands
  - Supports USB Suspend/Resume detection logic
  - Supports 4 endpoints: 1 control endpoint with maximum 8-byte packet, 1 bulk IN endpoint with maximum 64-byte packet, 1 bulk OUT endpoint with maximum 64-byte packet and 1 interrupt IN endpoint with maximum 8-byte packet
- **MAC/Phy**
  - Integrates the whole physical layer functions of 100BASE-TX and 10BASE-T by using phy address 1
  - Be programmed to isolate the internal PHY, the I/F to external PHY could be either IEEE 802.3 MII (10M8 for HomePNA 2.0). Supports configurable threshold for transmitting PAUSE frame
  - Supports wakeup frame, link status change and magic packet wake-up
  - Provides full-duplex operation on both 100Mbps and 10Mbps Ethernet modes
  - Provides Auto-negotiation(NWAY) function of full/half duplex operation for both 10/100 Mbps
  - Provides transmit wave-shaper, receive filters, and adaptive equalizer
  - Provides MLT-3 transceiver with DC restoration for Base-Line Wander compensation
  - Provides MAC and Transceiver loop-back modes for diagnostic
  - Supports external transmit transformer with turn ratio 1:1
  - Supports external receive transformer with turn ratio 1:1
- **EEPROM I/F**
  - Provides serial interface for read/write 93C46 EEPROM
  - Automatically loads device ID, vendor ID from EEPROM after power-on reset
- **FIFO**
  - Supports internal 2K bytes SRAM for transmission
  - Supports internal 24K bytes synchronous SRAM for receiving.
  - Supports “receive 32 packets” or “receive 16 packets” queue in the receive buffer
- **LED Display**
  - Provide LEDs many display mode
- **Miscellaneous**
  - Support 6 GPIO pins
  - Provides 100-pin LQFP package
  - 3.3V power supply with 5V/3.3V I/O tolerance

- **LAN Driver Support**
  - Windows Networks : NDIS 5.0
  - Linux
  - WinCE 4.0
- **Utility**
  - EEPROM burn-in program
  - MFG testing program

Revision History

Release Date	Revision	Description
July 2000	0.1	Draft product spec for review
September 2000	1.0	Rearrange
October 2000	2.0	add appendix
December 2000	2.01	P.62 Appendix 5/item 7/item b/item ii/ TXER change to RXER
December 2000	2.02	Add max. power consumption P.1 I^2C change to serial
April 2002	2.04	Add Appendix 1 / item 3/ item (6) No connection in external SRAM interface. They are pin 27,28,30,32~36,38,39,41,42,44~48,50,51,53~55,57~60 No connection in test pins. They are pin 5,9. Power consumption change at P.38 Add LED operation mode at P.11 Add EEPROM 0B[7:6] for LED mode setting at P.51 Remove all of HomePNA(1M8) description Remove all of external SRAM interface description Remove Phy transceiver reg. After reg. 6 Modify Phy transceiver reg. 0~6 description Modify EEPROM content in EEPROM example Add “25MHz crystal and Ribb still need” in Appendix 5

Pin Assignment Diagram



- **Pin Description**

Pin Name	Pin #	Type	Pin Description
● **Host Interface**			
I_CLK48	63	I	48Mhz Clock Input from crystal or oscillator.
O_CLK48	62	O	Output for crystal.
RST#	26	I	External Hardware Reset Input
DM	71	I/O	USB Data Minus pin.
DP	70	I/O	USB Data Plus pin.
● **MII Interface (Program `ADM8511` as MAC-only mode, set 81h[4:2]=001b and 01h bit 2 = 0)**			
COL	82	I	**Collision Detected** This signal is asserted high asynchronously by the external physical unit upon detection of a collision on the medium. It will remain asserted as long as the collision condition persists.
CRS	81	I	**Carrier Sense** This signal is asserted high asynchronously by the external physical unit upon detection of a non-idle medium.
MDC	100	O	**Management Data Clock** Clock signal with a maximum rate of 2.5MHz used to transfer management data for the external PMD on the MDIO pin.
MDIO	1	I/O	**Management Data I/O** Bi-directional signal used to transfer management information for the external PMD. Requires external 1.5k pull-up resistor.
RXCLK	91	I	**Receive Clock** A continuous clock that is recovered from the incoming data. During 100Mb/s operation RXCLK is 25MHz, during 10Mb/s this is 2.5MHz and during 1Mb/s operation this is 0.25MHz.

RXD[3:0]	95-97, 99	I	**Receive Data** This is a group of 4 data signals aligned on nibble boundary which are driven synchronous to the RXCLK by the external physical unit. RXD[3] is the most significant bit and RXD[0] is the least significant bit.
RXDV	93	I	Receive Data Valid This indicates that the external physical unit is presenting recovered and decoded nibbles on the RXD[3:0] and that RXCLK is synchronous to the recovered data.
RXER	90	I	**Receive Error** This signal is asserted high synchronously by the external physical unit whenever it detects a media error and RXDV is asserted. If no used, it should be grounded, e.g. isolate internal phy and use external phy. However, if the external phy has RXER pin, the RXER of ADM8511 should connect to this RXER of the external phy.
TXCLK	89	I	**Transmit Clock** A continuous clock that is source by the physical layer. During 100 Mb/s operation this is 25MHz ±100 ppm. During 10 Mb/s operation this clock is 2.5MHz ±100 ppm. During 1 Mb/s operation this clock is 0.25MHz ±100 ppm.
TXD[3:0]	83,84, 85,86	O	**Transmit Data** This is a group of 4 data signals which driven synchronously to the TXCLK for transmission to the external physical unit. TXD[3] is the most significant bit and TXD[0] is the least significant bit.
TXEN	87	O	**Transmit Enable** This signal is synchronous to TXCLK and provides precise framing for data carried on TXD[3:0]. It is asserted when TX[3:0] contains valid data to be transmitted. Require external pull-down resistor 4.7K if external phy is used

XLNKSTS	3	I	**Link Status Indication** Link status indication External PHY reports link status information to system and level change trigger. Pull-down to low if external phy is used.
● **Physical Interface**			
XTLP, XTLN	16, 15	I	Crystal inputs. To be connected to a 25MHz crystal.
RXIN, RXIP	6, 7	I	The differential receive inputs of 100BASE-TX or 10BASE-T, these pins directly input from Magnetic.
TXOP, TXON	18, 19	O	The differential Transmit outputs of 100BASE-TX or 10BASE-T, these pins directly output to Magnetic.
RIBB	13	I	Reference Bias Resistor. To be tied to an external 10.0K (1%) resistor which should be connected to the analog ground at the other end.
TST1, TST2	10, 11	O	Test pin
● **LED display**			
LED0	22	O	LED display for 100M b/s or 10M b/s speed. Active low indicates 100Base-TX, active high indicates 10 BaseT. 2mA @5V
LED1	23	O	LED display for link and activity status. Active low when link is established. 2mA @5V
LED2	24	O	LED display for Full Duplex or Collision status. Active low indicates full duplex, high indicates collision in half duplex. 2mA @5V

Note
The LED interface is EEPROM-programmable, 2 bit EEPROM control bit, Address 0B[7:6] at EEPROM, is used to select LED mode, the default setting are:
(1) LED0: 100Mbps(on, drive '0') or 10Mbps(off, drive '1')
(2) LED1: link (keeps on when link ok) or activity (blink with 10Hz when Pegasus II is receiving or transmitting but not collision)
(3) LED2: full duplex (keeps on when in full duplex mode) or collision (blink with 20Hz when colliding)
(4) All LED pins will be tri-state when using external PHY (offset 81h with bit[4:2] = 3'b001)

Mapping between LED action and EEPROM 0B[7:6] setting:

EEPROM 0B [7:6]	LED	Action
0,0	LED0	10/100(OFF/ON)
	LED1	LINK/ACTIVITY (ON / Flash)
	LED2	FULL DUP/COL (ON / Flash)
0,1	LED0	ACTIVITY when LINK (Flash)
	LED1	LINK 10(ON)
	LED2	LINK 100(ON
1,0	LED0	On: 100M, Off :10M
	LED1	Flash : Activity
	LED2	Flash : Liink
1,1	LED0	On : 10M Link, Flash : 10M Activity
	LED1	On : 100M Link, Flash : 100M Activity
	LED2	Full

- **No connection**

NC	48, 50, 51, 53, 54, 55, 57, 58, 30, 32, 35, 33, 59, 28, 60		No connection
NC	47, 46, 45, 44, 42, 41, 39, 38		No connection

NC	36		No connection
NC	34		No connection
NC	27		No connection
● **EEPROM Interface**			
EECS	67	O	**EEPROM Chip Select** This enables the EEPROM during loading of the Ethernet configuration data.
EEDI	65	O	**EEPROM Data In** The MAC will use this pin to serially write opcodes, addresses and data into the serial EEPROM.
EEDO	64	I	**EEPROM Data Out** The MAC will read the contents of the EEPROM serially through this pin.
EESK	66	O	**EEPROM Clock** After reset, the MAC if configured, will read the contents of the EEPROM using EESK, EEDO, and EEDI. This pin provides the clock for the EEPROM.
● **Miscellaneous**			
GPIO[5:0]	80, 78, 77, 76, 75, 74	I/O	These pins are used as general purpose Input/Output pins and offset 0A[1] = 0 in EEPROM. Default is internal pull-low 4mA@5V
POREN_N	2	I	Internal Power On Reset Logic Enable. Default is enable and internal pull - low. When external hardware reset is used, this pin should be connected to Vcc via 4.7k resistor.
● **Power Pins**			
PVDI	21, 37, 52, 68, 98	P	3.3v power supply for core.
PVDE	31, 49, 88	P	3.3v power supply for pads.

PV0I	25, 40, 61, 73, 94	P	Ground for PVDI
PV0E	29, 43, 56, 79, 92	P	Ground for PVDE
UVDD	69	P	3.3v power supply for USB transceiver
UVSS	72	P	Ground for UVDD
VAAR, VAAREF, VAAT	4, 14, 20	P	Analog Power Pins, 3.3v
GNDR, GNDREF, GNDT	8, 12, 17	P	Analog Ground Pins

Function Descriptions

- **USB Interface**

  USB is likely solution any time you want to use a computer to communication with devices outside the computer. The interface is suitable for one-of-kind and small-scale designs as well as mass-produced, standard peripheral. The benefits to USB are ease of use, fast and reliable data transfers, flexibility, low cost and power conservation.

  SIE

  SIE (Serial Interface Engine) is to control USB communications and check USB protocol, then transfer protocol to EP decoder. The SIE and USB transceivers, which provide the hardware interface to the USB cable, together comprise the USB engine.

  USB Command & EP Decoder

  The detail description is in Appendix 4.

- **MAC Interface**

  MII

  The Media Independent Interface (MII) is an 18 wire MAC/Phy interface described in 802.3u. The purpose of the interface is to allow MAC layer devices to attach to a variety of Physical Layer devices through a common interface. MII operates at either 100Mbps or 10Mbps, dependant on the speed of the Physical Layer. With clocks running at either 25 MHz or 2.5 MHz, 4 bit data is clocked between the MAC and Phy, synchronous with Enable and Error signals.

  On receipt of valid data from the wire interface, RX_DV will go active signaling to the MAC that the valid data will be presented on the RXD[3:0] pins at the speed of the RX_CLK.

  On transmission of data from the MAC, TX_EN is presented to the phy indicating the presence of valid data on TXD[3:0]. TXD[3:0] are sampled by the phy synchronous to TX_CLK during the time that TX_EN is valid.

  Adaptive Equalizer

  The amplitude and phase distortion from cable cause inter-symbol interference (ISI) which makes clock and data recovery difficult. The adaptive equalizer is designed to closely match the inverse transfer function of the twisted-pairs cable. The equalizer has the ability to change its equalizer frequency response according to the cable length. The

equalizer will tune itself automatically fo any cable, compensating for the amplitude and phase distortion introduced by the cable.

LEDs

Individual LED output are available to indicate Speed, Duplex, Collision, Transmit, and Link. These multi-function pins are inputs during reset and LED output pins thereafter. The level of these pins during reset determines their active output states. If a multi-function pin is pulled up during reset to select a particular function, then that LED output would become active low, and the LED circuit must be designed accordingly, and vice versa.

Jabber and SQE

After the MAC transmitter exceeds the jabber timer, the transmit and loopback functions will be disable and COL signal get asserted. After TX_EN goes low for more than 500ms, the TP transmitter will reactivate and COL gets de-asserted. Setting Jabber Disable will disable the jabber function.

When the SQE test is enabled, a COL pulse is asserted after each transmitted packet. SQE is enabled in 10Base-T by default.

Auto Polarity

Certain cable plants have crossed wiring on the twisted pairs; the reversal of TXIN and TXIP. Under normal circumstances this would cause the receive circuitry to reject all data. When the Auto Polarity Disable bit is cleared, the Phy has the ability to detect the fact that either 8 NLPs (normal link pulse) or a burst of FLPs are inverted and automatically reverse the receiver's polarity. The polarity state is store is atoreed in the Reverse Polarity bit.

Auto-Negotiation

It provides a linked device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the link, determine common abilities, and configure for joint operation. Auto-Negotiation is performed out-of-band using a pulse code sequence that is compatible with the 10BASE-T link integrity test sequence.

Baseline Wander Compensation

The 100BASE-TX data stream is not always DC balanced. The transformer blocks the DC components of the incoming signal, thus the DC offset of the differential receive inputs can drift. The shifting of the signal level, coupled with non-zero rise and fall times of the serial stream can cause pulse-width distortion. This creates jitter and possible increase in the bit error rates. Therefore, a DC restoration circuit is needed to compensate for the attenuation of the DC component. Unlike the traditional implementation, the circuit does not need the feedback information from the slicer or the clock recovery circuit. The design simplifies the circuit design. In 10BASE-T, the baseline wander correction circuit is not required.

- **FIFO Controller**

FIFO Controller in receive path is in charge of:

(1) Store received Ethernet packets to SRAM (internal 24Kbyte) and total 32 (or 16) packets can be stored to SRAM. If more than maximum packet counts are received or total packet size is more than 32K (or 24K for internal SRAM) bytes, the subsequent coming Ethernet packet will be discarded.

(2) FIFO controller will load data from SRAM to internal RX FIFO then inform EP Decoder that 64-byte data or a packet is ready in RX FIFO. Before FIFO controller inform this, any USB access to bulk IN endpoint will return NAK. This is to maintain the data transfer on USB bus via bulk IN transfer is continuous, thus a 64-byte internal RX FIFO is needed.

(3) If an Ethernet packet is being received and loading into SRAM while FIFO Controller is moving data from SRAM to internal RX FIFO, writing the Ethernet packet to SRAM will get the higher priority.

FIFO Controller in transmit path is in charge of:

(1) Store each individual USB packet to internal TX FIFO. When EP decoder informs end of packet, a complete Ethernet packet is stored in TX FIFO. FIFO Controller then informs MAC to transmit this packet.

(2) Total 4 Ethernet packets can be stored in TX FIFO. If all 4 Ethernet packet are stored in TX FIFO or total packet size is more than 2K bytes, FIFO Controller will inform EP Decoder that TX FIFO is full and EP Decoder will return NAK if accessing to bulk OUT endpoint is invoked. Thus additional USB packet won't be written into TX FIFO until TX FIFO has free space.

- **TX FIFO and RX FIFO**

  RX FIFO is a one-port 64-byte FIFO and TX FIFO is a two-port 2K-byte FIFO.

- **1/10/100 Ethernet MAC**

  The MAC controller takes in charge of
  (1) Generate CRC then transmit Ethernet packet.
  (2) Check CRC for received packet CRC, filter the received packets.
  (3) Polling PHY status.
  (4) Magic packet detection.
  (5) Automatically transmit PAUSE frame when received status meets the flow control criteria.
  (6) Late collision transmit packets will be discarded.

- **10/100M Ethernet PHY**

  The internal Ethernet PHY is compliant to IEEE 802.3u 100BASE-TX and IEEE802.3 10BASE-T. It provides the whole physical layer functions for both 10M and 100M Ethernet speed. The internal PHY can be isolated by programming register offset 7Bh, bit 1.

- ***Register Descriptions***
  - **System Register Table**

Offset	Register
00-02h	Ethernet control registers
03-07h	Reserved
08-0Fh	Multicast address table registers
10-15h	Ethernet ID registers
16-17h	Reserved
18-19h	Pause_timer registers
1Ah	Receive packet number based flow control register
1Bh	Occupied receive FIFO based flow control register
1Ch	EP1 control register
1Dh	RX FIFO control register
1Eh	BIST control register
1Fh	Reserved
20h	EEPROM offset register
21-22h	EEPROM data registers
23h	EEPROM access control register
24h	Reserved
25h	PHY address register
26-27h	PHY data registers
28h	PHY access control register
29h	Reserved
2Ah	USB status register
2B-2Ch	Ethernet transmit status registers
2Dh	Ethernet receive status register
2E-2Fh	Ethernet receive lost packet count register
30-3Fh	Wakeup frame 0 mask registers
40h	Wakeup frame0 offset register
41-42h	Wakeup frame0 CRC registers
43-47h	Reserved
48-57h	Wakeup frame 1 mask registers
58h	Wakeup frame 1 offset register
59-5Ah	Wakeup frame 1 CRC registers
5B-5Fh	Reserved
60-6Fh	Wakeup frame 2 mask registers
70h	Wakeup frame 2 offset register
71-72h	Wakeup frame 2 CRC registers
73-77h	Reserved
78h	Wakeup control register
79h	Reserved
7Ah	Wakeup status register
7Bh	Internal PHY control register
7Ch	GPIO[5:4] control register
7Dh	Reserved
7Eh	GPIO[1:0] control register
7Fh	GPIO[3:2] control register
80h	TEST register
81h	Test mode register
82-FFh	Reserved

- **Offset 00h: Ethernet control_0**

Bit	Field	HW Access	SW access	Default value	Description
7	tx_en	R	R/W	0	Enable Ethernet transmission.
6	rx_en	R	R/W	0	Enable Ethernet receive.
5	rx_flowctl_en	R	R/W	0	Enable receive pause frame.
4	wakeon_en	R	R/W	0	Enable wake-on-LAN mode.
3	rxstatus_append	R	R/W	1	Enable status append at the end of received packet.
2	stop_back_off	R	R/W	0	1: back-off counter stop when carrier is active and resume when carrier drop. 0: back-off counter isn't affected by carrier.
1	rx_multicast_all	R	R/W	0	Receive all multicast packet
0	rx_crc_sent	R	R/W	1	Include CRC in receive packet.

- **Offset 01h: Ethernet control_1**

Bit	Field	HW access	SW access	Default value	Description
7	reserved				
6	Reserved			0	
5	full_duplex	R	R/W	0	1: full-duplex mode. 0: half-duplex mode.
4	10mode	R	R/W	0	0: 10Base-T mode. 1: 100Base-T mode.
3	reset_mac	R	R/W	0	Reset MAC, After write 1, HW will clear this bit after MAC reset.
2	homelan_mode	R	R/W	0	0: MII I/F to external PHY
0-1	reserved				

- **Offset 02h: Ethernet control_2**

Bit	Field	HW access	SW access	Default value	Description
7-6	reserved				
5	load EEPROM start	R	R/W	0	When this bit is written with 1, HW will start to load EEPROM.
4	EEPROM write enable/disable	R	R/W	0	1: EEPROM write command 0: EEPROM write enable/disable command
3	loop_back	R	R/W	0	Enable MAC loop back mode
2	promiscuous	R	R/W	0	1: receive any packet. 0: receive packets which pass the address filter.
1	rx_bad_pkt	R	R/W	0	1: receive bad packets which pass the address filter. 0: filter all bad packet
0	Ep3_rd_clr/	R	R/W	0	1: Once EP3 is accessed, those registers(2B-2F, 7A) will be cleared. 0: Access EP3, no effect to those registers.

- **Offset 03-07h: reserved**

- **Multicast address**

offset	Bit	Field	HW access	SW access	Default value	Description
08h	7-0	Multicast0	R	R/W	0	Multicast address byte 0 (hash table[7:0]).
09h	7-0	Multicast1	R	R/W	0	Multicast address byte 1 (hash table[15:8]).
0Ah	7-0	Multicast2	R	R/W	0	Multicast address byte 2 (hash table[23:16]).
0Bh	7-0	Multicast3	R	R/W	0	Multicast address byte 3 (hash table[31:24]).
0Ch	7-0	Multicast4	R	R/W	0	Multicast address byte 4 (hash table[39:32]).
0Dh	7-0	Multicast5	R	R/W	0	Multicast address byte 5 (hash table[47:40]).
0Eh	7-0	Multicast6	R	R/W	0	Multicast address byte 6 (hash table[55:48]).
0Fh	7-0	Multicast7	R	R/W	0	Multicast address byte 7 (hash table[63:56]).

- **Ethernet ID**

Offset	Bit	Field	HW access	SW access	Default value	Description
10h	7-0	Etherid0	R/W	R/W	0	The 1st byte of ethernet ID is automatically loaded from EEPROM after HW reset.
11h	7-0	Etherid1	R/W	R/W	0	The 2nd byte of ethernet ID.
12h	7-0	Etherid2	R/W	R/W	0	The 3rd byte of ethernet ID.
13h	7-0	Etherid3	R/W	R/W	0	The 4th byte of ethernet ID.
14h	7-0	Etherid4	R/W	R/W	0	The 5th byte of ethernet ID.
15h	7-0	Etherid5	R/W	R/W	0	The 6th byte of ethernet ID.

- **Offset 16-17h: reserved**

- **Offset 18h: pause_timer low**

Bit	Field	HW access	SW access	Default value	Description
7-0	pause_timer	R	R/W	0F	The [11:4] of pause time in the PAUSE frame.

- **Offset 19h: reserved**

- **Offset 1Ah: receive packet number based flow control**

Bit	Field	HW access	SW access	Default value	Description
7	reserved				
6-1	pkt_no	R	R/W	6'h0F	This field specifies the threshold for transmitting the PAUSE frame. As the received packet number is more than or equal to this field, the PAUSE frame is sent automatically by HW.
0	flowctl_pkt	R	R/W	0	Enable pause frame transmission bases on receive packet number.

- **Offset 1Bh: occupied receive FIFO based flow control**

Bit	Field	HW access	SW access	Default value	Description
7	reserved				
6-1	rxsize	R	R/W	6'h0F	This field specifies the K byte threshold for transmitting the PAUSE frame. As the received FIFO is occupied than or equal to this field, the PAUSE frame is sent automatically by HW. If this field =2, as receive FIFO is occupied more than or equal to 2K byte, the PAUSE frame is transmitted.
0	flowctl_rxsize	R	R/W	0	Enable pause frame transmission bases on occupied receive FIFO size.

- **Offset 1Ch: EP1 Control**

Bit	Field	HW access	SW access	Default value	Description
7	ep1_send0_en	R	R/W	0	1: enable EP1 send 1-byte 00 when more than frame_interval's NAK is received 0: disable EP1 send 1-byte 00 function
6-5	test_itvl_a	R	R/W	2'd0	This value are used for internal test mode.
4-0	test_itvl_b	R	R/W	5'd0	This value are used for internal test mode.

- **Offset 1Dh: RX FIFO Control**

Bit	Field	HW Access	SW access	Default value	Description
7-2	reserved				
1	reserved			0	0: supports internal 24K-byte SRAM
0	rx32pkt	R	R/W	0	1: support maximum 32 packets in receive FIFO 0: support maximum 16 packets in receive FIFO

- **Offset 1Eh: BIST control**

Bit	Field	HW Access	SW access	Default value	Description
7-3	reserved				
2	bist_result	R/W	R	0	This bit indicated the bist result and is valid when "bist_test_done" is '1'. This bit also reflects the value of "pass_or_fail" signal in BIST module. 1: pass 0: fail
1	bist_test_done	R/W	R	0	This bit indicates the completion of bist. The bist completes if this bit is '1'. This bit also reflects the value of "test_done" signal in BIST module.
0	bist_en_n	R	R/W	1	This bit enable the BIST function and also drives the " reset" signal in BIST module. 1: disable BIST function 0: enable BIST function

- **Offset 20h: EEPROM offset**

Bit	Field	HW access	SW access	Default value	Description
7-6	reserved				
5-0	rom_offset	R	R/W	0	SW sets this register when access to EEPROM.

- **Offset 21h: EEPROM data low**

Bit	Field	HW access	SW access	Default value	Description
7-0	romdata_lo	R/W	R/W	0	SW sets this register when writes to EEPROM. HW sets this register when read data from EEPROM.

- **Offset 22h: EEPROM data high**

Bit	Field	HW access	SW access	Default value	Description
7-0	romdata_hi	R/W	R/W	0	SW sets this register when writes to EEPROM. HW sets this register when reads data from EEPROM.

- **Offset 23h: EEPROM access control**

Bit	Field	HW access	SW access	Default value	Description
7-3	reserved				
2	done	R/W	R/W	0	Set by HW to indicate successful completion of EEPROM access. Clear by SW when initiate a new access to EEPROM
1	rd_eeprom	R	R/W	0	Set by SW to initiate a read access to EEPROM. SW sets this bit after it well setting the rom_offset.
0	wr_eeprom	R	R/W	0	Set by SW to initiate a write access to EEPROM. SW set this bit after it well setting the rom_offset, romdata_lo and romdata_hi.

- **Offset 24h: reserved**

- **Offset 25h: PHY address**

Bit	Field	HW access	SW access	Default value	Description
7-5	reserved				
4-0	phy_addr	R	R/W	0	MII PHY address.

- **Offset 26h: PHY data low**

Bit	Field	HW access	SW access	Default value	Description
7-0	phydata_low	R/W	R/W	0	SW set this register when write to phy registers. HW set this register when read data from PHY register.

- **Offset 27h: PHY data high**

Bit	Field	HW access	SW access	Default value	Description
7-0	phydata_high	R/W	R/W	0	SW set this register when write to phy registers. HW set this register when read data from PHY register.

- **Offset 28h: PHY access control**

Bit	Field	HW access	SW access	Default value	Description
7	done	R/W	R/W	0	Set by HW to indicate successful completion of PHY access. Clear by SW when initiate a new access to PHY.
6	rd_phy	R	R/W	0	Set by SW to initiate a read access to PHY register. SW set this bit after it well setting the phy_addr and phyreg_addr.
5	wr_phy	R	R/W	0	Set by SW to initiate a write access to PHY register. SW set this bit after it well setting the phy_addr, phyreg_addr and phyreg_data.
4-0	phyreg_addr	R	R/W	0	PHY register address.

- **Offset 29h: reserved**

- **Offset 2Ah: usb bus status**

Bit	Field	HW access	SW access	Default value	Description
7-2	reserved				
1	usb_resume	R/W	R/W	0	Set by HW to indicate usb bus in resume state. Clear by SW read this register.
0	usb_suspend	R/W	R/W	0	Set by HW to indicate usb bus in suspend state. Clear by SW read this register.

- **Offset 2Bh: transmit status_1**

Bit	Field	HW access	SW access	Default value	Description
7	txunderrun	R/W	R	0	Set by HW to indicate tx underrun error. Clear by SW read this register or after EP3 is accessed.
6	excessive_col	R/W	R	0	Set by HW to indicate excessive collision. Clear by SW read this register or after EP3 is accessed.
5	late_col	R/W	R	0	Set by HW to indicate late collision error. Clear by SW read this register or after EP3 is accessed.
4	no_carrier	R/W	R	0	Set by HW to indicate no carrier. Clear by SW read this register or after EP3 is accessed.
3	loss_carrier	R/W	R	0	Set by HW to indicate carrier loss. Clear by SW read this register or after EP3 is accessed.
2	jabber_timeout	R/W	R	0	Set by HW to indicate jabber time out. Clear by SW read this register or after EP3 is accessed.
1-0	reserved				

- **Offset 2Ch: transmit status_2**

Bit	Field	HW access	SW access	Default value	Description
7	txfifo_full	R/W	R	0	Set by HW to indicate tx fifo full. Clear by SW read this register or after EP3 is accessed.
6	txfifo_empty	R/W	R	0	Set by HW to indicate tx fifo empty. Clear by SW read this register or after EP3 is accessed.
5-4	reserved				
3-0	txpkt_cnt	R/W	R	0	Set by HW to indicate Ethernet transmit packet count every interrupt EP polling. If more than 15 packets have been transmitted, this value will keep as 15. Clear by SW read or after EP3 is accessed.

- **Offset 2Dh: receive status**

Bit	Field	HW access	SW access	Default value	Description
7-2	reserved				
1	rx_pause	R/W	R/W	0	Set by HW to indicate a PAUSE frame is received. Clear by SW read this register or after EP3 is accessed.
0	rx_overflow	R/W	R	0	Clear by SW read this register or after EP3 is accessed.

- **Offset 2Eh: receive lost packet count high**

Bit	Field	HW access	SW access	Default value	Description
7	Lostpkt_	R/W	R/W	0	
6-0	rx_lostpkt	R/W	R/W	0	The [14:8] of lost packet counts due to receive FIFO overflow. Clear by SW read this register or after EP3 is accessed.

- **Offset 2Eh: receive lost packet count low**

Bit	Field	HW access	SW access	Default value	Description
7-0	rx_lostpkt	R/W	R/W	0	The [7:0] of lost packet counts due to receive FIFO overflow. Clear by SW read this register or after EP3 is accessed.

- **Wake-up frames**

Offset	Bit	Field	HW access	SW access	Default value	Description
30-3Fh		f0_mask				The 128 mask bits for fram0.
40h	7-0	f0_offset	R	R/W	0	Offset for wakeup frame0.
41h	7-0	f0_crc_low	R	R/W	0	The low byte of CRC16 match for frame 0.

42h	7-0	f0_crc_hi	R	R/W	0	The high byte of CRC16 match for frame 0.
43-47h		reserved				
48-57h		f1_mask				The 128 mask bits for fram1.
58h	7-0	f1_offset	R	R/W	0	Offset for wakeup frame1.
59h	7-0	f1_crc_low	R	R/W	0	The low byte of CRC16 match for frame 1.
5Ah	7-0	f1_crc_hi	R	R/W	0	The high byte of CRC16 match for frame 1.
5B-5Fh		reserved				
60-6Fh		f2_mask				The 128 mask bits for fram2.
70h	7-0	f2_offset	R	R/W	0	Offset for wakeup frame2.
71h	7-0	f2_crc_low	R	R/W	0	The low byte of CRC16 match for frame 2.
72h	7-0	f2_crc_hi	R	R/W	0	The high byte of CRC16 match for frame 2.
73-77h		reserved				

- **Offset 78h: wake-up control**

Bit	Field	HW access	SW access	Default value	Description
7	mgcpkt_en	R	R/W	0	Set by SW to enable magic packet wakeup function.
6	link_en	R	R/W	0	Set by SW to enable link status wakeup function.
5	wakeframe0_en	R	R/W	0	Set by SW to enable wakeup frame0 wakeup function.
4	wakeframe1_en	R	R/W	0	Set by SW to enable wakeup frame1 wakeup function.
3	wakeframe2_en	R	R/W	0	Set by SW to enable wakeup frame2 wakeup function.
2	crc16type	R	R/W	1	0: CRC-16 initial contents = 0000h 1: CRC-16 initial contents = ffffh
1-0	reserved				

- **Offset 79h: reserved**

- **Offset 7Ah: wake-up status**

Bit	Field	HW access	SW access	Default value	Description
7	rx_mgcpkt	R/W	R	0	Set by HW when receive a magic packet. Clear by SW read this register.
6	link_wake	R/W	R	0	Set by HW when link status change. Clear by SW read this register.
5	rx_wakeframe	R/W	R	0	Set by HW when receive a wakeup frame. Clear by SW read this register.
4-1	reserved				
0	link_sts	R/W	R	0	Indicate the current link status, 1 for link on, 0 for link off.

- **Offset 7B: internal PHY control**

Bit	Field	HW access	SW access	Default value	Description
7-2	reserved				
1	power_down_phy	R	R/W	0	0: power down internal 10/100 PHY 1: enable internal 10/100 PHY
0	phyrst	R	R/W	0	1: Reset internal PHY The internal PHY is reset when this bit is written with 1 and stops reset when this bit is written with 0.

- **Offset 7Ch: GPIO[5:4]**

Bit	Field	HW access	SW access	Default value	Description
7-6	reserved				
5	GPIO5_oe	R	R/W	0	GPIO5 output enable. 1: GPIO5 is used for output 0: GPIO5 is used for input
4	GPIO5_o	R	R/W	0	GPIO5 output value. When GPIO5 is used for output, this value is driven to GPIO5 pin. Set by SW.
3	GPIO5_i	R/W	R		GPIO5 input value. When GPIO5 is used for input, this field reflects the status of GPIO5. Default is pulled-down.
2	GPIO4_oe	R	R/W	0	GPIO4 output enable. 1: GPIO4 is used for output 0: GPIO4 is used for input
1	GPIO4_o	R	R/W	0	GPIO4 output value. When GPIO4 is used for output, this value id driven to GPIO4 pin. Set by SW.
0	GPIO4_i	R/W	R		GPIO4 input value. When GPIO4 is used for input, this field reflects the status of GPIO4. Default is pulled-down.

- **Offset 7Eh: GPIO[1:0]**

Bit	**Field**	**HW access**	**SW access**	**Default value**	**Description**
7-6	reserved				
5	GPIO1_oe	R	R/W	0	GPIO1 output enable. 1: GPIO1 is used for output 0: GPIO1 is used for input
4	GPIO1_o	R	R/W	0	GPIO1 output value. When GPIO1 is used for output, this value id driven to GPIO1 pin. Set by SW.
3	GPIO1_i	R/W	R		GPIO1 input value. When GPIO1 is used for input, this field reflects the status of GPIO1. Set by HW.
2	GPIO0_oe	R	R/W	0	GPIO0 output enable. 1: GPIO0 is used for output 0: GPIO0 is used for input
1	GPIO0_o	R	R/W	0	GPIO0 output value. When GPIO0 is used for output, this value id driven to GPIO0 pin. Set by SW.
0	GPIO0_i	R/W	R		GPIO0 input value. When GPIO0 is used for input, this field reflects the status of GPIO0. Set by HW.

- **Offset 7Fh: GPIO[3:2]**

Bit	Field	HW access	SW access	Default value	Description
7-6	reserved				
5	GPIO3_oe	R	R/W	0	GPIO3 output enable. 1: GPIO3 is used for output 0: GPIO3 is used for input
4	GPIO3_o	R	R/W	0	GPIO3 output value. When GPIO3 is used for output, this value id driven to GPIO3 pin. Set by SW.
3	GPIO3_i	R/W	R		GPIO3 input value. When GPIO3 is used for input, this field reflects the status of GPIO3. Set by HW.
2	GPIO2_oe	R	R/W	0	GPIO2 output enable. 1: GPIO2 is used for output 0: GPIO2 is used for input
1	GPIO2_o	R	R/W	0	GPIO2 output value. When GPIO2 is used for output, this value id driven to GPIO2 pin. Set by SW.
0	GPIO2_i	R/W	R		GPIO2 input value. When GPIO2 is used for input, this field reflects the status of GPIO2. Set by HW.

- **Offset 80h: TEST Register**

Bit	Field	HW access	SW access	Default value	Description
7-5	reserved				
4-1	group_sel	R	R/W	0	Internal probing signal group selection.
0	usb_test	R	R/W	0	0: 6 test pins are used for USB transceiver. 1: 6 test pins are used for internal signal probing.

- **Offset 81: Test Mode**

Bit	Field	HW access	SW access	Default value	Description
7-5	reserved				
4-2	MII test_mode	R	R/W	0	This value could be update from EEPROM offset 0A[4:2]. 3'b000: tri-state MII pins 3'b001: enable MAC's MII signals to external pins 3'b010: enable PHY's MII signals to external pins 3'b011: monitor mode MII
1	USB transceiver test_mode	R	R/W	1	This value could be update from EEPROM offset 0A[1]. 1'b0: external USB transceiver, GPIO[5:0] are used as external USB transceiver interface 1'b1: Internal USB transceiver, GPIO[5:0] are used as GPIO pins.
0	reserved				

- **Transceiver Register Set**

Transceiver registers list

Register	Description	Default
0	Control Register	1000
1	Status Register	7849
2	PHY Identifier 1 Register	0022
3	PHY Identifier 2 Register	5513
4	Auto-Negotiation Advertisement Register	01E1
5	Auto-Negotiation Link Partner Ability Register	0001
6	Auto-Negotiation Expansion Register	0004
7-31	Reserved	XXXX

Transceiver registers Descriptions

Register 0 (MII Control)

BIT	NAME	DESCRIPTION	Read/Write	DEFAULT
15	Reset	1 = PHY Reset 0 = normal operation	R/W, SC	0
14	Loopback	1 = enable loopback 0 = disable loopback	R/W	0
13	Speed selection	1 = 100Mbps/s 0 = 10 Mb/s	R/W	Pin - see note
12	Autonegotiation enable	1 = enable autoneg 0 = disable autoneg	R/W	Pin – see note
11	Power down	1 = Power Down 0 = normal operation	R/W	0
10	Isolate	1 = isolate PHY from MII 0 = normal operation	R/W	0
9	Restart autonegotiation	1 = Restart Autoneg	R/W, SC	0
8	Duplex mode	1 = full, 0 = half	R/W	Pin – see note
7	Collision test	Not implemented	RO	0 - see note
6:0	Reserved		RO	0000000

SC Self Clearing

Reset Reset this port only. This will cause the following:

1. Restart the autonegotiation process.

2. Reset the registers to their default values. Note that this does not affect registers 20, 22, 30 or 31. These registers are not reset by this bit to allow test configurations to be written and then not affected by resetting the port.

Note: No reset is performed to analogue sections of the port. There is also no physical reset to any internal clock synthesisers or the local clock recovery oscillator which will continue to run throughout the reset period. However since the port is restarted and autoneg re-run the process of locking the frequency of the local oscillator (slave) to the reference oscillator (master) will be repeated as it is at the start of any link initialization process.

Loopback Loop back of transmit data to receive via a path as close to the wire as possible. When set inhibits actual transmission on the wire.

Speed selection Forces speed of Phy only when autonegotiation is disabled. The default state of this bit will be determined by a power-up configuration pin in this case. Otherwise it defaults to 1.

Auto-neg enable Defaults to pin programmed value. When cleared allows forcing of speed and duplex settings. When set (after being cleared) causes re-start of autoneg process. Pin programming at power-up allows it to come up disabled and for software to write the desired capability before allowing the first negotiation to commence.

Restart Negotiation only has effect when autonegotiating. Restarts state machine.

Power down Has no effect in this device. Test mode power down modes may be implemented in other specific modules.

Isolate Puts RMII receive signals into high impedance state and ignores transmit signals.

Duplex mode When bit12 is cleared (i.e. autoneg disabled), this bit forces full duplex (bit = 1) or half duplex (bit = 0).

Collision test Always 0 because collision signal is not implemented.

Register 1 (Status):

BIT	NAME	DESCRIPTION	Read/Write	Default
15	100 BASE T4	Not supported	RO	0
14	100BASE-X Full Duplex	1 = PHY is 100BASE-X full duplex capable 0 = PHY is not 100BASE-X full duplex capable	RO	1
13	100BASE-X Half Duplex	1 = PHY is 100BASE-X half duplex capable 0 = PHY is not 100BASE-X half duplex capable	RO	1
12	10Mbps/s Full Duplex	1 = PHY is 10Mbps/s Full duplex capable 0 = PHY is not 10Mbps/s Full duplex capable	RO	1
11	10 Mb/s Half Duplex	1 = PHY is 10Mbps/s Half duplex capable 0 = PHY is not 10Mbps/s Half duplex capable	RO	1
10	100BASE-T2 full duplex	Not supported	RO	0
9	100BASE-T2 half duplex	Not supported	RO	0
8-7	Reserved		RO	00

6	MF Preamble Suppression	1 = PHY can accept management frames with preamble suppression 0 = PHY cannot accept management frames with preamble suppression	RO	1
5	Autoneg Complete	1 = autoneg completed, 0 = autoneg incomplete	RO	0
4	Remote Fault	1 = remote fault detected, 0 = no remote fault detected	RO, LH	0
3	Autoneg Ability	1 = PHY can auto-negotiate, 0 = PHY cannot auto-negotiate	RO	1
2	Link Status	1 = link is up, 0 = link is down	RO, LL	0
1	Jabber Detect	1 = jabber condition detected	RO, LH	0(see note)
0	Extended Capability	1 = extended register capabilities, 0 = basic register set capabilities only	RO	1

LL Latch Low

LH Latch High

Jabber detect Only used in 10Base-T mode. Reads as 0 in 100Base-TX mode.

Register 2 and 3

Each PHY has an identifier, which is assigned to the device.

The identifier contains a total of 32 bits, which consists of the following: 22 bits of a 24bit organisationally unique identifier (OUI) for the manufacturer; a 6-bit manufacturer's model number; a 4-bit manufacturer's revision number. For an explanation of how the OUI maps to the register, please refer to IEEE 802-1990 clause 5.1

Register 2

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15:0	PHY_ID[31-16]	OUI (bits 3-18)	RO	001D(Hex)

Register 3

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15:10	PHY_ID[15-10]	OUI (bits 19-24)	RO	001001(bin)
9:4	PHY_ID[9-4]	Manufacturer's Model Number (bits 5-0)	RO	000001(bin)

3:0	PHY_ID[3-0]	Revision Number (bits 3-0); Register 3, bit 0 is LS bit of PHY Identifier	RO	0001(bin)

This uses the OUI of ADMtek, device type of 1 and rev 0.

Register 4

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15	Next Page	1 = Device set to use Next Page, 0 = Device not set to use Next Page	R/W	0
14	Reserved		RO	0
13	Remote Fault	1 = Local remote fault sent to link partner 0 = no fault detected	R/W	0
12:11	Not implemented	Technology ability bits A7-A6	RO	00
10	Pause	Technology ability bit A5	R/W	0
9	Not implemented	Technology ability bit A4	RO	0
8	100BASE-TX full duplex	Technology ability bit A3 1 = Unit is capable of Full Duplex 0 = Unit is not capable of Full Duplex	R/W	0
7	100BASE-TX half duplex	Technology ability bit A2 1 = Unit is capable of Half Duplex 0 = Unit is not capable of Half Duplex 100BASE-TX	R/W	0
6	10BASE-T full duplex	Technology ability bit A1 1 = Unit is capable of Full Duplex 10BASE-T 0 = Unit is not capable of Full Duplex 10BASE-T	R/W	0
5	10BASE-T half duplex	Technology ability bit A0 1 = Unit is capable of Half Duplex 10BASE-T 0 = Unit is not capable of Half Duplex 10BASE-T	R/W	0
4:0	Selector Field	Identifies type of message being sent. Currently only one value is defined.	RO	00001

Register 5

The register is used to view the advertised capabilities of the link partner once autonegotiation is complete. The contents of this register should not be relied upon unless register 1 bit 5 is set (autoneg complete). After negotiation this register should contain a copy of the link partner's register 4. All bits are therefore defined in the same way as for register 4.

All bits are read only.

This register is used for Base Page code word only.

Base Page Register Format

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15	Next Page	1 = Link Partner is requesting Next Page function 0 = Base Page is requested	RO	0
14	Acknowledge	Link Partner acknowledgement bit	RO	0
13	Remote Fault	Link Partner is indicating a fault	RO	0
12:5	Technology Ability	Link Partner technology ability field.	RO	00(hex)
4:0	Selector Field	Link Partner selector field	RO	00000

Register 6

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15:5	Reserved		RO	000(hex)
4	Parallel Detection Fault	1 = Local Device Parallel Detection Fault 0 = No fault detected	RO, LH	0
3	Link Partner Next Page Able	1 = Link Partner is Next Page Able 0 = Link Partner is not Next Page Able	RO	0
2	Next Page Able	1 = Local device is Next Page Able 0 = Local device is not Next Page Able	RO	1
1	Page Received	1 = A New Page has been received 0 = A New Page has not been received	RO, LH	0
0	Link Partner Autonegotiation Able	1 = Link Partner is Autonegotiation able 0 = Link Partner is not Autonegotiation able	RO	0

LH Latch High

● Electrical Specifications and Timings

● Absolute Maximum Ratings

Supply Voltage (VDD)	-0.3 V to 3.6 V
DC Input Voltage (VIN)	-0.5 V to VDD+0.5V
DC Output Voltage (VOUT)	-0.5 V to VDD+0.5V
Power Comsumption	138mA @ Idle state in 10M
	160mA @ 10M Full Duplex Mode
	159 mA @ 100M Full Duplex Mode
Storage Temperature	-65 C to 150 C
Ambient Temperature	0 C to 70 C
ESD Rating	2000V

● Operating Condition

Symbol	Parameter	Condition	Min	Max	Units
VDD	Supply Voltage		3.0	3.6	V
5VDD	USB Bus Supply Voltage		4.4	5.25	V
I_{dd}	Supply Current			150	mA

● DC Specifications

USB Interface DC specification

Symbol	Parameter	Condition	Min	Max	Units
V_{ih}	Input High Voltage		2.0		V
V_{il}	Input Low Voltage			0.8	V
I_{ih}	Differential Input Sensitivity		0.1		V
V_{cm}	Differential Common Mode Range		0.8	2.5	V
V_{oh}	Output High Voltage		0.0	0.3	V
V_{ol}	Output Low Voltage		2.8	3.6	V
V_{crs}	Output Signal Crossover Voltage		0.8	2.5	V

EEPROM Interface DC specification

Standard Vcc (4.5V to 5.5V) DC Specification

Symbol	Parameter	Condition	Min	Max	Units
V_{ih}	Input High Voltage		2.0	Vcc +1	V
V_{il}	Input Low Voltage		-0.1	0.8	V
I_{ih}	Input High Leakage Current	$0<V_{in}<Vcc$		1	µA
I_{il}	Input Low Leakage Current	$0<V_{in}<Vcc$		-1	µA
V_{oh}	Output High Voltage	I_{oH} = -10 µA	Vcc –0.2		V
V_{ol}	Output Low Voltage	I_{oL} = 10 µA		0.2	V
C_{in}	Input Pin Capacitance			5	pF

Low Vcc (2.7V to 5.5V) DC Specification

Symbol	Parameter	Condition	Min	Max	Units
V_{ih}	Input High Voltage		0.8Vcc	Vcc +1	V
V_{il}	Input Low Voltage		-0.1	0.15Vcc	V
I_{ih}	Input High Leakage Current	$0<V_{in}<Vcc$		1	µA
I_{il}	Input High Leakage Current	$0<V_{in}<Vcc$		-1	µA
V_{oh}	Output High Voltage	I_{oH} = -10 µA	0.9Vcc		V
V_{ol}	Output Low Voltage	I_{oL} = 10 µA		0.1Vcc	V
C_{in}	Input Pin Capacitance			5	pF

GPIO Interface DC Specification

Symbol	Parameter	Condition	Min	Max	Units
V_{ih}	Input High Voltage		2.0		V
V_{il}	Input Low Voltage			0.8	V
I_{ih}	Input High Leakage Current	$0<V_{in}<Vcc$		10	µA
I_{il}	Input Low Leakage Current	$0<V_{in}<Vcc$		-10	µA
V_{oh}	Output High Voltage	I_{oH} = -4 mA	2.4		V
V_{ol}	Output Low Voltage	I_{oL} = 4 mA		0.4	V

● Timings

Reset Timing

ADM8511 can be reset either by hardware, software or USB reset.

1. A hardware reset is accomplished by asserting the RST# pin after power up the device. It should have a duration of at least 80 ms to ensure the external 48MHz crystal is in stable and correct frequency. All registers will be reset to default values.
2. A software reset is accomplished by setting the reset bit (bit 4) of the Ethernet Control Register (address 01h). This software reset will reset all registers to default values.
3. When ADM8511 sees an SE0 on USB bus for more than 2.5μs. This USB reset will reset all registers to default values.

USB Interface Timing

Symbol	Parameter	Condition	Min	Max	Units
T_{fr}	Rise Time		4	20	ns
T_{ff}	Fall Time		4	20	ns
T_{frfm}	Differential Rise and Fall Time Matching	T_{FR}/T_{FF}	90	111.11	%
T_{fdrate}	Full-speed Data Rate		11.9700	12.0300	Mb/s
T_{feopt}	Source SE0 interval of EOP		160	175	ns
T_{fst}	Width of SE0 interval during differential transition			14	ns

EEPROM Interface Timing

Symbol	Parameter	Min	Max	Units
t_{EESK}	**EESK** Clock Frequency	0	1	MHz
T_{EECSS}	**EECS** Setup Time to **EESK**	0.2		μs
T_{EECSH}	**EECS** Hold Time from **EESK**	0		ns
T_{EEDOH}	**EEDO** Hold Time from **EESK**	70		ns
T_{EEDOP}	**EEDO** Output Delay to “1” or “0”		2	μs
t_{EEDIS}	**EEDI** Setup Time to **EESK**	0.4		μs
t_{EEDIH}	**EEDI** Hold Time from **EESK**	0.4		μs

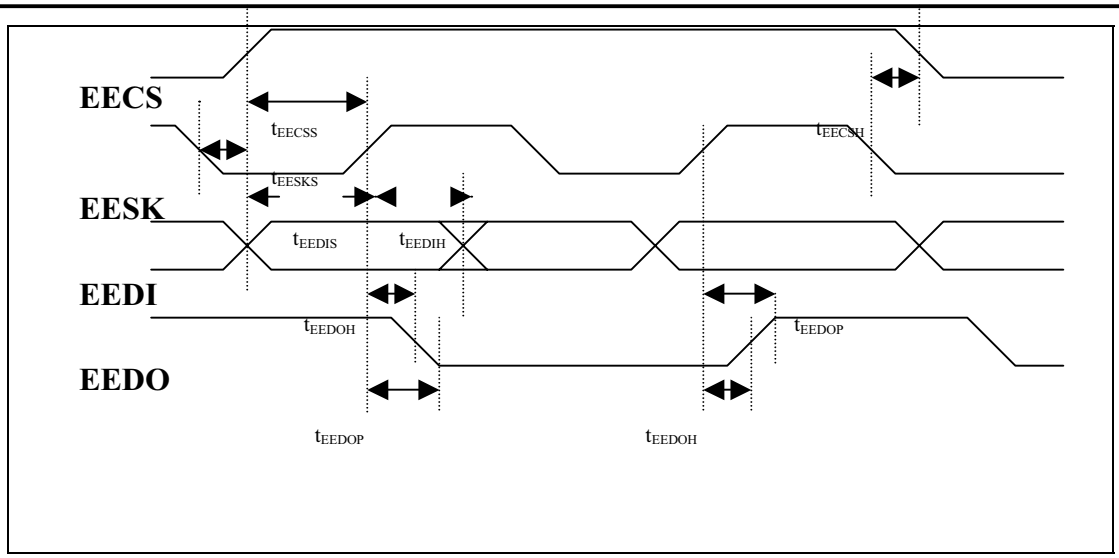


Fig. 1 EEPROM Interface Timings

- **MII Interface Timing**

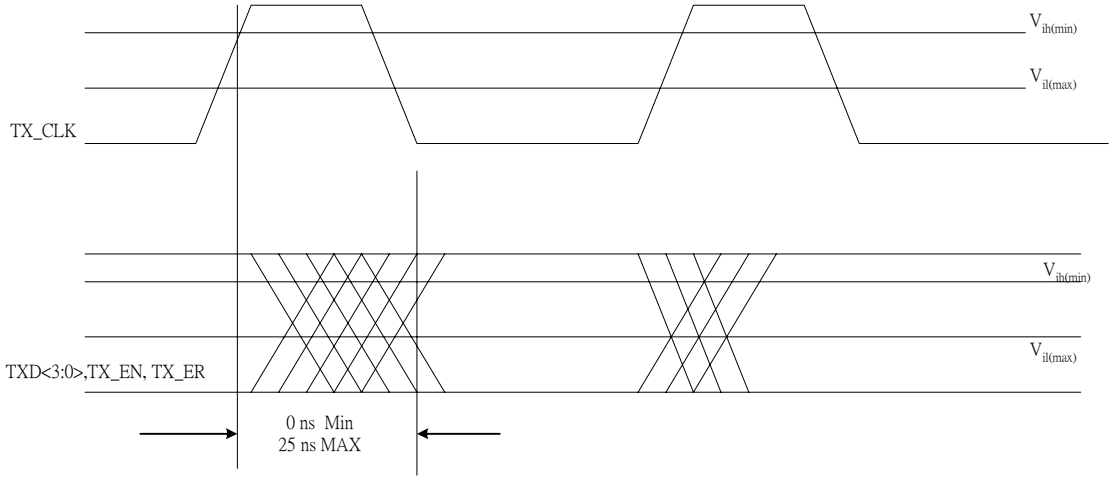


Fig. 4 Transmit signal timing relationships at the MII

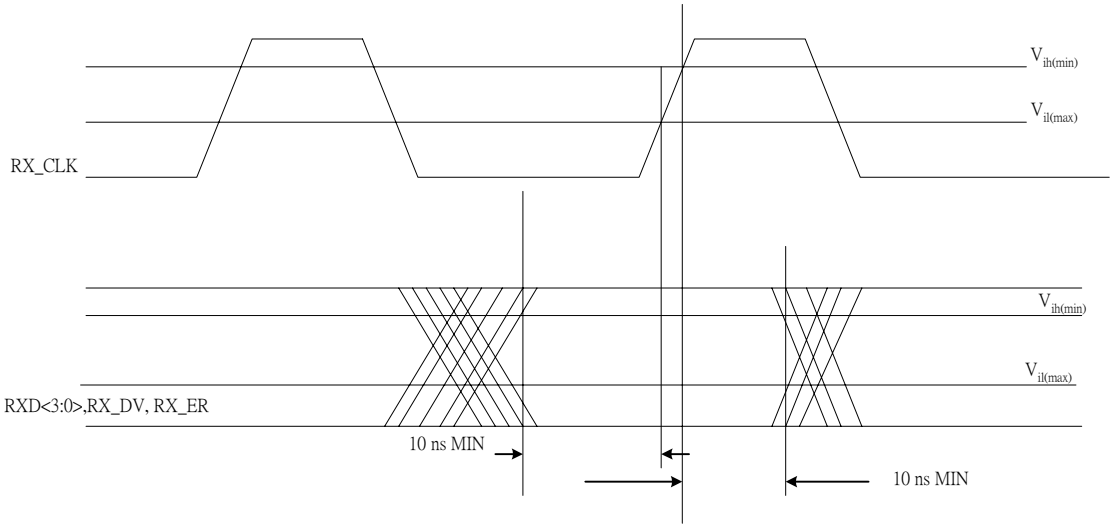


Fig. 5 Receive signal timing relations at the MII

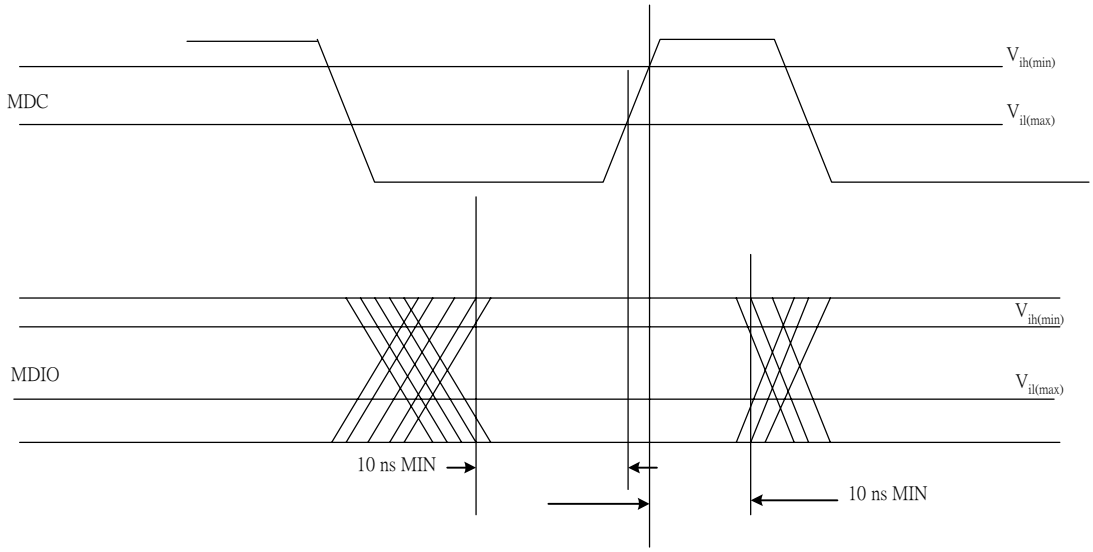


Fig. 6 MDIO sourced by STA

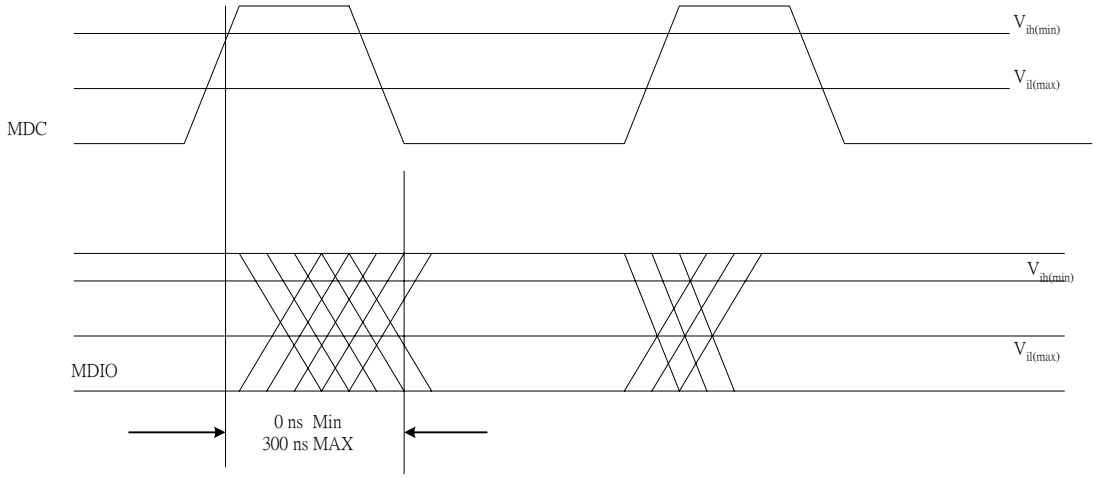


Fig. 7 MDIO sourced by PHY

12. Package

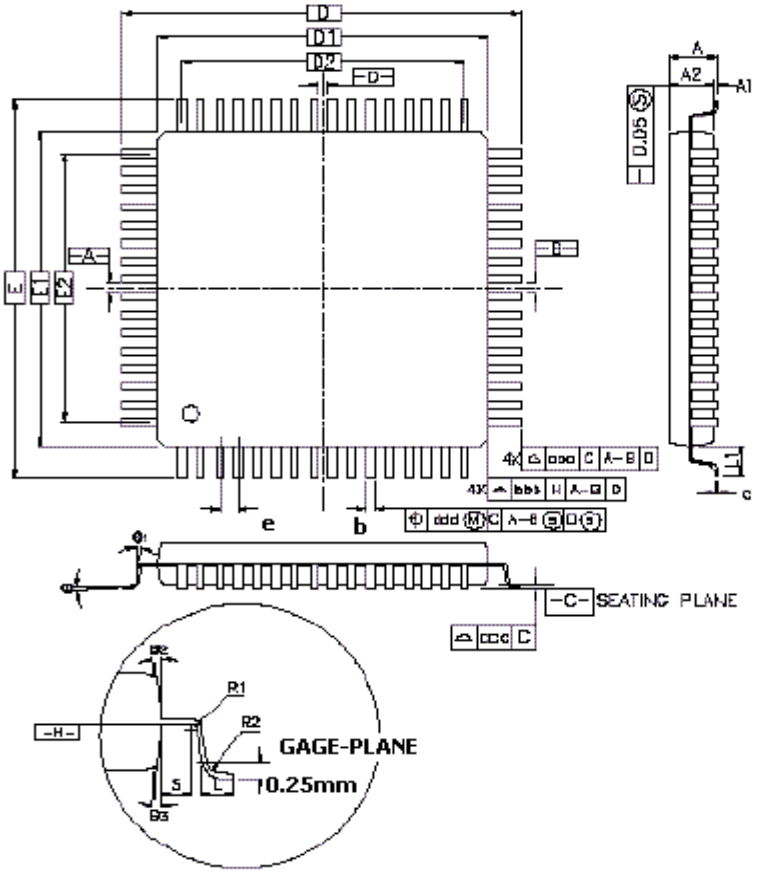


Fig. 8 Package outline of ADM8511

Dimensions for 100 pin LQFP Package

Symbol	Millimeter (mm)			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	--------	---------	1.60	-------	--------	0.063
A_1	0.05	---------	0.15	0.002	--------	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D_1	14.00 BSC.			0.551 BSC		
E	16.00 BSC.			0.630 BSC.		
E_1	14.00 BSC.			0.551 BSC.		
R_2	0.08	-------	0.20	0.003	------	0.008
R_1	0.08	------	------	0.003	------	------
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ_1	0°	------	------	0°	------	------
Θ_2	11°	12°	13°	11°	12°	13°
Θ_3	11°	12°	13°	11°	12°	13°
c	0.09	------	0.20	0.004	------	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 Ref			0.039 Ref		
S	0.20	------	------	0.008	------	------
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC,			0.020 BSC.		
D_2	12.00			0.472		
E_2	12.00			0.472		
Tolerance of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Notes :

1. Dimensions D_1 and E_1 do not incl0ude mold protrusion. Allowable protrusion is 0.25mm per. Side D_1 and E_1 are Maximum plastic body size dimensions including mold mismatch.
2. Dimension b does not include dambar protrusion stall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4 mm and 0.5mm pitch packages.

APPENDIX 1 Layout Guide

1.Placement:

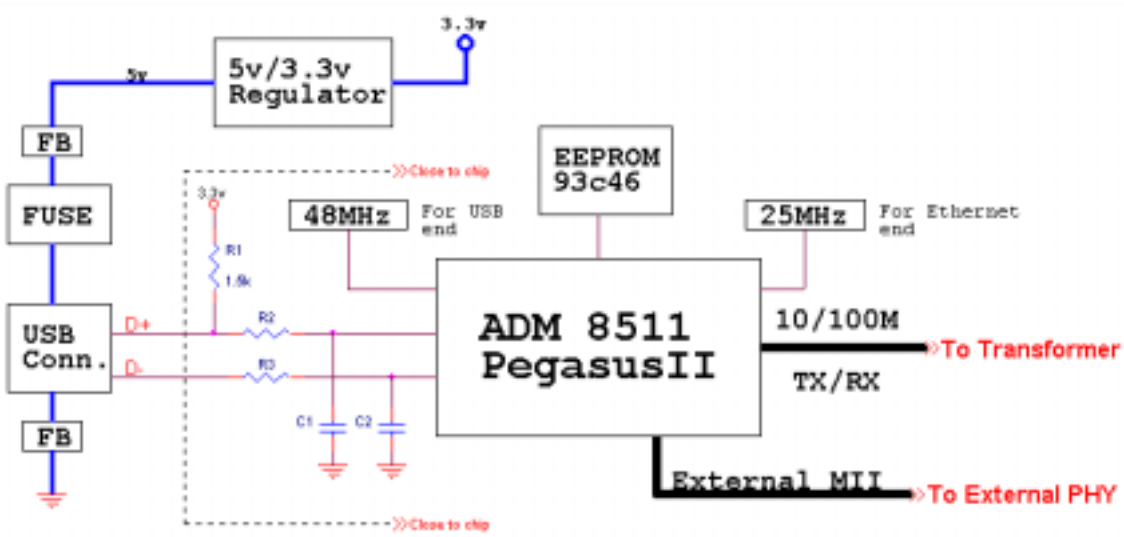
(1) On USB side,Place PegasusII and USB connector as close as possible.

(2) On Ethernet side,place PegasusII ,transformer and RJ45 as close as possible .

(3) The crystal or OSC device should be close to PegasusII and away from the following items:

- ●Any analog signal
- ●PCB edge
- ●Any other high frequency components and their associated traces.

(4)Place the filtering capacitor as close as possible at the power pin of ADM 8511 (Pegasus II) and its trace is short and wide.



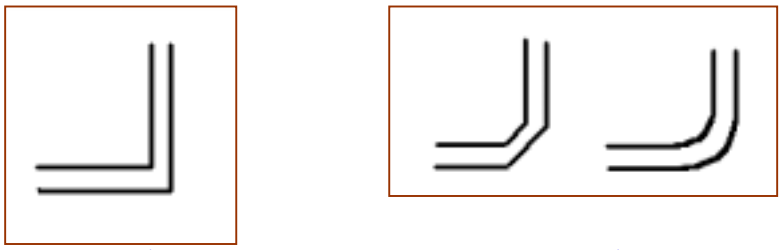
2.Trace routing

(1)Keep USB differential pair data signal D+ and D-:

- ●Trace width should be as wide as possible.
- ●Make D+ and D- traces route at the same signal plane and doesn't pass through other plane .
- ●Inhibit crossover on D+ and D-
- ●The termination resistance (R2,R3) and decoupling capacitors (C1,C2) should be close to ADM8511.
- ●D+ and D- Signal trace length should be equal and as short as possible.

(2)Arrangement Tx and Rx trace

● Tx+/- and Rx+/- trace avoid right angle and round angle >90 degree; suggested.



Bad Good

●Trace width must be wide and should be wider than 8 miles.

●Signal trace length between Tx+/- differential pairs should be cross and have equal length .The total length should be no longer than 2 cm. The same requirement also apply to Rx+/-.

●Make Tx and Rx trace route at the same signal plane and doesn't pass through other plane.

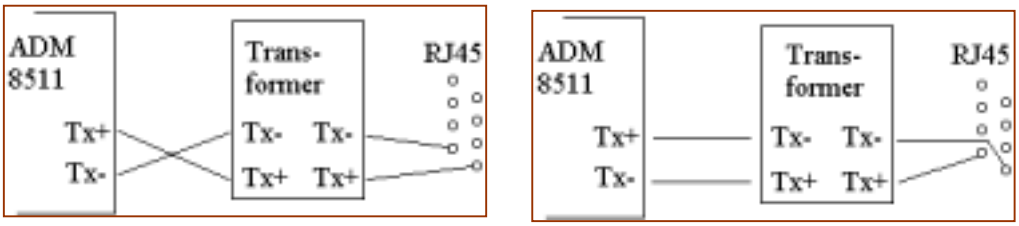
●Every differential pairs as cross as possible, but no less than 8 miles and space should be almost equal .

●Keep space large between Tx and Rx differential pairs, even separated ground planes underneath Tx and Rx signal pairs.

●Away from clock and power traces.

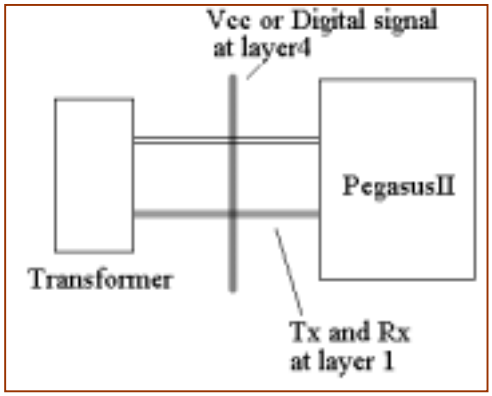
● If Tx routed trace must cross, the trace can be swapped between chip and transformer, and transformer to RJ45 ,too.

Origin Suggest



(3) Digital signal should be away from analog signal and power traces .If this can't be avoid , analog and Vcc should cross over 90 degree at other plane.

(4)Vcc trace should short and prefer to route in this plane format, special for GND.



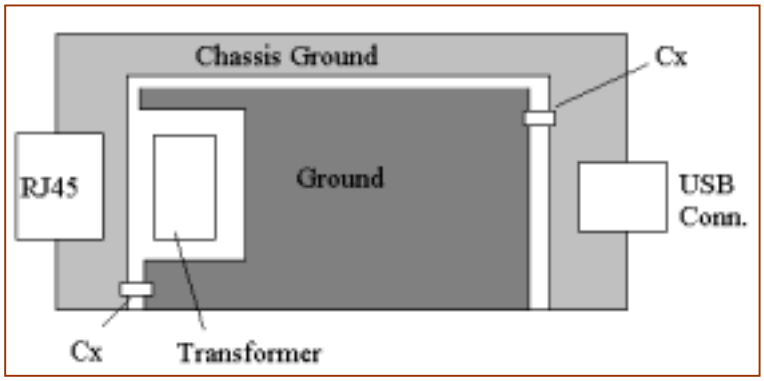
3.Power and Ground

(1)Every power pin should have 0.1uF SMD capacitors placed with it. To be effective, the capacitors should be placed as close as possible at the pin.

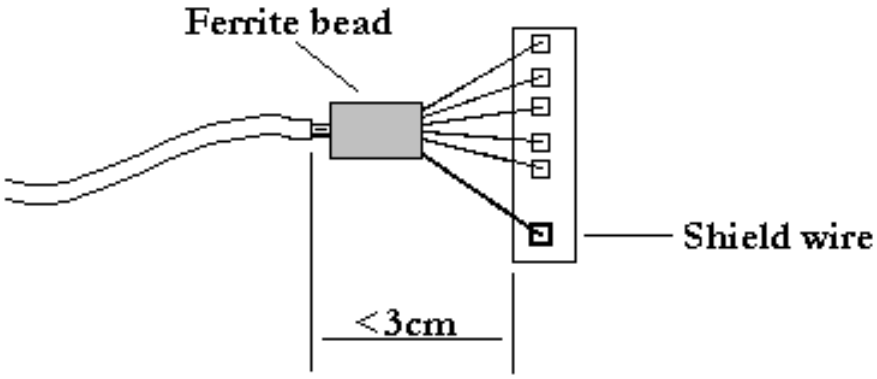
(2)The chassis ground plane connected to the USB B type and network connector chassis should be isolated from the signal plane with 0.1uF capacitors or bead to prevent any radiation from leaking and resulting in FCC failure.

(3)Right angle is recommend when partition Vcc as well as GND planes.

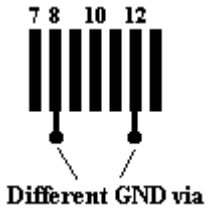
(4)Avoid power and ground planes placing directly under the transformer.See the Figure as below.



(5)If you use a permanently attached cable (plus the shield wire).it may require additional filtering for FCC test pass.and the length of unshielded cable should be limited to 3cm or less.



(6) Please connect pin12(GndRef) and pin8(GndR) first then use signal via to Gnd.



Bad

Good

APPENDIX 2 EEPROM Interface & Example

General EEPROM Format Description

If the EEPROM contents from offset 0 to offset 5 is "FF_FF_FF_FF_FF_FF", it means the EEPROM isn't programmed correctly, The default values for every field are used instead of loading from EEPROM.

Offset(byte)	Field	Description
00	node_id0	The 1st byte of Ethernet node ID.
01	node_id1	The 2nd byte of Ethernet node ID.
02	node_id2	The 3rd byte of Ethernet node ID.
03	node_id3	The 4th byte of Ethernet node ID.
04	node_id4	The 5th byte of Ethernet node ID.
05	node_id5	The 6th byte of Ethernet node ID.
06-07	reserved	
08	max_pwr	The maximum USB power consumption.
09	ep3_interval	The polling interval for endpoint 3. If this value is 0, EP3 is disabled.
0A[0]	iso_enable	0
0A[1]	USB transceiver Test_mode	0: select external USB transceiver. 1: select internal USB transceiver.
0A[4:2]	MII Test_mode	000b: tri-state MII pins 001b: enable MAC's MII signals to external interface 010b: enable PHY's MII signals to external interface 011b: monitor MII mode
OA[7]	Remote wakeup Enable	0: Enable 1: Disable
0B[7:6]	LED mode	Refer to pin assignment
0B[5:0]	reserved	
0C	languageid_lo	The low byte of language ID.
0D	languageid_hi	The high byte of language ID.
0E-0F	reserved	
10	manuid_lo	The low byte of manufacture ID.
11	manuid_hi	The high byte of manufacture ID.
12	proid_lo	The low byte of product ID.
13	proid_hi	The high byte of product ID.
14	manu_str_len	The length for manufacture string.
15	manu_str_offset	The word offset address of manufacture string.
16	pro_str_len	The length for product string.
17	pro_str_offset	The word offset address of product string.
18	seri_str_len	The length for serial number string.
19	seri_str_offset	The word offset address of serial number string.

Example

offset(byte)	**value**
0000h:	00, 00 E8 00 02 2C 00 00,
0008h:	50 01 02 00 09 04 00 00
0010h:	A6 07 11 85 0E 10 2A 20
0018h:	0A 38 00 00 00 00 00 00
0020h:	0E 03 41 00 44 00 4D 00
0028h:	74 00 65 00 6B 00 00 00
0030h:	1E 00 55 00 53 00 42 00
0038h:	20 00 31 00 30 00 2F 00
0040h:	2A 03 55 00 53 00 42 00
0048h:	-20 00 54 00 6F 00 20 00
0050h:	4C 00 41 00 4E 00 20 00
0058h:	43 00 6F 00 6E 00 76 00
0060h:	65 00 72 00 74 00 65 00
0068h:	72 00 00 00 00 00 00 00
0070h:	0A 03 30 00 30 00 30 00
0078h:	31 00 00 00 00 00 00 00

Offset(byte)	Value	Description
00-05	00_00_E8_10_46_02	NIC node ID
08	50	maximum power 160mA
09	01	interrupt endpoint 3 polling interval 1ms
0A	02	isochronous endpoint disable, select internal USB transceiver Use internal Ethernet PHY Wake on Lan enable
0C-0D	0904	Language ID 0409
10-11	A607	manufacture ID 07A6
12-13	8511	product ID 8511
14	0E	manufacture string length 0E bytes
15	10	manufacture string starts from word offset 10h, thus byte offset 20h.
16	1E	product string length 1E bytes
17	18	product string starts from word offset 18h, thus byte offset 30h.
18	0A	serial number string length 0A bytes
19	38	serial number string starts from word offset 38h, thus byte offset 70h.

20-2E	0E 03 41 00 44 00 4D 00 74 00 65 00 6B 00	0E:descriptor size 14 bytes 03: string descriptor 41.....: UNICODE encoded string
30-4E	1E 03 55 00 53 00 42 00 20 00.....	1E:descriptor size 30 bytes 03: string descriptor 55.....: UNICODE encoded string
50-5A	0A 03 30 00 30 00 30 00 31 00	0A: descriptor size 10 bytes 03: string descriptor 30.....: UNICODE encoded string

APPENDIX 3 USB Device Operation

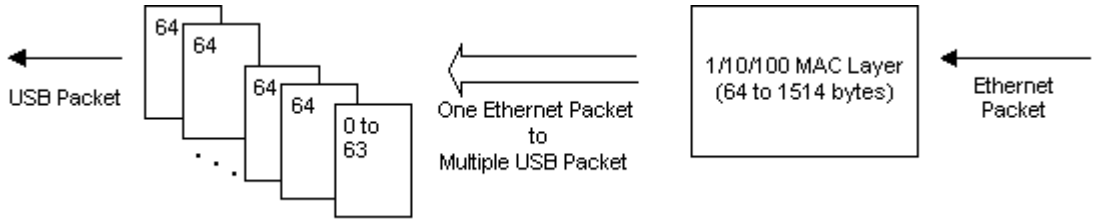
Endpoint 0

Endpoint 0 is in charge of response to standard USB commands and vendor specific commands. Internal registers setting are also via this endpoint. The response to each command is described in section 7.

Endpoint 1 bulk IN

Endpoint 1 is in charge of sending the received Ethernet packet to USB host. An Ethernet packet will be split to multiple 64-byte USB packets on USB. The end of the Ethernet packet is indicated by less then 64-byte or 0 length data transfer in this pipe. The Ethernet received status is optionally reported at the end of the packet.

While accessing to this endpoint if RX FIFO is either full or any packet is inside, the data in RX FIFO is returned in USB data stage. If ACK is received from USB host, data in RX FIFO is flushed. If no response or NAK is received from USB host, the content in RX FIFO will be re-transmitted. If RX FIFO isn't ready for transmission, NAK is returned to USB host.



The received status is reported as follows

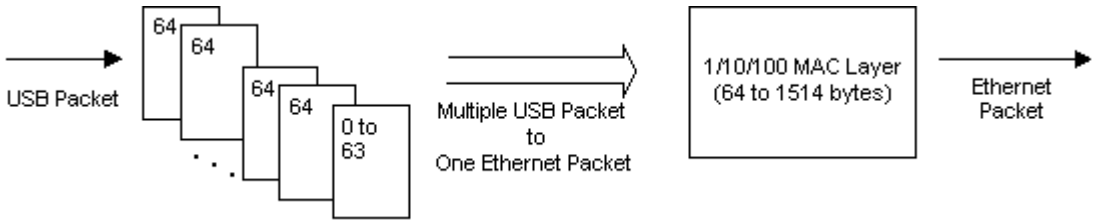
Offset	Bit	Field	Description
Offset0	7-0	rx_bytecnt_lo	The received byte count[7:0].
Offset1	3-0	rx_bytecnt_hi	The received byte count[11:8].
	7-4	Reserved	
Offset2	0	Multicast_frame	Indicate receive a multicast frame.
	1	Long_pkt	Indicate received packet length > 1518 bytes.
	2	Runt_pkt	Indicate received packet length < 64 bytes.
	3	crc_err	Indicate CRC check error.
	4	Dribble_bit	Indicate packet length is not integer multiple of 8-bit.
	7-5	Reserved	
Offset3	7-0	Reserved	

Endpoint 2 bulk OUT

Endpoint 2 is in charge of sending the USB packet to Ethernet. An Ethernet packet is concatenated as multiple 64-byte USB packets on USB. The first two bytes in every first concatenated USB packet indicate the total length of the Ethernet packet. The end of the Ethernet packet is indicated with less then 64-byte or 0 length data transfer in this pipe. The Ethernet transmit status is reported in transmit status register.

When access to this endpoint, data in USB data stage is transfer to TX FIFO when TX FIFO is free and ACK is returned. If TX FIFO isn't free, NAK is returned.

Field	1st byte in 1st USB packet	2nd byte in 1st USB packet	The following packets
Content	len[7:0]: Low byte Ethernet packet length	{reserved[4:0], len[10:8]}	Ethernet packet



Endpoint 3 interrupt IN

Endpoint 3 is in charge of returning the current Ethernet transfer status every polling interval. When access to this endpoint, 8 bytes data is returned to USB host. The 8-byte packet contains

Offset0	Offset1	Offset2	Offset3	Offset4
tx_status(Reg2Bh)	tx_status(Reg2Ch)	rx_status(Reg2Dh)	rx_lostpkt(Reg2Eh)	rx_lostpkt(Reg2Fh)

Offset5	Offset6-7(2B)
Wakeup_status(Reg7Ah)	0

APPENDIX 4 USB Command

Get_Register (Vendor Specific) Single/Burst read

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
C0	F0	0	{RegIndex[0:7], 00}	length

- Data Stage

Offset0(1B)	Offset1(1B)	Offset2(1B)
{RegIndex}	{RegIndex+1)	{RegIndex+2)

The returned total number of registers depends on the length field.

Set_Register (Vendor Specific) Single write

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
40	F1	{value[0:7],mask[0:7]}	{RegIndex[0:7], 00}	1

Set_Register(Vendor Specific) Burst write

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
40	F1	0	{RegIndex[0:7], 00}	length

- Data Stage

Offset0(1B)	Offset1(1B)	Offset2(1B)	Offset3(1B)
{RegIndex}	{RegIndex+1}	{RegIndex+2}	{RegIndex+3}

Ex. Write 44 to RegIndex=05h, the transfer will be

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
40	FE	4400	0500	0100

If wLength > 1, more than 1 register is accessed (burst write) and mask is not supported

=> DataStage for 8-byte OUT transfer appears

Ex. Burst write 20 registers from RegIndex=07h and data from 01_d to 20_d

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
40	FE	0000	0700	1400

- Data Stage

➢ 1st OUT transfer

Offset0(1B)	Offset1(1B)	Offset2(1B)	Offset3(1B)	Offset4(1B)	Offset5(1B)	Offset6(1B)	Offset7(1B)
01	02	03	04	05	06	07	08

➢ 2nd OUT transfer

Offset0(1B)	Offset1(1B)	Offset2(1B)	Offset3(1B)	Offset4(1B)	Offset5(1B)	Offset6(1B)	Offset7(1B)
09	0A	0B	0C	0D	0E	0F	10

➢ 3rd OUT transfer

Offset0(1B)	Offset1(1B)	Offset2(1B)
11	12	13

Get_Status(Device)

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	0	0	0	2

- Data Stage

D[15:2]	D[1]: Remote Wakeup	D[0]:Self Powered
0	register of remote_wakeup	1

Get_Status(Interface)

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
81	0	0	0	2

- Data Stage

D[15:0]
0

Get_Status(EP0)

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
82	0	0	0080 or 0000	2

- Data Stage

D[15:1]	D[0]: Halt
0	register of ep0_halt

Get_Status(EP1) bulk IN

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
82	0	0	0081	2

- Data Stage

D[15:1]	D[0]: Halt
0	register of ep1_halt

Get_Status(EP2) bulk OUT

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
82	0	0	0002	2

- Data Stage

D[15:1]	D[0]: Halt
0	register of ep2_halt

Get_Status(EP3) interrupt IN

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
82	0	0	0083	2

- Data Stage

D[15:1]	D[0]: Halt
0	register of ep3_halt

Get_Descriptor(Device) total 18-byte

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	6	0001	0	length

- Data Stage: wLength field specifies the total byte count to return

Offset0	Offset1(type)	Offset2(USB release no.)	Offset4(Class code)	Offset5(Sub Class Code)	Offset6(Protocol)	Offset7(EP0 MaxPktSize)	Offset8 (vendor ID)
12(1B)	01(1B)	0110(2B)	00(1B)	00(1B)	00(1B)	8(1B)	(2B)

Offset10 (productID)	Offset12(releaseID)	Offset14 (manufacture)	Offset15 (Product)	Offset16(serial no.)	Offset17(no. of config)
(2B)	0001(2B)	01(1B)	02(1B)	03(1B)	01(1B)

Get_Descriptor(Configuration) total 39-byte

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	6	0002	0	length

- Data Stage

➢ Configuration Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (TotalLength)	Offset4 (NumInterface)	Offset5 (ConfgValue)	Offset6 (StringIndex)	Offset7 (Attribute)	Offset8 (MaxPower)
09(1B)	02(1B)	0027(2B)	01(1B)	00(1B)	00(1B)	E0(1B)	max_pwr(1B)

➢ Interface 0 Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (InterfaceNum)	Offset3 (AltInterface)	Offset4 (NumEP)	Offset5 (IntfClass)	Offset6 (IntfSubClass)	Offset7 (IntfProtocol)	Offset8 (StringIndex)
09(1B)	04(1B)	00(1B)	00(1B)	04(1B)	xx(1B)	E0(1B)	xx(1B)	00(1B)

➢ EP1 Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (EPAddr)	Offset3 (Attribute)	Offset4 (MaxPktSize)	Offset6 (Interval)
07(1B)	05(1B)	81(1B)	02(1B) bulk	0064(2B)	00(1B)

➢ EP2 Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (EPAddr)	Offset3 (Attribute)	Offset4 (MaxPktSize)	Offset6 (Interval)
07(1B)	05(1B)	02(1B)	02(1B) bulk	0064(2B)	00(1B)

➢ EP3 Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (EPAddr)	Offset3 (Attribute)	Offset4 (MaxPktSize)	Offset6 (Interval)
07(1B)	05(1B)	83(1B)	03(1B) interrupt	0008(2B)	ep3_interval(1B)

Get_Descriptor(String) Index0, LanguageID Code

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	06	0003	0000	length

- Data Stage

Offset0 (Length)	Offset1 (DscrType)	Offset2 (LanguageID)
04(1B)	03(1B)	0904(2B)

Get_Descriptor(String) Index1, manufacture

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	06	0103	0904	length

- Data Stage

Offset0 (Length)	Offset1 (DscrType)	
length(1B)	03(1B)	String

Get_Descriptor(String) Index2, product

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	06	0203	0904	length

- Data Stage

Offset0 (Length)	Offset1 (DscrType)	
length(1B)	03(1B)	String

Get_ Descriptor(String) Index3, serial no.

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	06	0303	0904	length

- Data Stage

Offset0 (Length)	Offset1 (DscrType)	
Length(1B)	03(1B)	String

Get_Configuration

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	08	0	0	0001

- Data Stage

Offset0 (ConfgValue)(1B)

Get_Interface

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
81	10	0	0	0001

- Data Stage

Offset0 (AltIntf)(1B)
00

Set_Address

Set_Configuration

Set_Interface

Clear_Feature(Device) Remote Wakeup

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
00	01	0100	0	0

Set_feature(Device) Remote Wakeup

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
00	03	0100	0	0

Clear_Feature(EP0,1,2,3) Halt

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
02	03	0000	{00, EP no}	0

Set_Feature(EP0,1,2,3) Halt

- Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
02	03	0000	{00, EP no}	0

APPENDIX 5 Design Notes for Ethernet & MII Application(HPNA&HomePlug)

1.48MHz Crystal

ADM8511 need a 48MHz crystall (+/- 50ppm,over tone) to work on USB side. Because the 48MHz crystal is a over tone part , It need work with a L/C pair. However, 48MHz fundamental crystal is also valid and associates with two ceramic capacitor.

2.SRAM

All of the SRAM pin can be NC (No Connection).

3.RST# and POREN_N

a. Internal Power On Reset in ethernet only or combo (Ethernet & HPNA) solution:
The ADM8511 provides internal power reset. In ethernet only or combo sloution,you can let RST# and POREN_N pin NC.

b. External reset in external PHY only solution.(e.g. Home PNA only)
Condition : (1) POREN_N pull to high and (2) RST# asserts low when external reset is active.
RST# combines with a reset circuit (e.g. RC circuit) to provide a low pulse to be reset signal. The duration of the low pulse is 50ms at least . The recommended time is more than 80ms. Moreover, it still needs 25MHz crystal oscillation circuit and Ribb pin connects a 10K resistor to ground.

4.XLNKSTS:

a. Ethernet only solution:

This pin need strapping to low directly.

c. Combo or External PHY only solution:

reports link status information to system and level change trigger.

5.LED

all of the LED pin are active Low and only display internal PHY status.

6.Ethernet pin (LED,XTLP/N,TXOP/N,RXIP/N,RIBB,TST0…3)

In External PHY solution ,All can be NC.

7.MII interface signal pins

a. In ethernet only solution:

All of the MII pin can be NC.

b. In combo or external PHY only solution:

i. MDIO rquires external 1.5k pull-up resistor.

ii. TXEN requires external 4.7k pull-down resistor.

If the external PHY did not provide RXER, this pin needs strapping to low directly.