ICD2042A

Dual VGA Clock Generator

Single-Chip Dual Oscillator for Personal Computer Graphics Boards Handles Frequency Requirements of Popular VGA/XGA/8514 Chip Sets

- 3 Independent Clock Outputs — Separate Pixel and Memory Clocks and Buffered Reference Clock
- Phase-Locked Loop Output Range of 350 KHz – 120 MHz
- Phase-Locked Loop Oscillator Input Derived from PC System Bus or from Single 14.31818 MHz Crystal
- Ideally Suited for VGA, XGA and 8514 Graphics Applications
- Sophisticated Internal Loop Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters
- 3-State Oscillator Control Disables Outputs for Test Purposes
- "Change-on-the-Fly" Frequency Selection Supports Most Popular VGA/8514 Chip Sets
- 5V Operation
- Low-Power, High-Speed CMOS Technology
- Available in 16-Pin SOIC Package

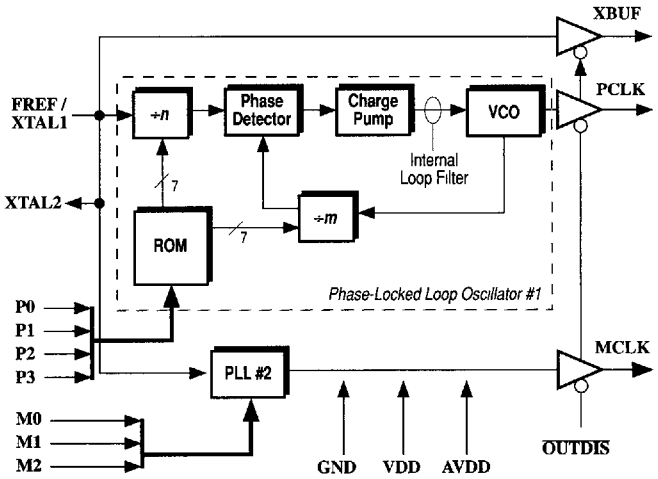


Fig. 1: ICD2042A Block Diagram

Contents

Figures

Tables

Introduction

The proliferation of video standards, support for various monitors, increasing screen resolutions, and different memory speeds present in the DOS graphics community often require as many as six different crystal can oscillators per PC board. A new family of frequency synthesis parts from IC DESIGNS replaces the large number of these oscillators required to build such multi-function graphic boards as EGA, VGA, Super VGA, and 8514. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit board space required.

The ICD2042A Dual VGA Clock Generator supports new designs using the newer graphic chip sets which generate output frequency select information. The ICD2042A features two independent clock outputs for the pixel clock and the memory clock which are chosen via select lines. Additional features include 3-stateable outputs and direct support for popular graphics chip set selection decodes.

Pin & Signal Descriptions

Fig. 2: Pin Descriptions

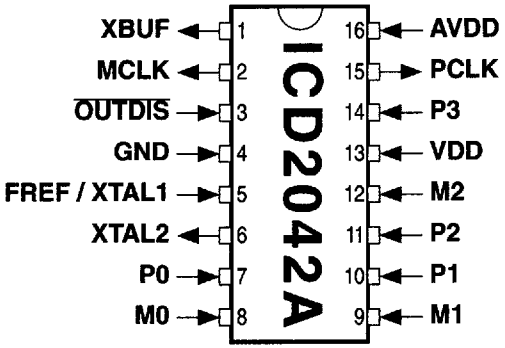


Table 1: Signal Descriptions

Pin #	Signal	Function
1	XBUF	Buffered Reference Frequency Output
2	MCLK	Memory Clock Oscillator Output (see *Table 2: Memory Clock ROM Decode Options* on page 115)
3	$\overline{\text{OUTDIS}}$	Output Disable (Enable 3-State Output) when signal is pulled low. (Internal pull-up allows no-connect if 3-state operation not needed).
4	GND	Ground
5	FREF / XTAL1	Input Reference Oscillator (nominally 14.31818 MHz.) A crystal may be used if a reference oscillator is not available.
6	XTAL2	Oscillator Output to a reference Series-Resonant Crystal. For higher accuracy, a Parallel-Resonant Crystal may be used. Assume CLOAD ≈ 17pF. For more specifics on crystal requirements please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics* on page 292. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.)
7	P0	Input Pixel Clock Selection Signal — Bit 0 (internal pull-up)
8	M0	Input Memory Clock Selection Signal — Bit 0 (internal pull-up)
9	M1	Input Memory Clock Selection Signal — Bit 1 (internal pull-up)
10	P1	Input Pixel Clock Selection Signal — Bit 1 (internal pull-up)
11	P2	Input Pixel Clock Selection Signal — Bit 2 (internal pull-up)
12	M2	Input Memory Clock Selection Signal — Bit 2 (internal pull-up)
13	VDD	+5V to I/O Ring
14	P3	Input Pixel Clock Selection Signal — Bit 3 (internal pull-down)
15	PCLK	Pixel Clock Oscillator Output
16	AVDD	+5V to Analog Core (Special Order: bond VDD to AVDD internally.)

General Considerations

Design Recommendations

The ICD2061A, with its ability to program the output frequencies, is recommended for designs in which a fixed ROM would be inconvenient and/or the desired volume does not warrant a custom ROM.

The ICD2042A is currently a custom order only.

Pixel and Memory Clock Oscillator Selection

The output frequency value of the pixel clock oscillator (PCLK) is selected by the four pixel clock selection inputs: P0, P1, P2, and P3. This feature allows the ICD2042A to support different video configurations. The output frequency value of the memory clock oscillator (MCLK) is selected by the three memory clock selection inputs: M0, M1, and M2. The selection table is *Table 2: Memory Clock ROM Decode Options* on page 115.

At any time during operation, the selection lines can be changed to select a different frequency. When this occurs, the internal phase-locked loop will immediately seek the newly selected frequency. During the transition period, the clock output will multiplex glitch-free to the reference signal until the PLL settles to the new frequency.

Normally, the MCLK select lines are hard-wired during manufacturing to correspond to the desired memory speed. A different memory clock frequency output may be generated by changing the memory select lines of the ICD2042A. The timing for this transition is detailed in *Table 6: AC Characteristics* on page 120.

Table 2: Memory Clock ROM Decode Options

M2	M1	M0	Word	2042–23	2042–24	2042–27
				(Frequencies in MHz)		
0	0	0	0	48.000	48.000	40.000
0	0	1	1	39.800	39.800	41.000
0	1	0	2	66.000	66.000	41.500
0	1	1	3	50.000	50.000	42.000
1	0	0	4	56.644	56.644	42.500
1	0	1	5	32.000	32.000	43.000
1	1	0	6	44.000	44.000	44.000
1	1	1	7	39.800	39.800	48.000

PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at the higher pixel clock frequencies above 50 MHz.

A full power and ground plane layout should be employed both under and around the IC package. It is important that the ground plane be nearly continuous with a minimum of cuts, holes, or breaks. Both analog and digital ground pins should go directly to this plane.

To produce an output of high spectral purity, additional supply noise precautions might be required, particularly in noisy environments. The analog power pin (AVDD) should be bypassed to ground with a 0.1µF multi-layer ceramic capacitor and a 2.2µF/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin. A 22Ω resistor placed between the power supply and AVDD can help to filter noisy supply lines.

The designer should also avoid routing the two output traces of the ICD2042A in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies.

When designing with this device, it is best to locate the ICD2042A closest to the device requiring the highest frequency. For more details concerning layout and power considerations, please see the IC DESIGNS Application Note *Power Feed and Board Layout Issues* on page 281.

Output Frequency Accuracy

The accuracy of the ICD2042A output frequencies depends on the target output frequencies. The tables within this document contain target frequencies which differ from the actual frequencies produced by the clock synthesizer.

The output frequencies of the ICD2042A are an integral fraction of the input (reference) frequency:

$$f_{(OUT)} = (2 \times f_{(REF)} \times \frac{P}{Q})$$

Only certain output frequencies are possible for a particular reference frequency. However, the ICD2042A always produces an output frequency within 0.1% of the target frequencies listed, which is more than sufficient to meet standard display requirements. [Actual values are available from the factory.]

3-State Output Operation

The $\overline{\text{OUTDIS}}$ signal, when pulled low, will 3-state the MCLK, PCLK and XBUF output lines. This supports wired-or connections between external clock lines (example: the Feature Connector external clock) and allows for procedures such as automated testing, where the clock must be disabled. The $\overline{\text{OUTDIS}}$ signal contains an internal pull-up, but should be tied to VDD if not used.

No External Components Required

Under normal conditions no external components are required for proper operation of any of the internal circuitry of the ICD2042A.

Circuit Description

Each oscillator block is a classical phase-locked loop connected as shown in the diagram on the first page. The external input frequency $f_{(REF)}$ is typically 14.31818 MHz (as derived from the PC system bus) and goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable "synthesized" signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO to either go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up-and-down movement of the variable frequency will ultimately lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

Minimized Parasitic Problems

All of the IC DESIGNS families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements with their output oscillator pins placed on separate sides of the package. Further, all the synthesis VCOs are separated from their digital logic. Finally, separate power and ground buses for the analog and digital circuitry are used.

The package leadframes are optimized for the lowest possible inductance from the supply pin on the package to the die within, and results in minimized supply noise problems such as ground-bounce and output crosstalk.

Stability and "Bit-Jitter"

The long-term frequency stability of the IC DESIGNS phase-locked loop frequency synthesis components is good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short-term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low-gain VCOs and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be visually unnoticeable in the graphics display.

Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2042A is inherently stable over temperature and manufacturing process variations. Incorporating the loop filter internal to the chip assures the loop filter will track the same process variations as does the VCO. With the ICD2042A, no manufacturing "tweaks" to external filter components are required as is the case with external de-coupled filters.

Ordering Information

Table 3: Order Codes

Part Number	Package Type	Temperature Range	Pixel Clock ROM Option
ICD2042A	S = 16-Pin SOIC	C = Commercial[a]	Custom Order Only

a. 0°C to +70°C

Device Specifications

Electrical Data

Table 4: Absolute Maximum Ratings

Name	Description	Min	Max	Units
V_{DD} & AV_{DD}	Supply voltage relative to GND	–0.5	7.0	Volts
V_{IN}	Input voltage with respect to GND	–0.5	V_{DD} + 0.5	Volts
T_{STOR}	Storage temperature	–65	+150	°C
T_{SOL}	Max soldering temperature (10 sec)		+260	°C
T_J	Junction temperature		+125	°C
P_{DISS}	Power dissipation		350	mWatts

NOTE: Above the Maximum Ratings, the useful life may be impaired. For user guidelines, not tested.

OPERATING RANGE: V_{DD} & AV_{DD} = +5V ±5%; 0°C ≤ $T_{AMBIENT}$ ≤ 70°C
(This applies to all specifications below.)

Table 5: DC Characteristics

Name	Description	Min	Max	Units	Conditions
V_{IH}	High-level input voltage	2.0		Volts	
V_{IL}	Low-level input voltage		0.8	Volts	
V_{OH}	High-level CMOS output voltage	V_{DD} – 0.4		Volts	I_{OH} = –4.0 mA
V_{OL}	Low-level output voltage		0.4	Volts	I_{OL} = 4.0 mA
I_{IH}	Input high current		150	µA	$V_{IH} = V_{DD}$
I_{IL}	Input low current		–250	µA	V_{IL} = 0V
I_{OZ}	Output leakage current		10	µA	(3-state)
I_{DD}	Power supply current		50	mA	(@ high frequency)
I_{ADD}	Analog power supply current		6	mA	

3

Table 6: AC Characteristics

Symbol	Name	Description	Min	Typ	Max	Units
$f_{(REF)}$	reference frequency	Reference Oscillator nominal value (Different reference frequencies require a custom ROM; standard parts use 14.31818 MHz, unless otherwise stated.)	4	14.318	25	MHz
$t_{(REF)}$	reference clock period	$1 \div f_{(REF)}$	40	69.8	250	ns
t_1	input duty cycle	Duty cycle for the input oscillator defined as $t_1 \div t_{(REF)}$	25%	50%	75%	
t_2	output period	CPUCLK oscillator value	8.3 (120 MHz)		2857 (350 KHz)	ns
t_3	output duty cycle	Duty cycle for the output oscillator defined as $t_3 \div t_2$ measured at 2.5V	40%		60%	
t_4	rise time	Rise time for the output oscillator into a 25pF load			3	ns
t_5	fall time	Fall time for the output oscillator into a 25pF load			3	ns
t_6	3-state	Time for the output oscillators to go into 3-state mode after $\overline{\text{OUTDIS}}$ signal assertion			12	ns
t_7	clk valid	Time for the output oscillators to recover from 3-state mode after $\overline{\text{OUTDIS}}$ signal goes high			12	ns
t_{MUXREF}	clk stable	Time required for the output oscillators to become valid after P0–3 or M0–2 select signals change value	3.4	5	6.9	msec
t_{freq1}	freq1 output	Old frequency output				
t_{freq2}	freq2 output	New frequency output				
t_A	$f_{(REF)}$ mux time	Time clock output remains high while output muxes to reference frequency	$\frac{t_{(REF)}}{2}$		$3\frac{t_{(REF)}}{2}$	
t_B	t_{freq2} mux time	Time clock output remains high while output muxes to new frequency value	$\frac{t_{freq2}}{2}$		$3\frac{t_{freq2}}{2}$	

NOTE: Input capacitance is typically 10pF, except for the crystal pads.

Timing Diagrams

Fig. 3: Rise and Fall Times

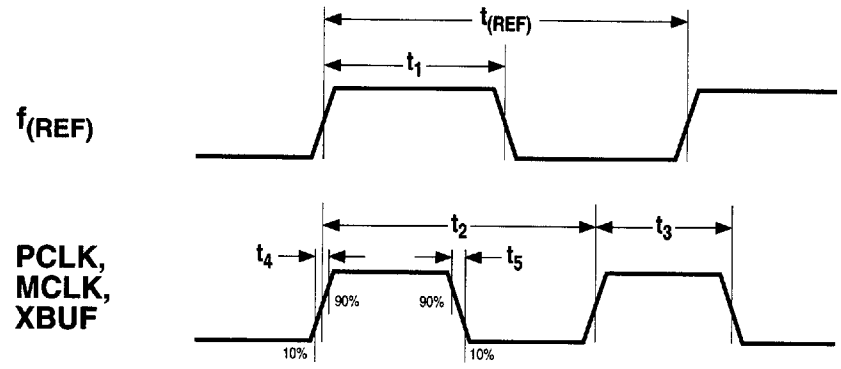


Fig. 4: 3-StateTiming

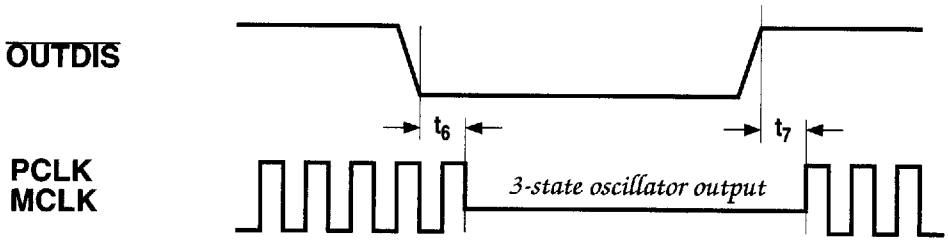
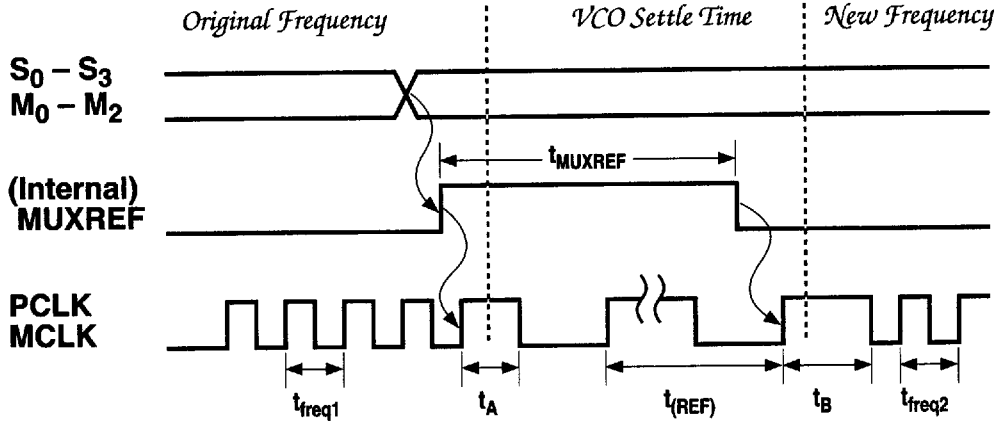


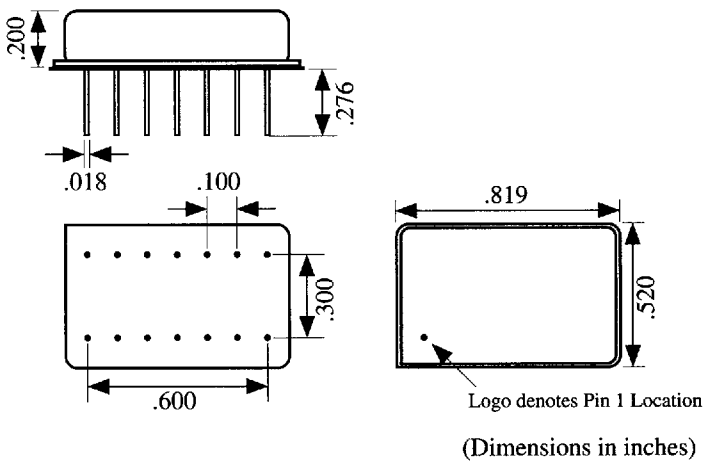
Fig. 5: Selection Timing



14-Pin Packages

Table 1: 14-Pin Metal Can Outline

Package (Lead Count = 14)



(Dimensions in inches)

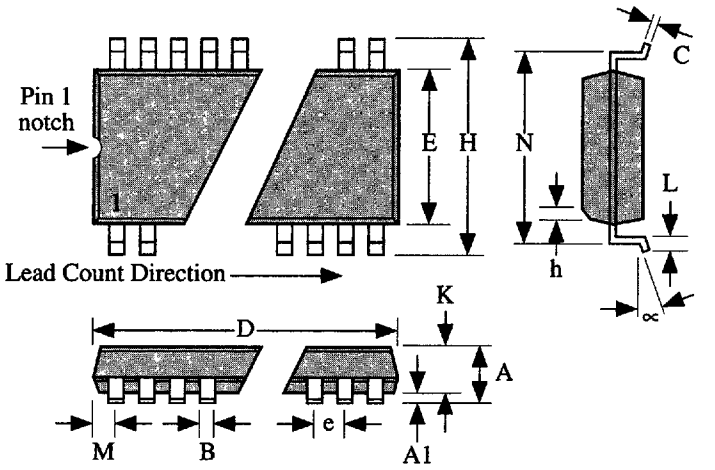
8

16-Pin Packages

Table 2: 16-Pin SOIC Outline

Symbol	MIN	MAX
A	.099	.104
A1	.004	.009
B	.014	.019
C	.010	REF
D	.405	.410
E	.294	.299
e	.050	TYP
H	.402	.419
h	.025 x	45°
L	.030	.040
∝	0°	8°
K	.088	.098
M	.020	.030
N	.335	.351

Package (Lead Count = 16)

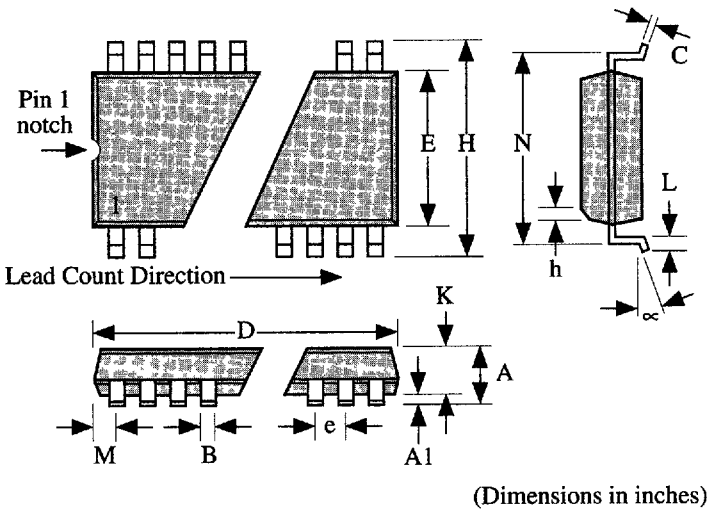


20-Pin Packages

Table 3: 20-Pin SOIC Outline

Symbol	MIN	MAX
A	.099	.104
A1	.004	.009
B	.014	.019
C	.010	REF
D	.505	.512
E	.294	.299
e	.050	TYP
H	.402	.419
h	.025 x 45°	
L	.030	.040
∝	0°	8°
K	.088	.098
M	.020	.030
N	.335	.351

Package (Lead Count = 20)



(Dimensions in inches)

8