60V, 0.010 Ohm, 75A, N-Channel, Logic Level UltraFET Power MOSFETs

These N-Channel power MOSFETs are manufactured using the innovative UltraFET™ process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

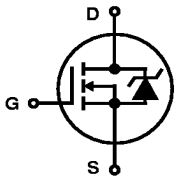
Features

- *Ultra Low On-Resistance*, $r_{DS(ON)} = 0.009\Omega$, $V_{GS}=10V$
  $r_{DS(ON)} = 0.010\Omega$, $V_{GS}=5V$
- *Temperature Compensating* PSPICE and SABER Models
- *Thermal Impedance* PSPICE and SABER Models
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Switching Time vs R_{GS} Curves

Applications

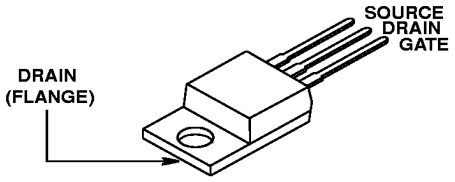
- *Automotive*
- *Industrial*
- *Power Management*

Symbol



Packaging

JEDEC TO-220AB



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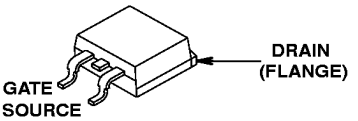
JEDEC TO-263AB



HUF76444S3S

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	60	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	60	V
Gate to Source Voltage	V_{GS}	±16	V
Drain Current			
Continuous ($T_C = 25^oC$, V_{GS} = 5V)	I_D	75	A
Continuous ($T_C = 25^oC$, V_{GS} = 10V)	I_D	75	A
Continuous ($T_C = 100^oC$, V_{GS} = 5V)	I_D	75	A
Continuous ($T_C = 100^oC$, V_{GS} = 4.5V)	I_D	75	A
Pulsed Drain Current	I_{DM}	TBD	
Pulsed Avalanche Rating	UIS	0.3	A^2s
Power Dissipation	P_D	275	W
Derate Above 25^oC		1.85	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS						
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V	60	-	-	V
		I_D = 250μA, V_{GS} = 0V, $T_C = -40^oC$	55	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 55V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 50V, V_{GS} = 0V, $T_C = 150^oC$	-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±16V	-	-	±100	nA
ON STATE SPECIFICATIONS						
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA	1	-	-	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 75A, V_{GS} = 10V	-	0.0075	0.009	Ω
		I_D = 75A, V_{GS} = 5V	-	0.0083	0.010	Ω
		I_D = 75A, V_{GS} = 4.5V	-	0.0083	0.010	Ω
THERMAL SPECIFICATIONS						
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-220 and TO-263	-	-	0.54	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	62	$^oC/W$
SWITCHING SPECIFICATIONS (V_{GS} = 4.5V)						
Turn-On Time	t_{ON}	V_{DD} = 30V, $I_D \cong$ 75A, R_L = 0.40Ω, V_{GS} = 4.5V, R_{GS} = 2.5Ω	-	-	250	ns
Turn-On Delay Time	$t_{d(ON)}$		-	22	-	ns
Rise Time	t_r		-	145	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	35	-	ns
Fall Time	t_f		-	30	-	ns
Turn-Off Time	t_{OFF}		-	-	100	ns

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
SWITCHING SPECIFICATIONS (V_{GS} = 10V)							
Turn-On Time	t_{ON}	V_{DD} = 30V, $I_D \cong$ 75A, R_L = 0.40Ω, V_{GS} = 10V, R_{GS} = 2.5Ω		-	-	105	ns
Turn-On Delay Time	$t_{d(ON)}$			-	15	-	ns
Rise Time	t_r			-	56	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	45	-	ns
Fall Time	t_f			-	35	-	ns
Turn-Off Time	t_{OFF}			-	-	120	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 30V, $I_D \cong$ 75A, R_L = 0.40Ω $I_{g(REF)}$ = 1.0mA	-	113	135	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0V to 5V		-	63	76	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 1V		-	4.3	5.2	nC
Gate to Source Gate Charge	Q_{gs}			-	12.8	-	nC
Gate to Drain Gate Charge	Q_{gd}			-	41	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	4150	-	pF
Output Capacitance	C_{OSS}			-	2000	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	425	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 75A	-	-	1.25	V
Reverse Recovery Time	t_{rr}	I_{SD} = 75A, dI_{SD}/dt = 100A/μs	-	-	105	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 75A, dI_{SD}/dt = 100A/μs	-	-	205	nC