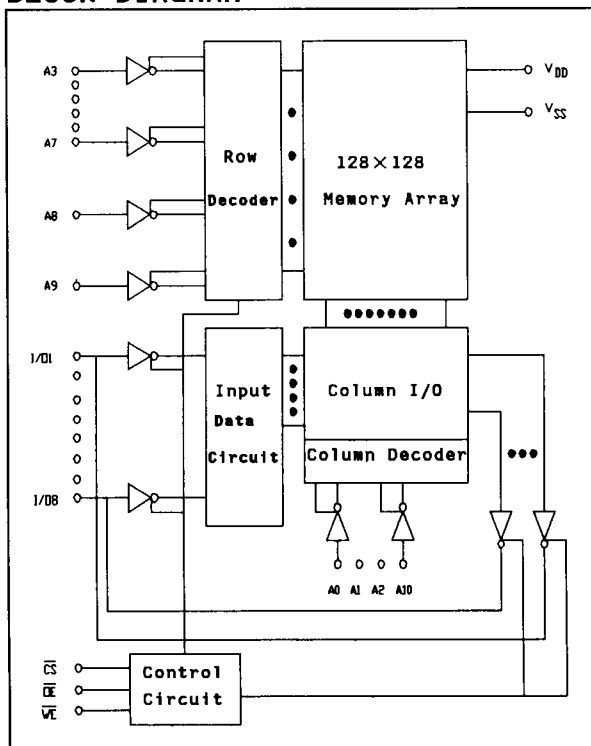
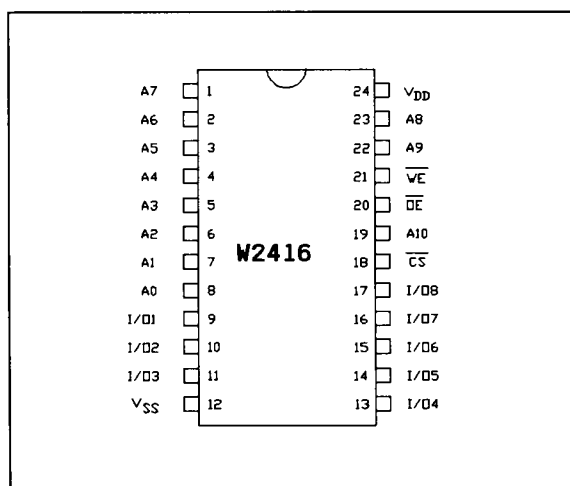


**W2416****2K X 8 CMOS STATIC RAM****FEATURES**

- Low Power Consumption :  
Active : 250mW (Typ.)  
Standby : 10  $\mu$ W(Typ.)-- L-Version
- Fast Access Time : 70/100 ns (Max.)
- Single +5V Supply
- Fully Static Operation
- Direct TTL Compatible : All Inputs and Outputs
- Three State Outputs
- Capability of Battery Back Up Operation (L-Version)
- Data Retention Voltage : 2V (Min.) (L-Version)
- Available in 24 Pin DIP, SOP, or Skinny DIP Packages

**BLOCK DIAGRAM****DESCRIPTION**

The W2416 is a High Speed, Low Power CMOS Static RAM Organized as 2048 $\times$ 8 Bits and Operates on a Single 5-Volt Supply. It is Manufactured Using WINBOND's High Performance CMOS Technology.

**PIN CONFIGURATION****PIN DESCRIPTION**

| SYMBOL          | DESCRIPTION         |
|-----------------|---------------------|
| A0 - A10        | Address Inputs      |
| I/O1-I/O8       | Data Inputs/Outputs |
| $\overline{CS}$ | Chip Select Input   |
| $\overline{WE}$ | Write Enable Input  |
| $\overline{OE}$ | Output Enable Input |
| $V_{DD}$        | Power Supply        |
| $V_{SS}$        | Ground              |

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## DC CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS

| PARAMETER                            | RATING               | UNIT |
|--------------------------------------|----------------------|------|
| Supply Voltage to $V_{SS}$ Potential | -0.5 to +7.0         | V    |
| Inputs/Outputs to $V_{SS}$ Potential | -0.5 to $V_{DD}+0.5$ | V    |
| Allowable Power Dissipation          | 1.0                  | W    |
| Storage Temperature                  | -55 to +150          | °C   |
| Operating Temperature                | 0 to +70             | °C   |

### TRUTH TABLE

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | Mode           | I/O1 - I/O8 | $V_{DD}$ Current     |
|-----------------|-----------------|-----------------|----------------|-------------|----------------------|
| H               | X               | X               | Not Selected   | High Z      | $I_{SB}$ , $I_{SB1}$ |
| L               | H               | H               | Output Disable | High Z      | $I_{DD}$             |
| L               | L               | H               | Read           | Data Out    | $I_{DD}$             |
| L               | X               | L               | Write          | Data In     | $I_{DD}$             |

### OPERATING CHARACTERISTICS

( $V_{DD}=5V \pm 10\%$ ,  $V_{SS}=0V$ ,  $T_a=0$  to  $70^\circ\text{C}$ )

| PARAMETER                         | SYMBOL    | TEST CONDITIONS                                                                                                       | MIN.  | TYP. | MAX.           | UNIT               |
|-----------------------------------|-----------|-----------------------------------------------------------------------------------------------------------------------|-------|------|----------------|--------------------|
| Input Low Voltage                 | $V_{IL}$  | -                                                                                                                     | - 0.5 | -    | + 0.8          | V                  |
| Input High Voltage                | $V_{IH}$  | -                                                                                                                     | + 2.2 | -    | $V_{DD} + 0.5$ | V                  |
| Input Leakage Current             | $I_{LI}$  | $V_{IN}= V_{SS}$ to $V_{DD}$                                                                                          | - 2   | -    | + 2            | $\mu\text{A}$      |
| Output Leakage Current            | $I_{LO}$  | $V_{I/O} = V_{SS}$ to $V_{DD}$<br>$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or<br>$\overline{WE} = V_{IL}$ | - 2   | -    | + 2            | $\mu\text{A}$      |
| Output Low Voltage                | $V_{OL}$  | $I_{OL} = +4.0\text{mA}$                                                                                              | -     | -    | 0.4            | V                  |
| Output High Voltage               | $V_{OH}$  | $I_{OH} = -1.0\text{mA}$                                                                                              | 2.4   | -    | -              | V                  |
| Operating Power<br>Supply Current | $I_{DD}$  | $\overline{CS} = V_{IL}$ , I/O = 0mA<br>CYCLE = MIN, DUTY = 100%                                                      | -     | -    | 80             | mA                 |
| Standby Power<br>Supply Current   | $I_{SB}$  | $\overline{CS} = V_{IH}$                                                                                              | -     | -    | 3              | mA                 |
|                                   | $I_{SB1}$ | $\overline{CS} \geq V_{DD} - 0.2V$                                                                                    | L     | -    | 2              | 100 $\mu\text{A}$  |
|                                   |           |                                                                                                                       | S     | -    | -              | 1000 $\mu\text{A}$ |

Note : Typical characteristics are at  $V_{DD}=5V$ ,  $T_a=25^\circ\text{C}$ .

## CAPACITANCE

( $V_{DD}=5V$ ,  $T_a=25^{\circ}C$ ,  $f=1MHz$ )

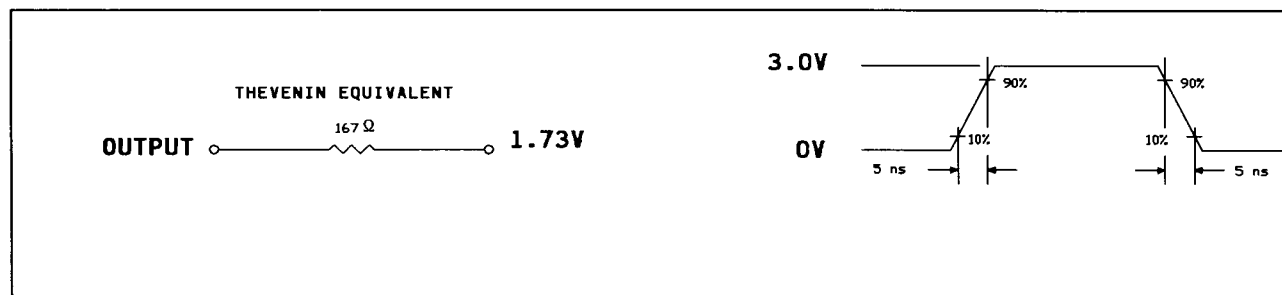
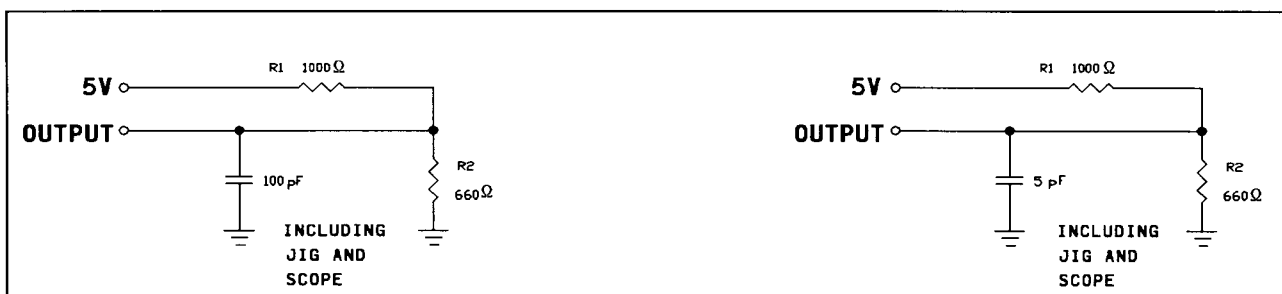
| PARAMETER                | SYMBOL    | CONDITIONS   | MAX. | UNIT |
|--------------------------|-----------|--------------|------|------|
| Input Capacitance        | $C_{IN}$  | $V_{IN}=0V$  | 6    | pF   |
| Input/Output Capacitance | $C_{I/O}$ | $V_{OUT}=0V$ | 8    | pF   |

Note : This parameter is sampled and not 100% tested.

## AC TEST CONDITIONS

| PARAMETER                               | CONDITIONS                             |
|-----------------------------------------|----------------------------------------|
| Input Pulse Levels                      | 0V to 3V                               |
| Input Rise and Fall Times               | 5ns                                    |
| Input and Output Timing Reference Level | 1.5V                                   |
| Output Load                             | $C_L=100pF$ , $I_{OH}/I_{OL}=-1mA/4mA$ |

## AC TEST LOADS AND WAVEFORMS



## AC CHARACTERISTICS

( $V_{DD}=5V \pm 10\%$ ,  $V_{SS}=0V$ ,  $T_a=0$  to  $70^\circ C$ )

### (1) READ CYCLE

| PARAMETER                            | SYMBOL    | W2416-70 |      | W2416-10 |      | UNIT |
|--------------------------------------|-----------|----------|------|----------|------|------|
|                                      |           | MIN.     | MAX. | MIN.     | MAX. |      |
| Read Cycle Time                      | $T_{RC}$  | 70       | -    | 100      | -    | ns   |
| Address Access Time                  | $T_{AA}$  | -        | 70   | -        | 100  | ns   |
| Chip Select Access Time              | $T_{ACS}$ | -        | 70   | -        | 100  | ns   |
| Output Enable to Output Valid        | $T_{AOE}$ | -        | 35   | -        | 50   | ns   |
| Chip Selection to Output in Low Z    | $T_{CLZ}$ | 5        | -    | 5        | -    | ns   |
| Output Enable to Output in Low Z     | $T_{OLZ}$ | 5        | -    | 5        | -    | ns   |
| Chip Deselection to Output in High Z | $T_{CHZ}$ | -        | 35   | -        | 35   | ns   |
| Output Disable to Output in High Z   | $T_{OHZ}$ | -        | 30   | -        | 35   | ns   |
| Output Hold from Address Change      | $T_{OH}$  | 5        | -    | 5        | -    | ns   |

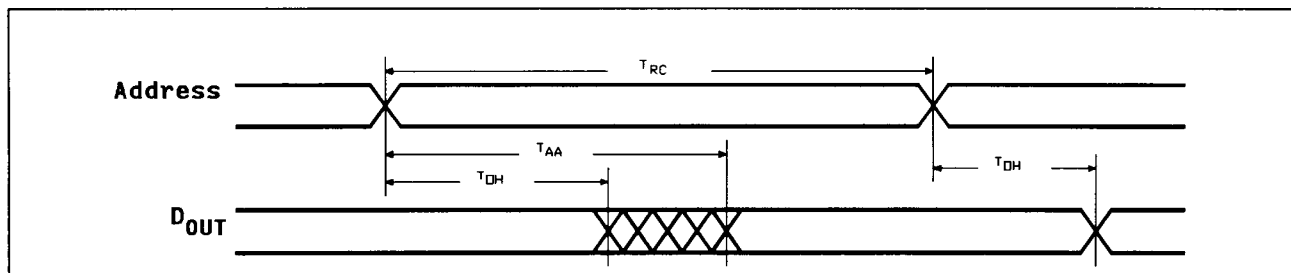
### (2) WRITE CYCLE

| PARAMETER                          |                                | SYMBOL    | W2416-70 |      | W2416-10 |      | UNIT |
|------------------------------------|--------------------------------|-----------|----------|------|----------|------|------|
|                                    |                                |           | MIN.     | MAX. | MIN.     | MAX. |      |
| Write Cycle Time                   |                                | $T_{WC}$  | 70       | -    | 100      | -    | ns   |
| Chip Selection to End of Write     |                                | $T_{CW}$  | 45       | -    | 80       | -    | ns   |
| Address Valid to End of Write      |                                | $T_{AW}$  | 50       | -    | 80       | -    | ns   |
| Address Setup Time                 |                                | $T_{AS}$  | 5        | -    | 5        | -    | ns   |
| Write Pulse Width                  |                                | $T_{WP}$  | 45       | -    | 60       | -    | ns   |
| Write Recovery Time                | $\overline{CS}, \overline{WE}$ | $T_{WR}$  | 5        | -    | 5        | -    | ns   |
| Data to Write Time Overlap         |                                | $T_{DW}$  | 30       | -    | 40       | -    | ns   |
| Data Hold from Write Time          |                                | $T_{DH}$  | 5        | -    | 5        | -    | ns   |
| Write to Output in High Z          |                                | $T_{WHZ}$ | 0        | 30   | 0        | 35   | ns   |
| Output Disable to Output in High Z |                                | $T_{OHZ}$ | 0        | 30   | 0        | 30   | ns   |
| Output Active from End of Write    |                                | $T_{OW}$  | 5        | -    | 5        | -    | ns   |

## TIMING WAVEFORMS

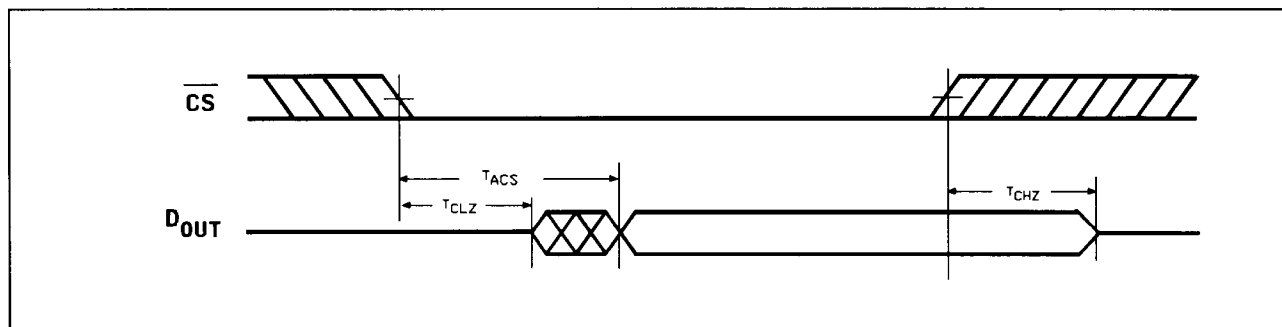
### READ CYCLE 1

(Address Controlled)



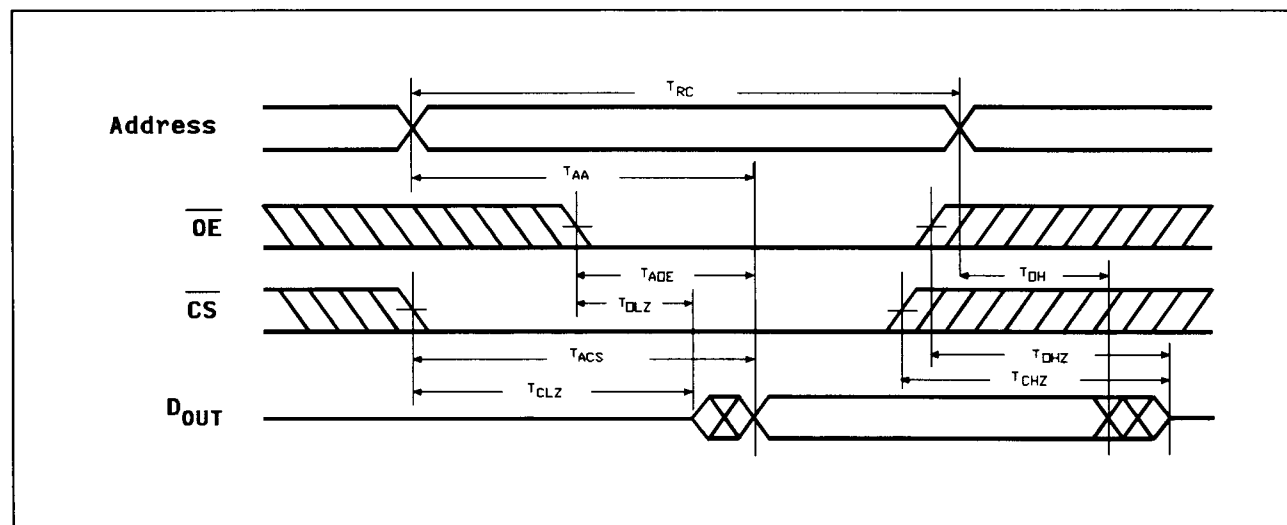
### READ CYCLE 2

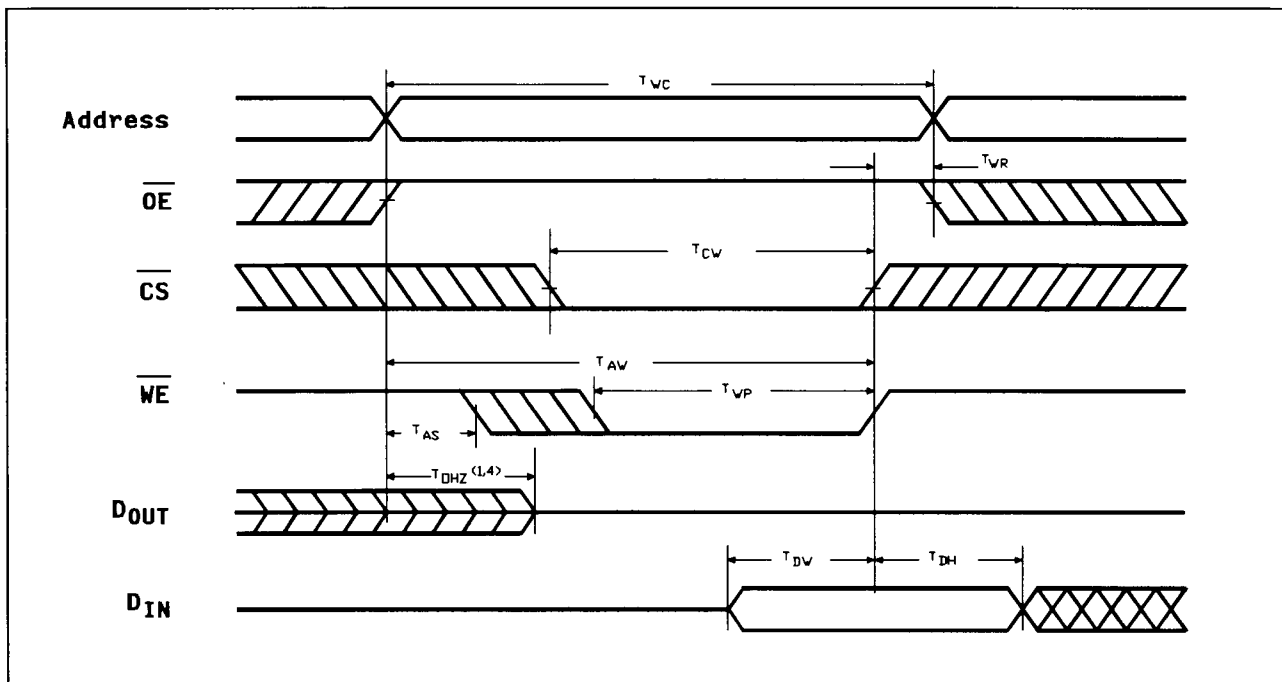
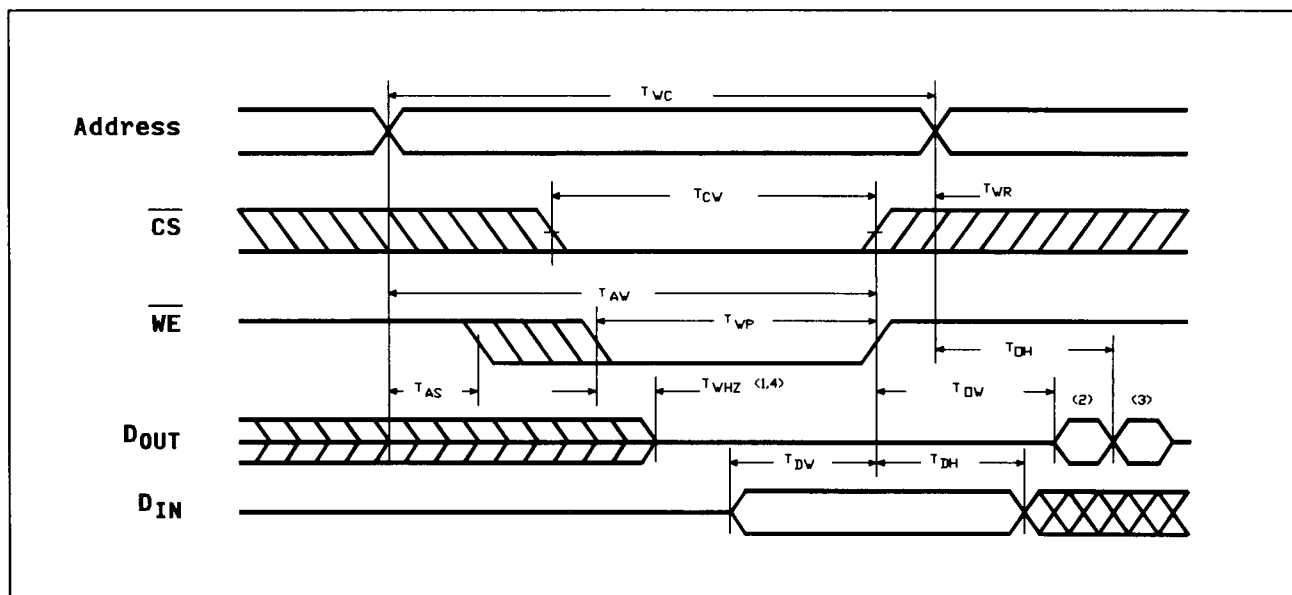
(Chip Select Controlled)



### READ CYCLE 3

(Output Enable Controlled)



**WRITE CYCLE 1**

**WRITE CYCLE 2**


## Notes:

1. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
2.  $D_{OUT}$  is the same phase of write data of this write cycle.
3.  $D_{OUT}$  is the read data of next address.
4. Transition is measured  $\pm 500\text{mV}$  from steady state with  $C_L = 5\text{pF}$ . This parameter is guaranteed and not 100% tested.

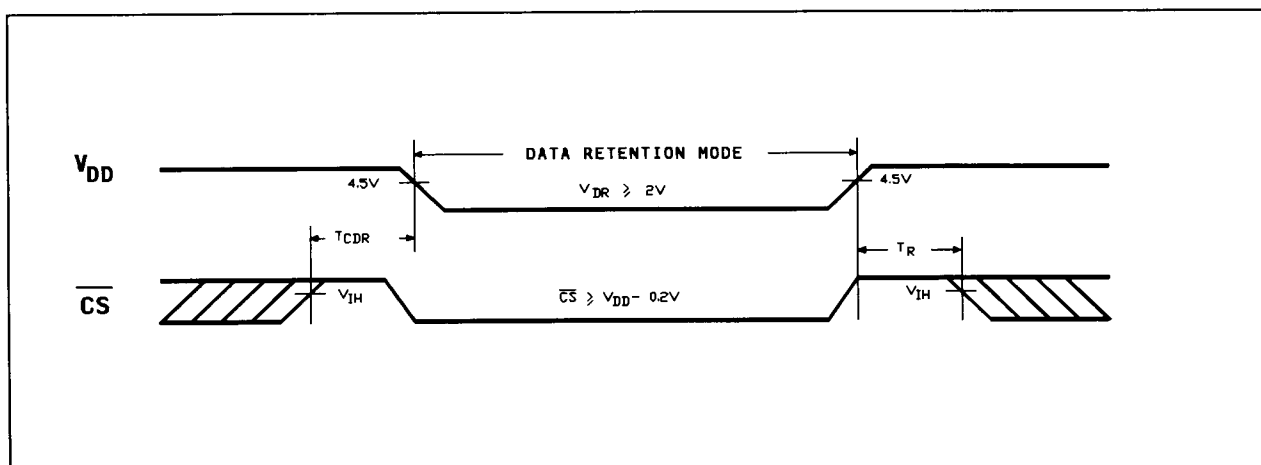
### DATA RETENTION CHARACTERISTICS

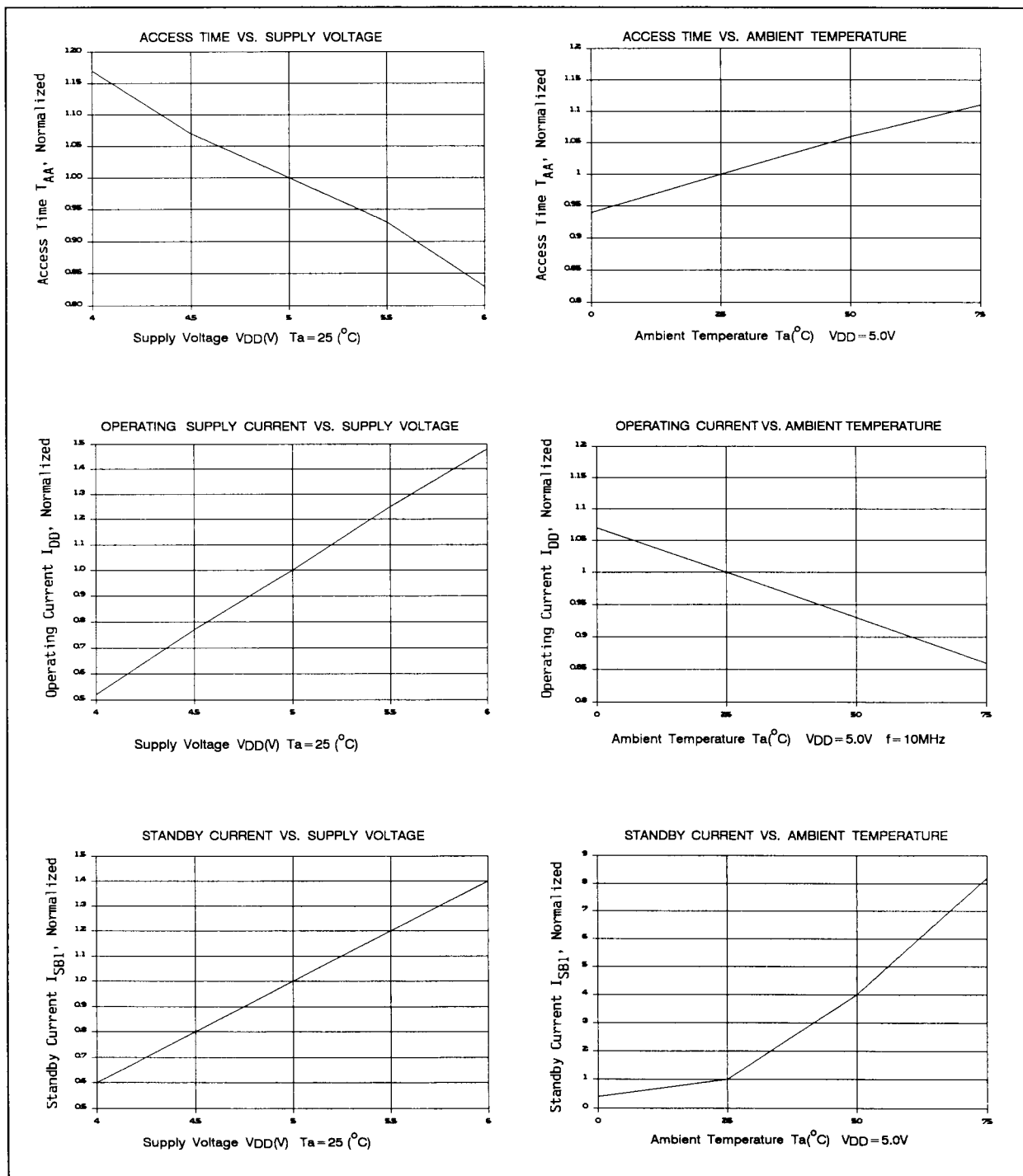
(Ta=0 to 70°C, Guaranteed Only for L-Version)

| PARAMETER                            | SYMBOL     | TEST CONDITIONS                                                   | MIN.       | TYP. | MAX. | UNIT          |
|--------------------------------------|------------|-------------------------------------------------------------------|------------|------|------|---------------|
| $V_{DD}$ for Data Retention          | $V_{DR}$   | $\overline{CS} \geq V_{DD} - 0.2\text{V}$                         | 2.0        | -    | -    | V             |
| Data Retention Current               | $I_{DDDR}$ | $\overline{CS} \geq V_{DD} - 0.2\text{V}$<br>$V_{DD} = 3\text{V}$ | -          | 2    | 50   | $\mu\text{A}$ |
| Chip Deselect to Data Retention Time | $T_{CDR}$  | See Retention Waveform                                            | 0          | -    | -    | ns            |
| Operation Recovery Time              | $T_R$      |                                                                   | $T_{RC}^*$ | -    | -    | ns            |

Note: \*  $T_{RC}$  = Read Cycle Time

### DATA RETENTION WAVEFORM



**CHARACTERISTICS CURVES**


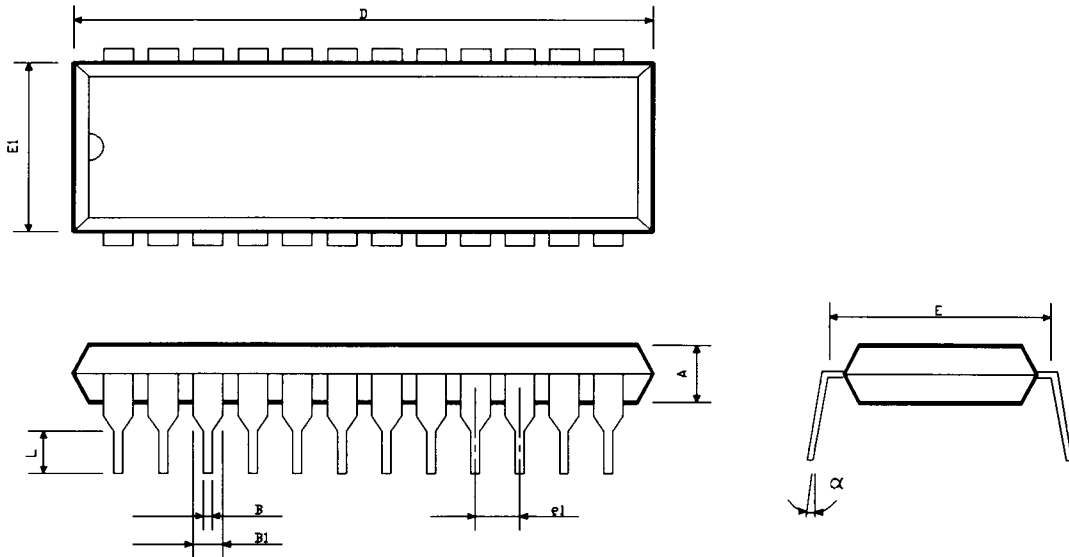
# ORDERING INFORMATION

| Part No.   | Access Time<br>(ns) | Operating<br>Current<br>Max. (mA) | Standby<br>Current<br>Max. (mA) | Package       | Remark    |
|------------|---------------------|-----------------------------------|---------------------------------|---------------|-----------|
| W2416-70   | 70                  | 80                                | 1                               | 600mil DIP    |           |
| W2416-70L  | 70                  | 80                                | 0.1                             | 600mil DIP    | Low Power |
| W2416-10   | 100                 | 80                                | 1                               | 600mil DIP    |           |
| W2416-10L  | 100                 | 80                                | 0.1                             | 600mil DIP    | Low Power |
| W2416S-70  | 70                  | 80                                | 1                               | 300mil SOP    |           |
| W2416S-70L | 70                  | 80                                | 0.1                             | 300mil SOP    | Low Power |
| W2416S-10  | 100                 | 80                                | 1                               | 300mil SOP    |           |
| W2416S-10L | 100                 | 80                                | 0.1                             | 300mil SOP    | Low Power |
| W2416K-70  | 70                  | 80                                | 1                               | 300mil Skinny |           |
| W2416K-70L | 70                  | 80                                | 0.1                             | 300mil Skinny | Low Power |
| W2416K-10  | 100                 | 80                                | 1                               | 300mil Skinny |           |
| W2416K-10L | 100                 | 80                                | 0.1                             | 300mil Skinny | Low Power |

## Notes:

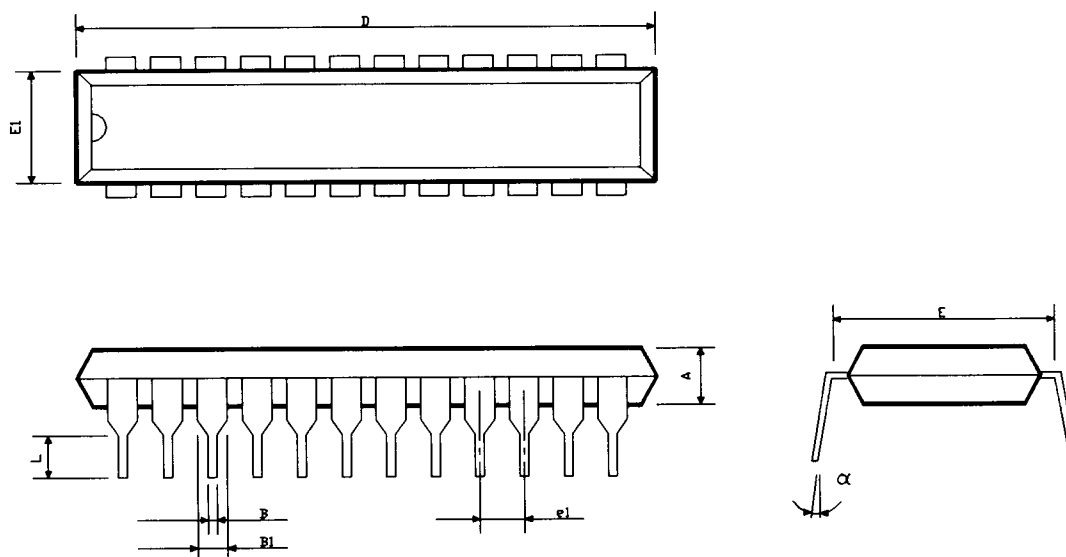
1. Winbond Electronics Corp. reserves the right to make changes to its products without prior notice, in order to improve design and performance.
2. If such products are to be used in applications in which personal injury might occur from failure, purchaser must do its own quality assurance testing appropriate to such application.

# **PACKAGE DIMENSION** **24 LEAD P-DIP**

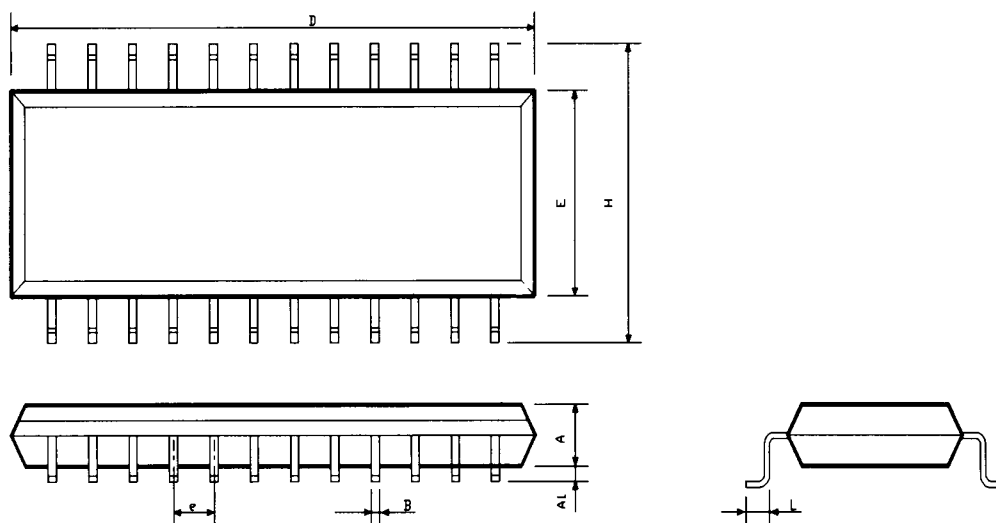


| Symbol   | Dimensions in inch     | Dimensions in mm       |
|----------|------------------------|------------------------|
| A        | $0.155 \pm 0.005$      | $3.937 \pm 0.127$      |
| B        | $0.018 \pm 0.004$      | $0.457 \pm 0.102$      |
| B1       | $0.060 \pm 0.004$      | $1.524 \pm 0.102$      |
| D        | $1.250 \pm 0.010$      | $31.750 \pm 0.254$     |
| E        | $0.600 \pm 0.010$      | $15.240 \pm 0.254$     |
| E1       | $0.550 \pm 0.010$      | $13.970 \pm 0.254$     |
| e1       | $0.100 \pm 0.010$      | $2.540 \pm 0.254$      |
| L        | $0.135 \pm 0.010$      | $3.429 \pm 0.254$      |
| $\alpha$ | $0^\circ \sim 7^\circ$ | $0^\circ \sim 7^\circ$ |

## 24 LEAD P-DIP SKINNY



| Symbol   | Dimensions in inch     | Dimensions in mm       |
|----------|------------------------|------------------------|
| A        | $0.130 \pm 0.005$      | $3.302 \pm 0.127$      |
| B        | $0.018 \pm 0.004$      | $0.457 \pm 0.102$      |
| B1       | $0.060 \pm 0.004$      | $1.524 \pm 0.102$      |
| D        | $1.250 \pm 0.010$      | $31.877 \pm 0.254$     |
| E        | $0.300 \pm 0.010$      | $7.620 \pm 0.254$      |
| E1       | $0.260 \pm 0.010$      | $6.604 \pm 0.254$      |
| e1       | $0.100 \pm 0.010$      | $2.540 \pm 0.254$      |
| L        | $0.130 \pm 0.010$      | $3.302 \pm 0.254$      |
| $\alpha$ | $0^\circ \sim 7^\circ$ | $0^\circ \sim 7^\circ$ |

**24 LEAD SO NARROW BODY**


| Symbol | Dimensions in inch | Dimensions in mm   |
|--------|--------------------|--------------------|
| A      | $0.091 \pm 0.006$  | $2.311 \pm 0.152$  |
| A1     | $0.008 \pm 0.003$  | $0.203 \pm 0.076$  |
| B      | $0.016 \pm 0.003$  | $0.406 \pm 0.076$  |
| D      | $0.606 \pm 0.004$  | $15.392 \pm 0.102$ |
| E      | $0.295 \pm 0.004$  | $7.493 \pm 0.102$  |
| e      | $0.050 \pm 0.008$  | $1.270 \pm 0.203$  |
| H      | $0.406 \pm 0.008$  | $10.312 \pm 0.203$ |
| L      | $0.036 \pm 0.006$  | $0.914 \pm 0.152$  |



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Note: All data and specifications are subject to change without notice.