Telmos
TELMOS INC.

TMD54HC 373/TMD74HC 373
3 STATE OCTAL LATCHES
TMD54HC 374/TMD74HC 374
3 STATE OCTAL D-FLIP-FLOPS

- CMOS INPUT COMPATIBLE
- 13 NS PROPAGATION DELAY TYP.
- 1 μA MAX. INPUT CURRENT
- DRIVES 30 LS-TTL LOADS
- FULL PARALLEL LOAD ACCESS
- 3 STATE BUS-DRIVING OUTPUTS
- HIGH NOISE IMMUNITY
- MEETS OR EXCEEDS JEDEC STANDARD NUMBER 7

Description

The 373 and 374 series octal latches and flip-flops use a 3 micron silicon gate P-well CMOS process. They have the ability to drive 30 LS TTL loads in addition to possessing high noise immunity and low power consumption. These devices are ideally suited for interfacing with bus lines in a bus organized system. These 8 bit registers feature three-state outputs designed specifically for driving high capacitive or relatively low impedance loads. When driving a bus no interface or pull-up resistors are required.

When the LATCH ENABLE input of the 373HC is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state.

The 374HC contains positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, is transferred to the Q outputs on positive going transitions of the clock (CK) input. Application of a high level to the OUTPUT CONTROL (OC) input causes all outputs to go to a high impedance state.

This 54HC/74HC family is pinout, function and speed compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal clamps to V_{CC} and ground.

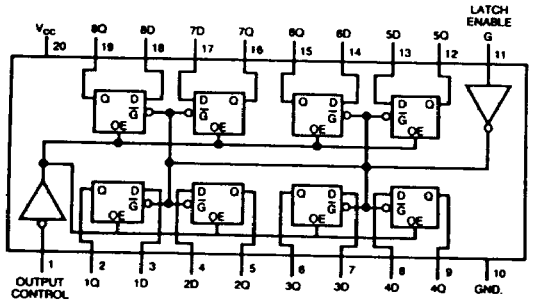
All unused inputs must be connected to an appropriate logic voltage level (either V_{CC} or GND).

PRELIMINARY

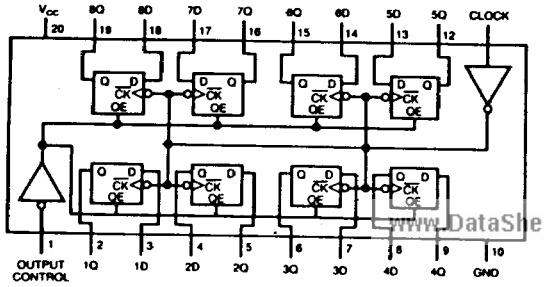
Ordering Information

RANGE	PART NUMBER	TYPE	PACKAGE
INDUSTRIAL TEMP. RANGE	TMD74HC373	OCTAL LATCH	20 PIN PLASTIC
	TMD74HC374	FLIP-FLOP	20 PIN PLASTIC
MILITARY TEMP. RANGE	TMD54HC373	OCTAL LATCH	20 PIN CERDIP
	TMD54HC374	FLIP-FLOP	20 PIN CERDIP

TMD54HC373/TMD74HC373



TMD54HC374/TMD74HC374



Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 +7.0V
DC Input Voltage (V_{IN})	− .5 to V_{CC} + .5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±50 mA
DC Output Current, per pin (I_{OUT})	±50 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±100 mA
Latch up current	±100 mA
Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
TMD74HC	−40	+85	°C
TMD54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics

V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C Typ		74HC T_A = −40 to 85°C Guaranteed Limits	54HC T_A = −55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 20 uA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 6ma	4.5V	4.3	4.0	3.9	3.8	V
		$\|I_{OUT}\|$ = 15ma	6.0V	5.6	5.2	5.1	5.0	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 20 uA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 12ma	4.5V	0.2	0.4	0.4	0.4	V
		$\|I_{OUT}\|$ = 24ma	6.0V	0.3	0.5	0.5	–	V
T_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
T_{OZ}	Maximum 3-State Output Leakage Current	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND Enable = V_{IN}	6.0V		±0.5	±5.0	±10.0	μA
T_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND $\|I_{OUT}\|$ = 0 uA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation Temperature derating-plastic package: – 12mW/°C from 65°C to 85°C; cerdip package: –12mW/°C from 100°C to 125°C.

AC Electrical Characteristics TMD54HCT373/TMD74HCT373

V_{CC} = 2.0-6.0V, C_L = 50 pF, $t_r = t_f$ = 6ns (unless otherwise specified) (see note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C Typ		74HC T_A = −40 to 85°C Guaranteed Limits	54H T_A = −55 to 125°C Guaranteed Limits	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay Data To Output	C_L = 50 pF	2.0V	35	100	130	150	ns
		C_L = 150 pF	2.0V	50	140	180	210	ns
		C_L = 50 pF	4.5V	13	20	25	28	ns
		C_L = 150 pF	4.5V	19	26	33	37	ns
		C_L = 50 pF	6.0V	11	18	23	26	ns
		C_L = 150 pF	6.0V	15	24	30	34	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay LE To Output	C_L = 50 pF	2.0V	40	110	140	160	ns
		C_L = 150 pF	2.0V	60	150	190	220	ns
		C_L = 50 pF	4.5V	15	25	30	33	ns
		C_L = 150 pF	4.5V	20	33	40	44	ns
		C_L = 50 pF	6.0V	13	22	26	29	ns
		C_L = 150 pF	6.0V	17	30	35	38	ns
t_{PZL}, t_{PZH}	Maximum Enable Propagation Delay Control To Output	R_L = 1 k						
		C_L = 50 pF	2.0V	30	90	120	140	ns
		C_L = 150 pF	2.0V	45	130	170	200	ns
		C_L = 50 pF	4.5V	14	24	29	33	ns
		C_L = 150 pF	4.5V	19	32	39	44	ns
		C_L = 50 pF	6.0V	12	20	25	28	ns
		C_L = 150 pF	6.0V	16	27	33	37	ns
t_{PLZ}, t_{PHZ}	Maximum Disable Propagation Delay Control To Output	R_L = 1 K	2.0V	30	120	140	1160	ns
		C_L = 50 pF	4.5V	15	30	34	37	ns
			6.0V	12	26	29	31	ns
t_S	Minimum Set Up Time		2.0V		20	25	30	ns
			4.5V		5	6	7	ns
			6.0V		5	6	7	ns
t_H	Minimum Hold Time		2.0V		40	50	60	ns
			4.5V		10	13	15	ns
			6.0V		10	13	15	ns
t_W	Minimum Pulse Width		2.0V	23	60	75	90	ns
			4.5V	7	14	17	20	ns
			6.0V	6	12	14	17	ns
t_{TLH} t_{THL}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0V	15	40	50	60	ns
			4.5V	6	12	15	18	ns
			6.0V	5	10	13	15	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Output Control	Enable G	Data	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level
Q_0 = level of output before steady-state input conditions were established.
Z = high impedance

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

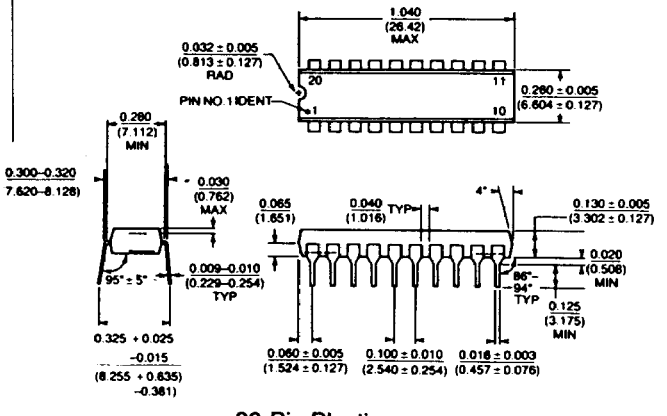
H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Q_0 = The level of the output before steady state input conditions were established.

AC Electrical Characteristics TMD54HCT374/TMD74HCT374

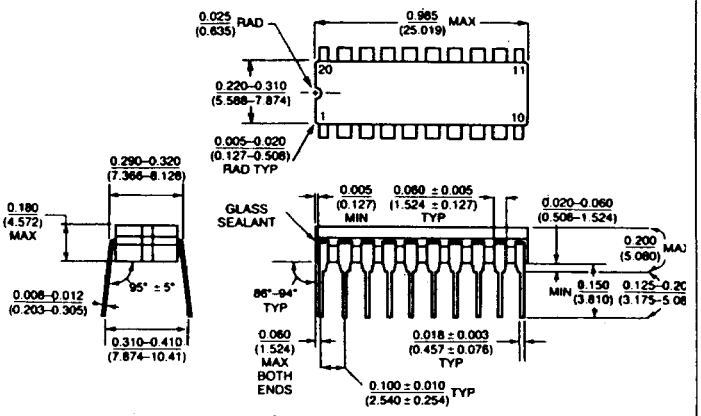
V_{CC} = 2.0-6.0V, C_L = 50 pF, $t_r = t_f$ = 6ns (unless otherwise specified) (see note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C Typ	74HC T_A = −40 to 85°C Guaranteed Limits	54H T_A = −55 to 125°C Guaranteed Limits	Units
f_{MAX}	Maximum Clock Frequency	C_L = 50 pF	2.0V	8	6.5	5.5	MHZ
			4.5V	35	30	25	MHZ
			6.0V	40	35	30	MHZ
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output	C_L = 50 pF	2.0V	45 120	150	170	ns
		C_L = 150 pF	2.0V	60 160	200	225	ns
		C_L = 50 pF	4.5V	15 26	31	34	ns
		C_L = 150 pF	4.5V	20 35	41	45	ns
		C_L = 50 pF	6.0V	13 22	26	29	ns
		C_L = 150 pF	6.0V	17 30	35	38	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control To Output	R_L = 1 k					
		C_L = 50 pF	2.0V	30 90	120	140	ns
		C_L = 150 pF	2.0V	45 130	170	200	ns
		C_L = 50 pF	4.5V	14 24	29	33	ns
		C_L = 150 pF	4.5V	19 32	39	44	ns
		C_L = 50 pF	6.0V	12 20	25	28	ns
		C_L = 150 pF	6.0V	16 27	33	37	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control To Output	R_L = 1 K	2.0V	30 120	140	160	ns
		C_L = 50 pF	4.5V	15 30	34	37	ns
			6.0V	12 26	29	31	ns
t_S	Minimum Set Up Time Data To Clock		2.0V	45	60	75	ns
			4.5V	15	17	19	ns
			6.0V	12	14	16	ns
t_H	Minimum Hold Time Clock To Data		2.0V	20	25	30	ns
			4.5V	5	5	5	ns
			6.0V	5	5	5	ns
t_W	Minimum Clock Pulse Width		2.0V	23 60	75	90	ns
			4.5V	7 14	17	20	ns
			6.0V	6 12	14	17	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0V	15 40	50	60	ns
			4.5V	6 12	15	18	ns
			6.0V	5 10	13	15	ns
C_{IN}	Maximum Input Capacitance			5 10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10 20	20	20	pF

Note 4 Refer to JEDEC standard No. 7 for AC switching waveforms and test circuits.



20-Pin Plastic



20-Pin Cerdip

All dimensions in inches (millimeters)

7/84 Printed in U.S.A.