Octal 16-/14-/12-Bit Rail-to-Rail DACs in 16-Lead SSOP

FEATURES

- **Smallest Pin Compatible Octal DACs:**
  LTC2600: 16 Bits
  LTC2610: 14 Bits
  LTC2620: 12 Bits
- **Guaranteed 16-Bit Monotonic Over Temperature**
- Tiny 16-Lead Narrow SSOP Package
- Wide 2.5V to 5.5V Supply Range
- Low Power Operation: 250µA per DAC at 3V
- Individual Channel Power-Down to 1µA, Max
- Ultralow Crosstalk between DACs (<10µV)
- High Rail-to-Rail Output Drive (±15mA, Min)
- Double-Buffered Digital Inputs
- Pin-Compatible 10-/8-Bit Versions (LTC1660/LTC1665)

APPLICATIONS

- Mobile Communications
- Process Control and Industrial Automation
- Instrumentation
- Automatic Test Equipment

DESCRIPTION

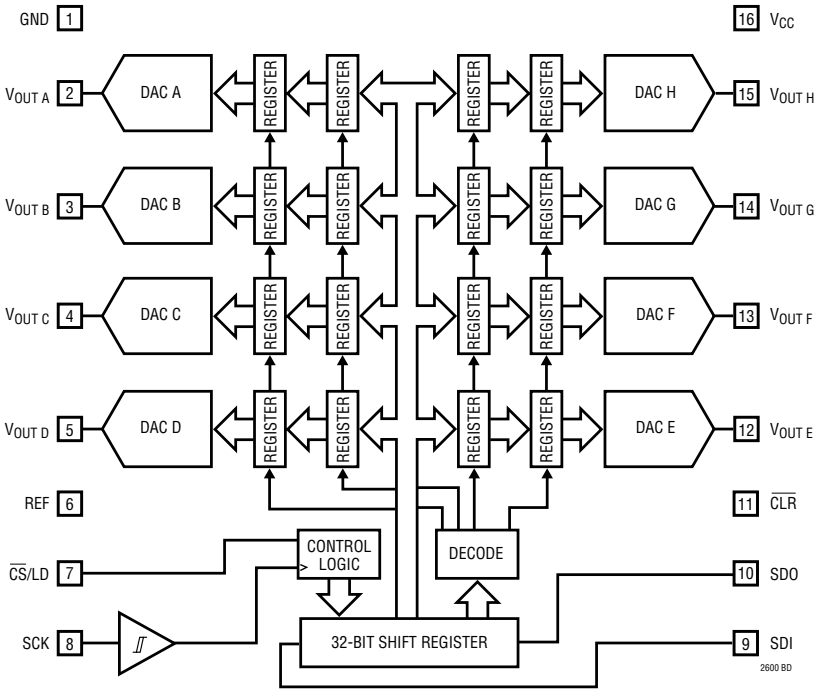
The LTC®2600/LTC2610/LTC2620 are octal 16-, 14- and 12-bit, 2.5V-to-5.5V rail-to-rail voltage-output DACs in 16-lead narrow SSOP packages. They have built-in high performance output buffers and are guaranteed monotonic.

These parts establish new board-density benchmarks for 16- and 14-bit DACs and advance performance standards for output drive, crosstalk and load regulation in single-supply, voltage-output multiples.

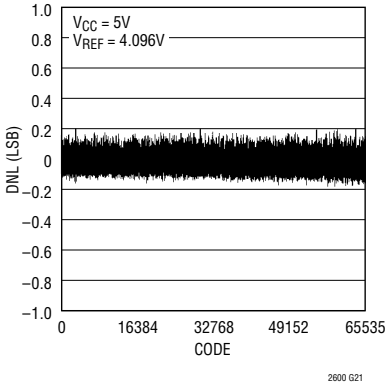
The parts use a simple SPI/MICROWIRE™ compatible 3-wire serial interface which can be operated at clock rates up to 50MHz. Daisy-chain capability and a hardware $\overline{CLR}$ function are included.

The LTC2600/LTC2610/LTC2620 incorporate a power-on reset circuit. During power-up, the voltage outputs rise less than 10mV above zero scale; and after power-up, they stay at zero scale until a valid write and update take place.

BLOCK DIAGRAM



Differential Nonlinearity (LTC2600)

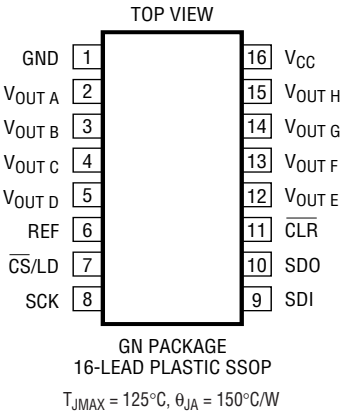


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Any Pin to GND ..... –0.3V to 6V
Any Pin to V_{CC} ..... –6V to 0.3V
Maximum Junction Temperature ..... 125°C
Operating Temperature Range
LTC2600C/LTC2610C/LTC2620C ..... 0°C to 70°C
LTC2600I/LTC2610I/LTC2620I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC2600CGN LTC2600IGN LTC2610CGN LTC2610IGN LTC2620CGN LTC2620IGN
GN PART MARKING
2600 2600I 2610 2610I 2620 2620I

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.5V to 5.5V, $V_{REF} \leq V_{CC}$, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITONS		LTC2620 MIN	LTC2620 TYP	LTC2620 MAX	LTC2610 MIN	LTC2610 TYP	LTC2610 MAX	LTC2600 MIN	LTC2600 TYP	LTC2600 MAX	UNITS
DC Performance													
	Resolution		●	12			14			16			Bits
	Monotonicity	V_{CC} = 5V, V_{REF} = 4.096V (Note 2)	●	12			14			16			Bits
DNL	Differential Nonlinearity	V_{CC} = 5V, V_{REF} = 4.096V (Note 2)	●			±0.5			±1			±1	LSB
INL	Integral Nonlinearity	V_{CC} = 5V, V_{REF} = 4.096V (Note 2)	●		±0.75	±4		±3	±16		±12	±64	LSB
	Load Regulation	V_{REF} = V_{CC} = 5V, Midscale											
		I_{OUT} = 0mA to 15mA Sourcing	●		0.025	0.125		0.1	0.5		0.3	2	LSB/mA
		I_{OUT} = 0mA to 15mA Sinking	●		0.025	0.125		0.1	0.5		0.3	2	LSB/mA
		V_{REF} = V_{CC} = 2.5V, Midscale											
		I_{OUT} = 0mA to 7.5mA Sourcing	●		0.05	0.25		0.2	1		0.8	4	LSB/mA
		I_{OUT} = 0mA to 7.5mA Sinking	●		0.05	0.25		0.2	1		0.8	4	LSB/mA

SYMBOL	PARAMETER	CONDITIONS		LTC2600/LTC2610/LTC2620 MIN	TYP	MAX	UNITS
DC Performance							
ZSE	Zero-Scale Error	V_{CC} = 5V, V_{REF} = 4.096V Code = 0	●		1	9	mV
V_{OS}	Offset Error	V_{CC} = 5V, V_{REF} = 4.096V, (Note 7)	●		±1	±9	mV
	V_{OS} Temperature Coefficient				1.7		µV/°C
GE	Gain Error	V_{CC} = 5V, V_{REF} = 4.096V	●		±0.2	±0.7	%FSR
	Gain Temperature Coefficient				6.5		ppm/°C
PSR	Power Supply Rejection	V_{CC} = ±10%			–80		dB

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.5V to 5.5V, $V_{REF} \leq V_{CC}$, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC2600/LTC2610/LTC2620 MIN	TYP	MAX	UNITS
R_{OUT}	DC Output Impedance	$V_{REF} = V_{CC}$ = 5V, Midscale; –15mA ≤ I_{OUT} ≤ 15mA	●		0.025	0.15	Ω
		$V_{REF} = V_{CC}$ = 2.5V, Midscale; –7.5mA ≤ I_{OUT} ≤ 7.5mA	●		0.030	0.15	Ω
	DC Crosstalk (Note 4)	Due to Full Scale Output Change (Note 5)			10		µV
		Due to Load Current Change			3.5		µV/mA
		Due to Powering Down (per Channel)			–7.3		µV
I_{SC}	Short-Circuit Output Current	V_{CC} = 5.5V, V_{REF} = 5.6V					
		Code: Zero Scale; Forcing Output to V_{CC}	●	15	34	60	mA
		Code: Full Scale; Forcing Output to GND	●	15	34	60	mA
		V_{CC} = 2.5V, V_{REF} = 2.6V					
		Code: Zero Scale; Forcing Output to V_{CC}	●	7.5	18	50	mA
		Code: Full Scale; Forcing Output to GND	●	7.5	24	50	mA
Reference Input							
	Input Voltage Range		●	0		V_{CC}	V
	Resistance	Normal Mode	●	11	16	20	kΩ
	Capacitance				90		pF
I_{REF}	Reference Current, Power Down Mode	All DACs Powered Down	●		0.001	1	µA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5V (Note 3)	●		2.6	4	mA
		V_{CC} = 3V (Note 3)	●		2.0	3.2	mA
		All DACs Powered Down (Note 3) V_{CC} = 5V	●		0.35	1	µA
		All DACs Powered Down (Note 3) V_{CC} = 3V	●		0.10	1	µA
AC Performance							
	Voltage Output Slew Rate				0.80		V/µs
	Capacitive Load Driving				1000		pF
	Glitch Impulse	At Midscale Transition			12		nV • s
	Multiplying Bandwidth				180		kHz
e_n	Output Voltage Noise Density	At f = 1kHz			120		nV/√Hz
		At f = 10kHz			100		nV/√Hz
	Output Voltage Noise	0.1Hz to 10Hz			15		μV_{P-P}
Digital I/O							
V_{IH}	Digital Input High Voltage	V_{CC} = 2.5V to 5.5V	●	2.4			V
		V_{CC} = 2.5V to 3.6V	●	2.0			V
V_{IL}	Digital Input Low Voltage	V_{CC} = 4.5V to 5.5V	●			0.8	V
		V_{CC} = 2.7V to 5.5V	●			0.6	V
		V_{CC} = 2.5V to 5.5V	●			0.5	V
V_{OH}	Digital Output High Voltage	Load Current = –100µA	●	V_{CC} – 0.4			V
V_{OL}	Digital Output Low Voltage	Load Current = +100µA	●			0.4	V
I_{LK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±1	µA
C_{IN}	Digital Input Capacitance	(Note 6)	●			8	pF

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (See Figure 1) (Note 6)

SYMBOL	PARAMETER	CONDITONS		MIN	TYP	MAX	UNITS
V_{CC} = 2.5V to 5.5V							
t_1	SDI Valid to SCK Setup		●	4			ns
t_2	SDI Valid to SCK Hold		●	4			ns
t_3	SCK High Time		●	9			ns
t_4	SCK Low Time		●	9			ns
t_5	$\overline{CS}$/LD Pulse Width		●	10			ns
t_6	LSB SCK High to $\overline{CS}$/LD High		●	7			ns
t_7	$\overline{CS}$/LD Low to SCK High		●	7			ns
t_8	SDO Propagation Delay from SCK Falling Edge	C_{LOAD} = 10pF V_{CC} = 4.5V to 5.5V V_{CC} = 2.5V to 5.5V	 ● ●			 20 45	 ns ns
t_9	CLR Pulse Width		●	20			ns
t_{10}	$\overline{CS}$/LD High to SCK Positive Edge		●	7			ns
	SCK Frequency	50% Duty Cycle	●			50	MHz

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: Linearity and monotonicity are defined from code k_L to code $2^N - 1$, where N is the resolution and k_L is given by $k_L = 0.016(2^N/V_{REF})$, rounded to the nearest whole code. For V_{REF} = 4.096V and N = 16, k_L = 256 and linearity is defined from code 256 to code 65,535.

Note 3: Digital inputs at 0V or V_{CC}.

Note 4: DC crosstalk is measured with V_{CC} = 5V and V_{REF} = 4.096V, with the measured DAC at midscale, unless otherwise noted.

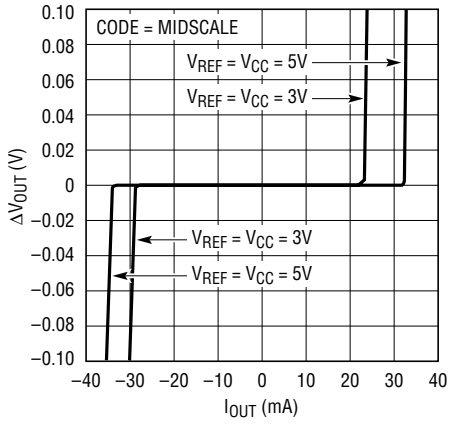
Note 5: R_L = 2kΩ to GND or V_{CC}.

Note 6: Guaranteed by design and not production tested.

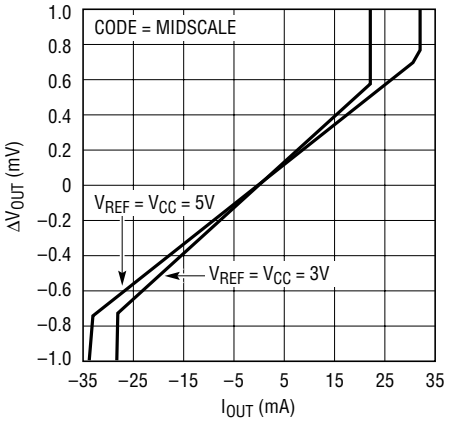
Note 7: Inferred from measurement at code 256 (LTC2600), code 64 (LTC2610) or code 16 (LTC2620).

TYPICAL PERFORMANCE CHARACTERISTICS (LTC2600/LTC2610/LTC2620)

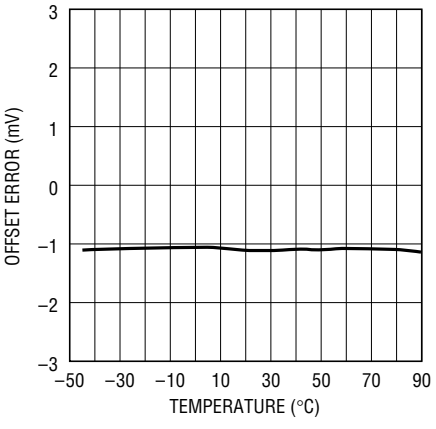
Current Limiting



Load Regulation



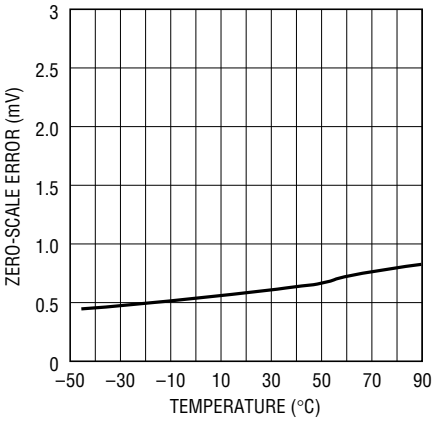
Offset Error vs Temperature



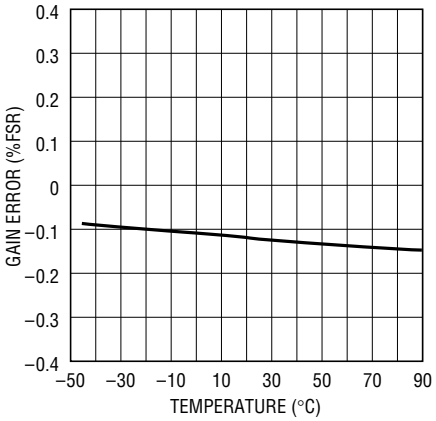
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2600/LTC2610/LTC2620

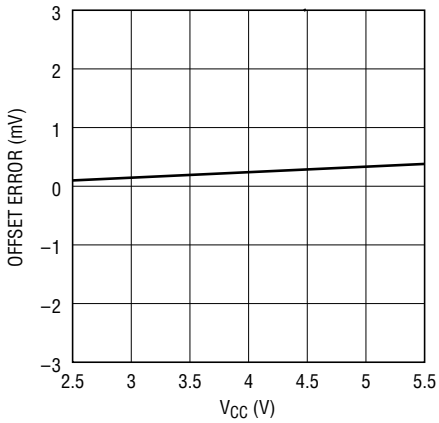
Zero-Scale Error vs Temperature



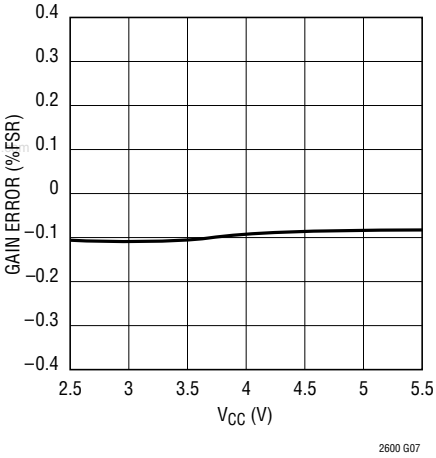
Gain Error vs Temperature



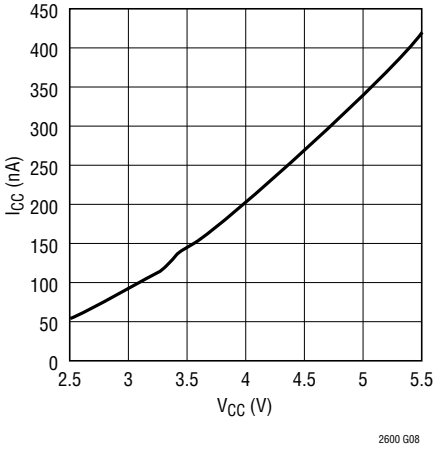
Offset Error vs V_{CC}



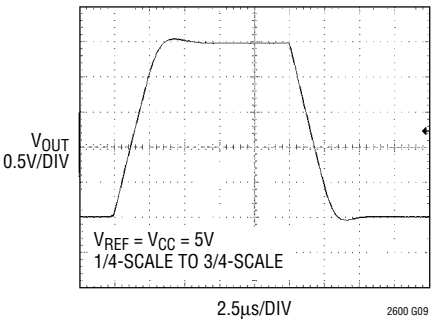
Gain Error vs V_{CC}



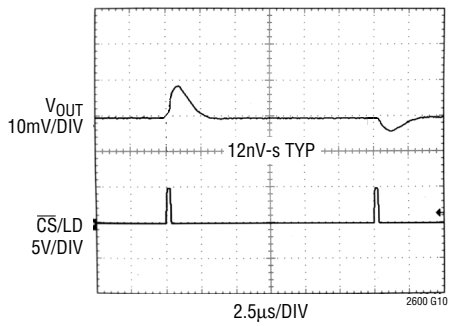
I_{CC} Shutdown vs V_{CC}



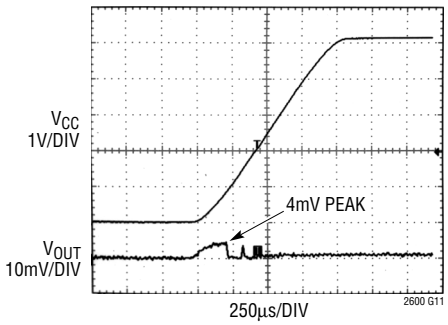
Large-Signal Settling



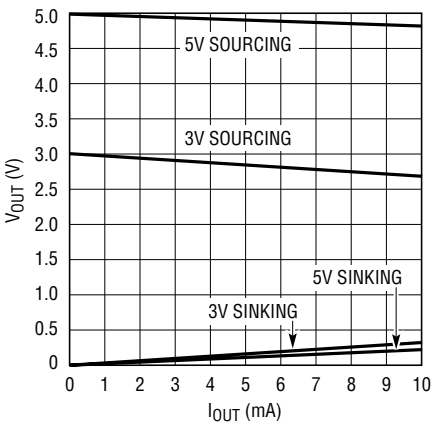
Midscale Glitch Impulse



Power-On Reset Glitch



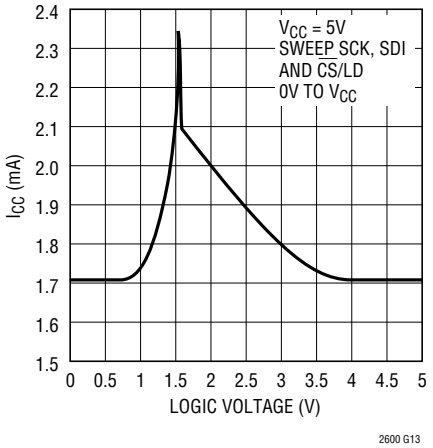
Headroom at Rails vs Output Current



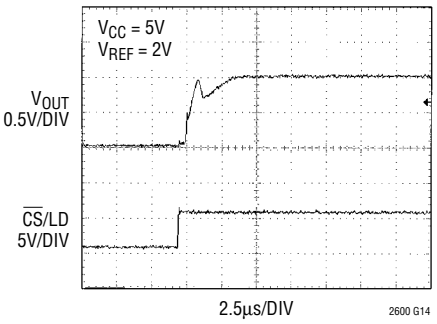
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2600/LTC2610/LTC2620

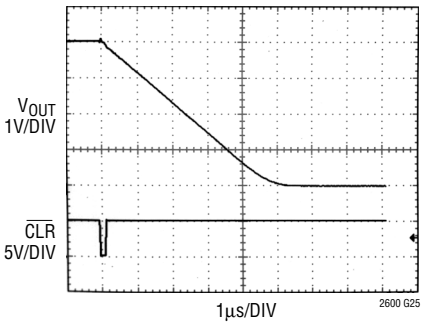
Supply Current vs Logic Voltage



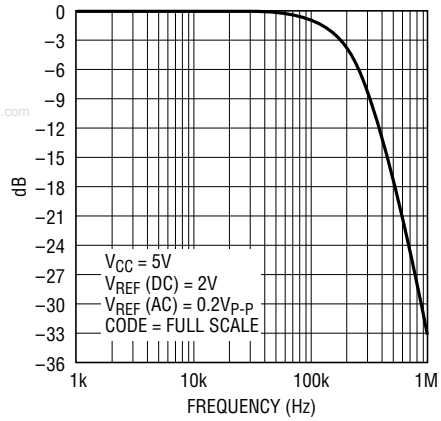
Exiting Power-Down to Midscale



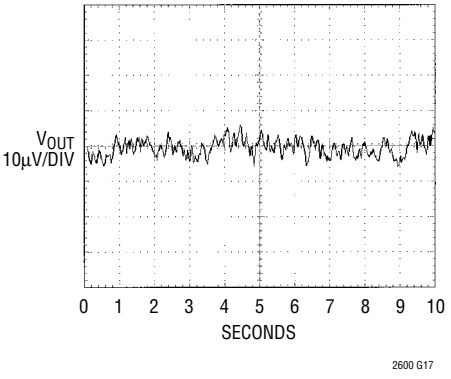
Hardware $\overline{CLR}$



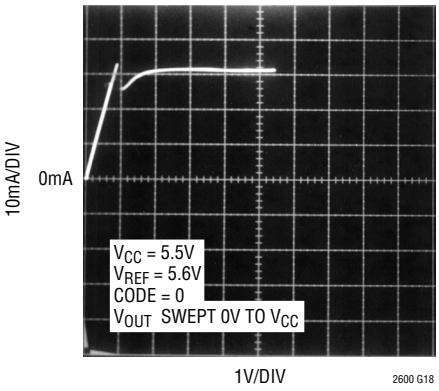
Multiplying Bandwidth



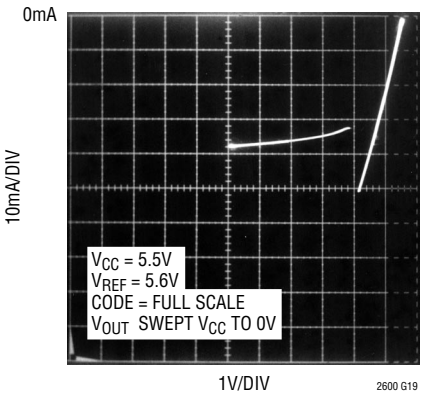
Output Voltage Noise, 0.1Hz to 10Hz



Short-Circuit Output Current vs V_{OUT} (Sinking)



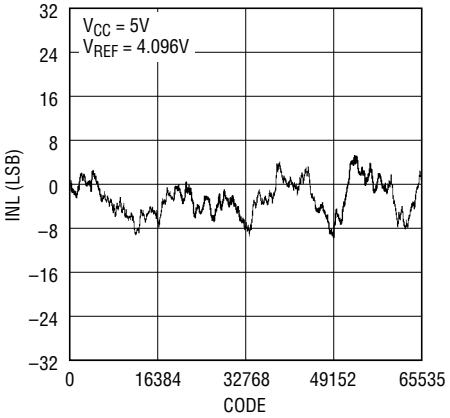
Short-Circuit Output Current vs V_{OUT} (Sourcing)



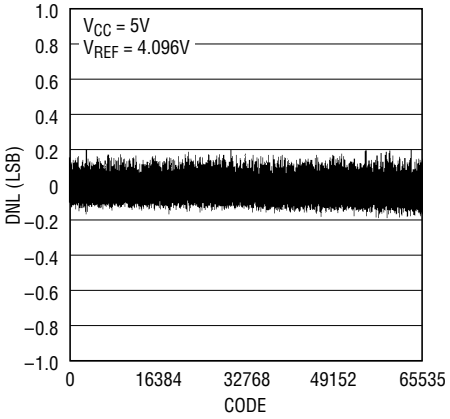
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2600

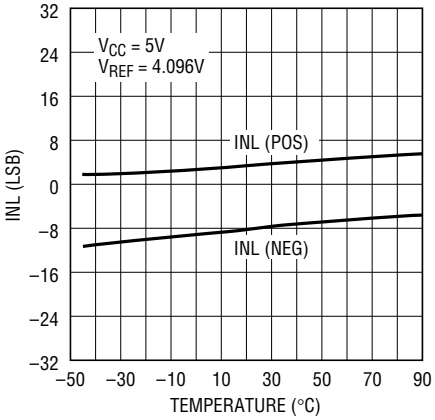
Integral Nonlinearity (INL)



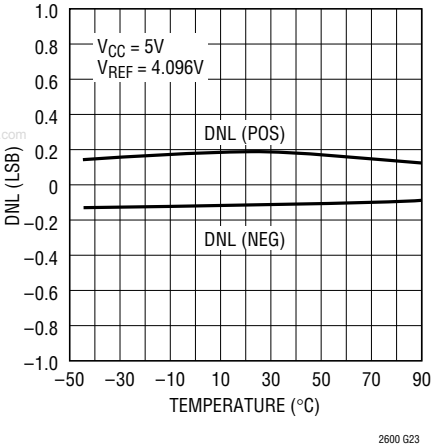
Differential Nonlinearity (DNL)



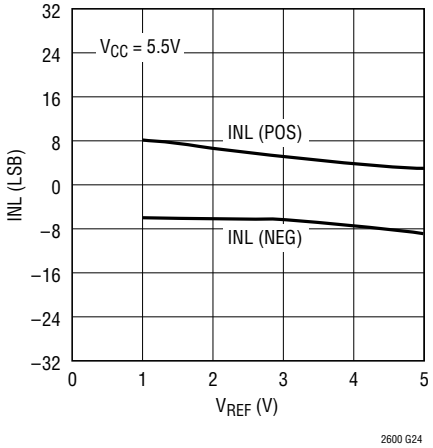
INL vs Temperature



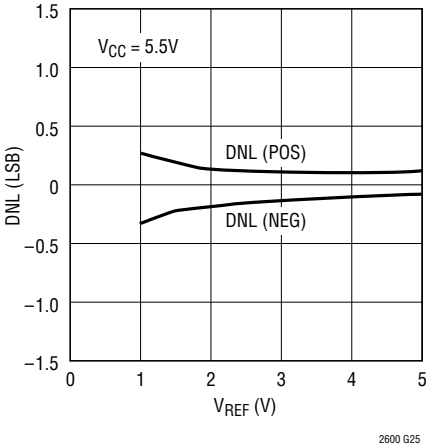
DNL vs Temperature



INL vs V_{REF}

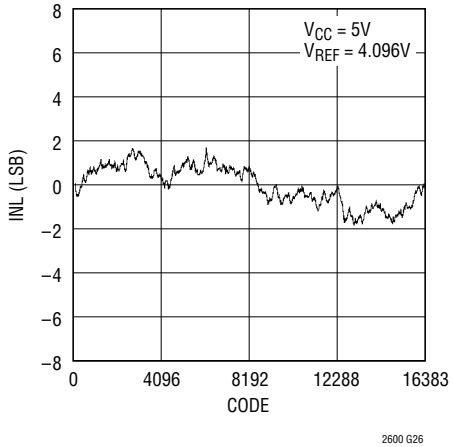


DNL vs V_{REF}

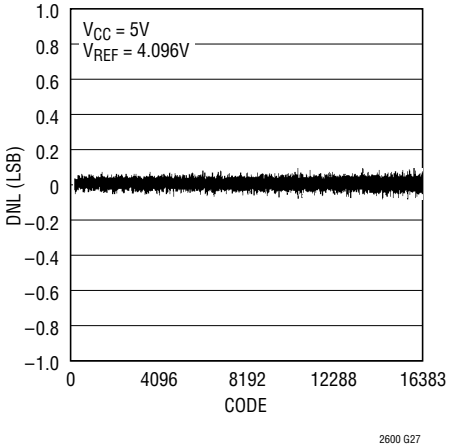


LTC2610

Integral Nonlinearity (INL)



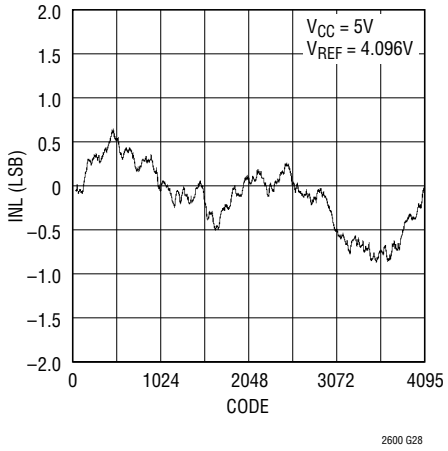
Differential Nonlinearity (DNL)



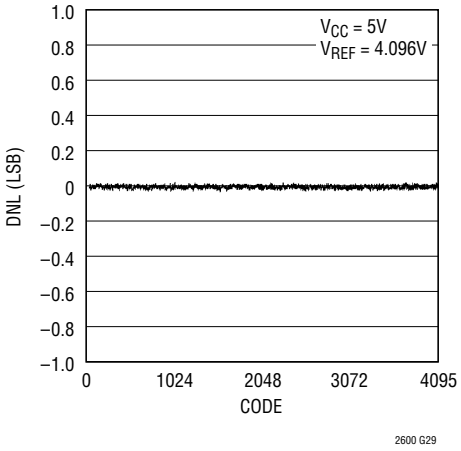
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2620

Integral Nonlinearity (INL)



Differential Nonlinearity (DNL)



PIN FUNCTIONS

GND (Pin 1): Analog Ground.

$V_{OUT\ A}$ to $V_{OUT\ H}$ (Pins 2-5 and 12-15): DAC Analog Voltage Outputs. The output range is 0 – V_{REF}.

REF (Pin 6): Reference Voltage Input. $0V \leq V_{REF} \leq V_{CC}$.

$\overline{CS}$/LD (Pin 7): Serial Interface Chip Select/Load Input. When $\overline{CS}$/LD is low, SCK is enabled for shifting data on SDI into the register. When $\overline{CS}$/LD is taken high, SCK is disabled and the specified command (see Table 1) is executed.

SCK (Pin 8): Serial Interface Clock Input. CMOS and TTL compatible.

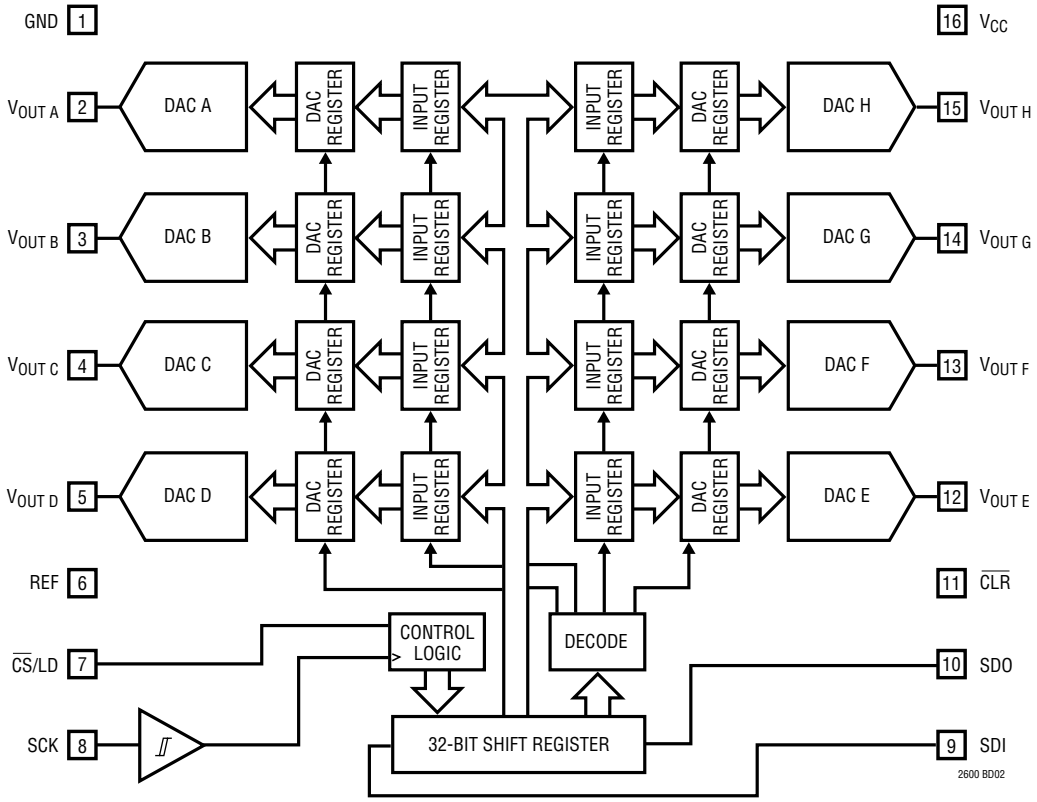
SDI (Pin 9): Serial Interface Data Input. Data is applied to SDI for transfer to the device at the rising edge of SCK. The LTC2600 accepts input word lengths of either 24 or 32 bits.

SDO (Pin 10): Serial Interface Data Output. The serial output of the shift register appears at the SDO pin. The data transferred to the device via the SDI pin is delayed 32 SCK rising edges before being output at the next falling edge. This pin is used for daisy-chain operation.

$\overline{CLR}$ (Pin 11): Asynchronous Clear Input. A logic low at this level-triggered input clears all registers and causes the DAC voltage outputs to drop to 0V. CMOS and TTL compatible.

V_{CC} (Pin 16): Supply Voltage Input. $2.5V \leq V_{CC} \leq 5.5V$.

BLOCK DIAGRAM



TIMING DIAGRAM

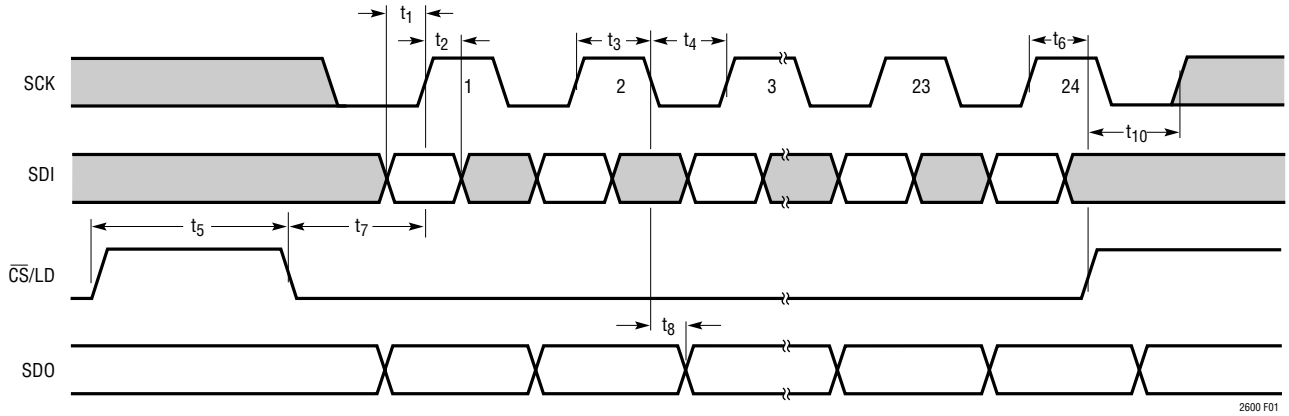


Figure 1

OPERATION

Power-On Reset

The LTC2600/LTC2610/LTC2620 clear the outputs to zero scale when power is first applied, making system initialization consistent and repeatable.

For some applications, downstream circuits are active during DAC power-up, and may be sensitive to nonzero outputs from the DAC during this time. The LTC2600/LTC2610/LTC2620 contain circuitry to reduce the power-on glitch; furthermore, the glitch amplitude can be made arbitrarily small by reducing the ramp rate of the power supply. For example, if the power supply is ramped to 5V in 1ms, the analog outputs rise less than 10mV above ground (typ) during power-on. See Power-On Reset Glitch in the Typical Performance Characteristics section.

Power Supply Sequencing

The voltage at REF (Pin 6) should be kept within the range $-0.3V \le V_{REF} \le V_{CC} + 0.3V$ (see Absolute Maximum Ratings). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at V_{CC} (Pin 16) is in transition.

Transfer Function

The transfer function is

$$V_{OUT(IDEAL)} = \left(\frac{k}{2^N}\right)V_{REF}$$

where k is the decimal equivalent of the binary DAC input code, N is the resolution and V_{REF} is the voltage at REF (Pin 6).

Serial Interface

Referring to Figure 2a: The $\overline{CS}$/LD input is level triggered. When this input is taken low, it acts as a chip-select signal, powering-on the SDI and SCK buffers and enabling the input shift register. Data (SDI input) is transferred at the next 24 rising SCK edges. The 4-bit command word, C3-C0, is loaded first; then the 4-bit DAC address, A3-A0; and finally the 16-bit data word. The data word comprises the 16-, 14- or 12-bit input code, ordered MSB-to-LSB, followed by 0, 2 or 4 don't-care bits (LTC2600, LTC2610 and LTC2620 respectively). Data can only be transferred to the device when the $\overline{CS}$/LD signal is low.The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to carry out the action specified in the 24-bit input word. The complete sequence is shown in Figure 2a; the command (C3-C0) and address (A3-A0) assignments are shown in Table 1.

Optionally, the instruction may be extended to 32 bits. To use the 32-bit word width, 8 don't-care bits are transferred to the device first, followed by the 24-bit input word as just described (see Figure 2b). The 32-bit word width is required for daisy-chain operation, and is also available to accommodate microprocessors which have a minimum word width of 2 bytes.

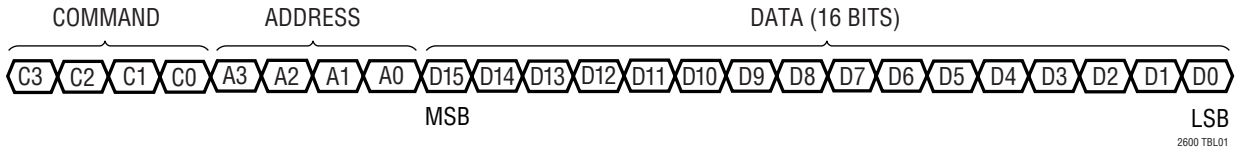
Table 1.

COMMAND				
C3	C2	C1	C0	
0	0	0	0	Write to Input Register n
0	0	0	1	Update (Power-Up) DAC Register n
0	0	1	0	Write to Input Register n, Update (Power Up) All
0	0	1	1	Write to and Update (Power Up) n
0	1	0	0	Power Down n
1	1	1	1	No Operation

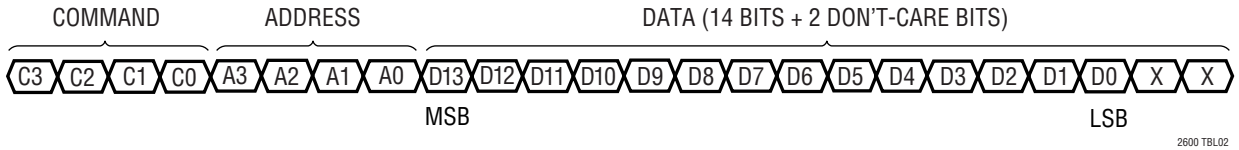
ADDRESS (n)				
A3	A2	A1	A0	
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
0	1	0	0	DAC E
0	1	0	1	DAC F
0	1	1	0	DAC G
0	1	1	1	DAC H
1	1	1	1	All DACs

OPERATION

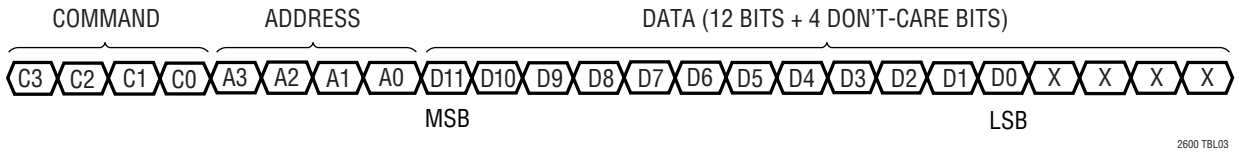
INPUT WORD (LTC2600)



INPUT WORD (LTC2610)



INPUT WORD (LTC2620)



Daisy-Chain Operation

The serial output of the shift register appears at the SDO pin. Data transferred to the device from the SDI input is delayed 32 SCK rising edges before being output at the next SCK falling edge.

The SDO output can be used to facilitate control of multiple serial devices from a single 3-wire serial port (i.e., SCK, SDI and $\overline{CS}$/LD). Such a "daisy chain" series is configured by connecting SDO of each upstream device to SDI of the next device in the chain. The shift registers of the devices are thus connected in series, effectively forming a single input shift register which extends through the entire chain. Because of this, the devices can be addressed and controlled individually by simply concatenating their input words; the first instruction addresses the last device in the chain and so forth. The SCK and $\overline{CS}$/LD signals are common to all devices in the series.

In use, $\overline{CS}$/LD is first taken low. Then the concatenated input data is transferred to the chain, using SDI of the first device as the data input. When the data transfer is complete, $\overline{CS}$/LD is taken high, completing the instruction sequence for all devices simultaneously. A single device can be controlled by using the "no operation" command (1111) for the other devices in the chain.

Power Down Mode

Command 0100_b is reserved for the special "power down" instruction (see Table 1). Any or all DACs may be powered down by selecting the appropriate DAC address (n). In this mode, the digital interface stays active while the analog circuits are disabled. The static power consumption of the digital interface is leakage current only. The reference input and analog outputs are set in a high impedance state, although the DAC feedback resistors are still in place loading the DAC outputs with 90kΩ to ground. As shown in Table 1, any or all of the DACs can be powered back up by executing an update command to the selected DAC which will power up that DAC and update its output with the last loaded DAC word.

Voltage Outputs

Each of the 8 rail-to-rail amplifiers contained in these parts has guaranteed load regulation when sourcing or sinking up to 15mA at 5V (7.5mA at 3V).

Load regulation is a measure of the amplifier's ability to maintain the rated voltage accuracy over a wide range of load conditions. The measured change in output voltage per milliampere of forced load current change is expressed in LSB/mA.

OPERATION

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from LSB/mA to Ohms. The amplifiers' DC output impedance is 0.025Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 25Ω typical channel resistance of the output devices; e.g., when sinking 1mA, the minimum output voltage = 25Ω • 1mA = 25mV. See the graph Headroom at Rails vs Output Current in the Typical Performance Characteristics section.

The amplifiers are stable driving capacitive loads of up to 1000pF.

Board Layout

The excellent load regulation and DC crosstalk performance of these devices is achieved in part by keeping "signal" and "power" grounds separated internally and by reducing shared internal resistance to just 0.005Ω.

The GND pin functions both as the node to which the reference and output voltages are referred and as a return path for power currents in the device. Because of this, careful thought should be given to the grounding scheme and board layout in order to ensure rated performance.

The PC board should have separate areas for the analog and digital sections of the circuit. This keeps digital signals away from sensitive analog signals and facilitates the use of separate digital and analog ground planes which have minimal capacitive and resistive interaction with each other.

Digital and analog ground planes should be joined at only one point, establishing a system star ground as close to the device's ground pin as possible. Ideally, the analog ground plane should be located on the component side of the board, and should be allowed to run under the part to shield it from noise. Analog ground should be a continuous and uninterrupted plane, except for necessary lead pads and vias, with signal traces on another layer.

OPERATION

The GND pin of the part should be connected to analog ground. Resistance from the GND pin to system star ground should be as low as possible. Resistance here will add directly to the effective DC output impedance of the device (typically 0.025Ω), and will degrade DC crosstalk. Note that the LTC2600/LTC2610/LTC2620 are no more susceptible to these effects than other parts of their type; on the contrary, they allow layout-based performance improvements to shine rather than limiting attainable performance with excessive internal resistance.

Rail-to-Rail Output Considerations

In any rail-to-rail voltage output device, the output is limited to voltages within the supply range.

Since the analog outputs of the device cannot go below ground, they may limit for the lowest codes as shown in Figure 3b. Similarly, limiting can occur near full scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 3c. No full-scale limiting can occur if V_{REF} is less than V_{CC} – FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

OPERATION

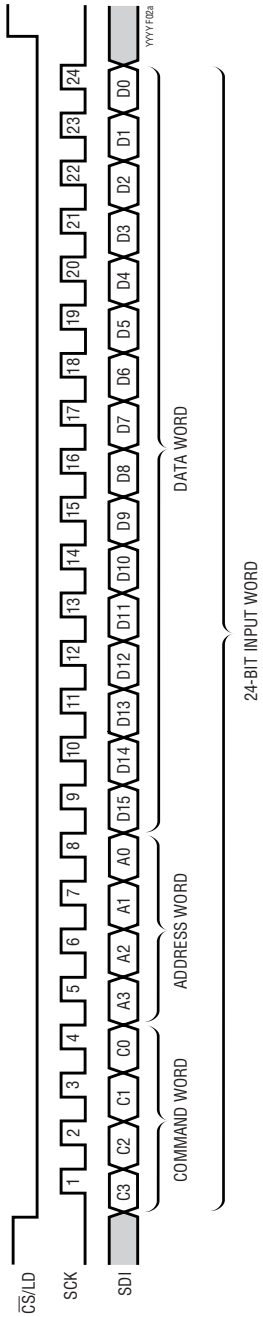


Figure 2a. LTC2600 24-Bit Load Sequence (Minimum Input Word). LTC2610 SDI Data Word: 14-Bit Input Code + 2 Don't-Care Bits; LTC2620 SDI Data Word: 12-Bit Input Code + 4 Don't-Care Bits

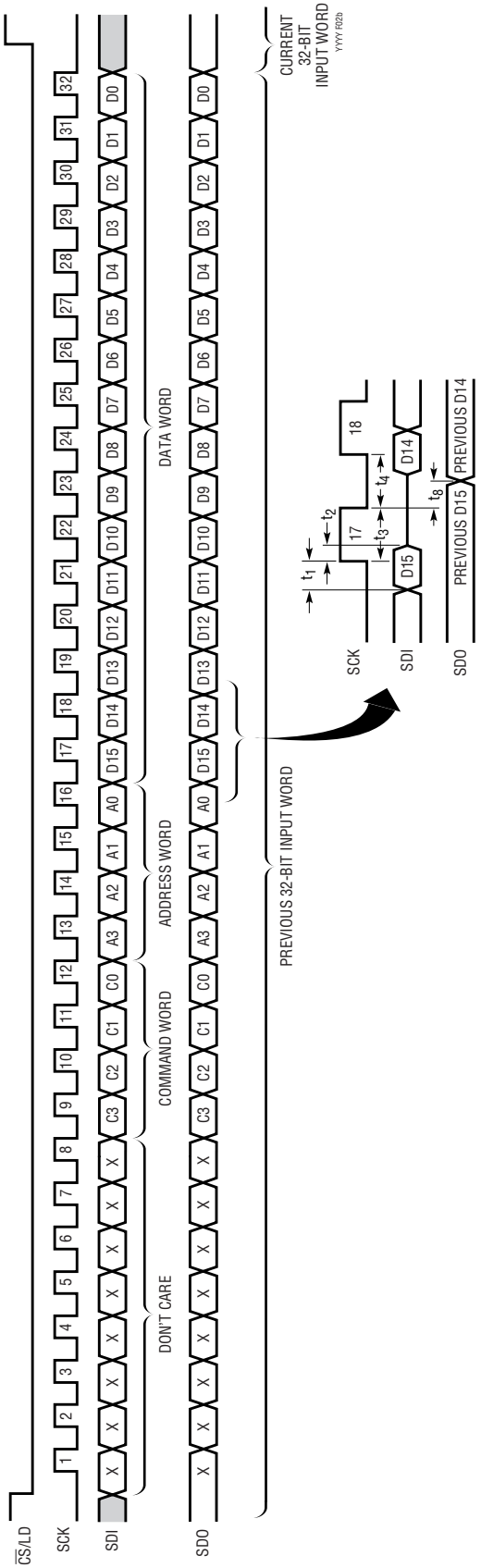


Figure 2b. LTC2600 32-Bit Load Sequence (Required for Daisy-Chain Operation). LTC2610 SDI/SDO Data Word: 14-Bit Input Code + 2 Don't-Care Bits; LTC2620 SDI/SDO Data Word: 12-Bit Input Code + 4 Don't-Care Bits

OPERATION

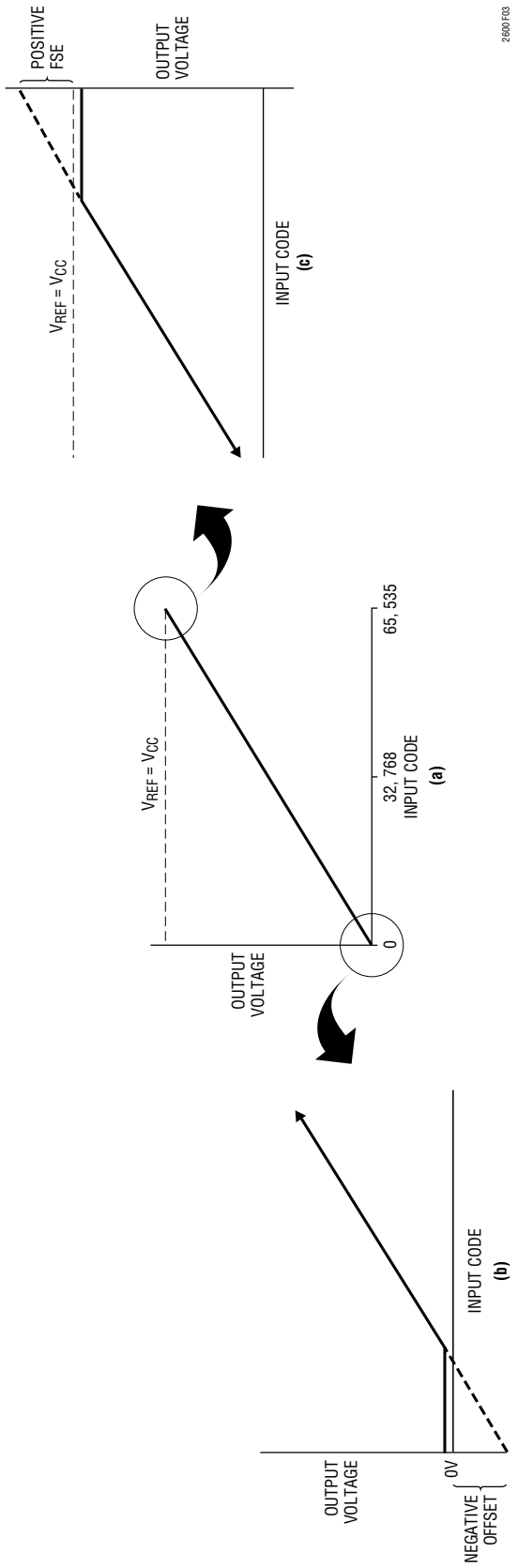
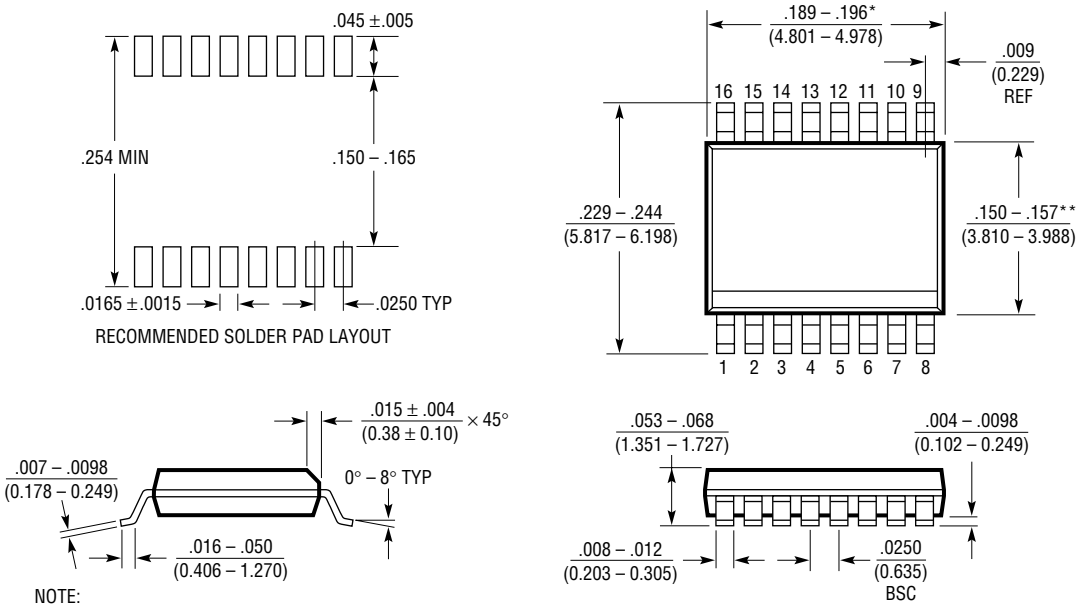


Figure 3. Effects of Rail-to-Rail Operation On a DAC Transfer Curve. (a) Overall Transfer Function (b) Effect of Negative Offset for Codes Near Zero Scale (c) Effect of Positive Full-Scale Error for Codes Near Full Scale

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0502

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1458/LTC1458L	Quad 12-Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.096V LTC1458L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1654	Dual 14-Bit Rail-to-Rail V_{OUT} DAC	Programmable Speed/Power, 3.5µs/750µA, 8µs/450µA
LTC1655/LTC1655L	Single 16-Bit V_{OUT} DAC with Serial Interface in SO-8	V_{CC} = 5V(3V), Low Power, Deglitched
LTC1657/LTC1657L	Parrallel 5V/3V 16-Bit V_{OUT} DAC	Low Power, Deglitched, Rail-to-Rail V_{OUT}
LTC1660/LTC1665	Octal 10/8-Bit V_{OUT} DAC in 16-Pin Narrow SSOP	V_{CC} = 2.7V to 5.5V, Micropower, Rail-to-Rail Output
LTC1821	Parallel 16-Bit Voltage Output DAC	Precision 16-Bit Settling in 2µs for 10V Step

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