PRELIMINARY

Integrated Circuit Systems, Inc.

ICS83940-02

LOW SKEW, 1-TO-18 LVCMOS FANOUT BUFFER

GENERAL DESCRIPTION

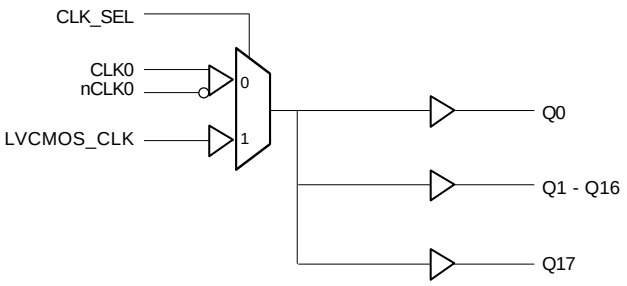
The ICS83940-02 is a low skew, 1-to-18 Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 18 to 36 by utilizing the ability of the outputs to drive two series terminated lines. The differential clock input is designed to accept any differential input levels including LVPECL.

The ICS83940-02 is characterized at full 3.3V, full 2.5V and mixed 3.3V input and 2.5V output operating supply modes. Guaranteed output and part-to-part skew characteristics make the ICS83940 ideal for those clock distribution applications demanding well defined performance and repeatability.

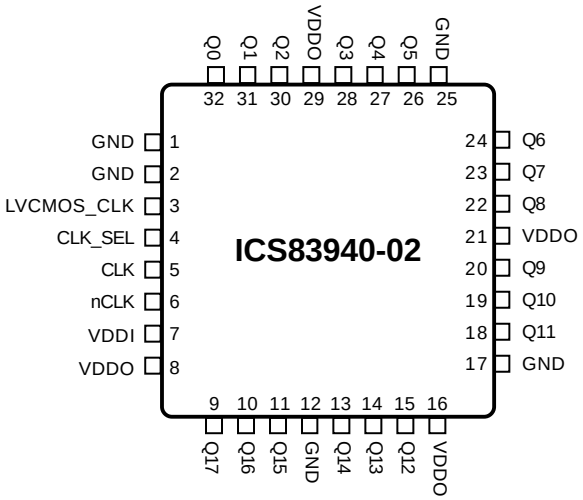
FEATURES

- 18 LVCMOS outputs, 7Ω typical output impedance
- Output frequency up to 200MHz
- 150ps output skew
- Part to part skew: TBD
- Selectable LVCMOS or differential clock input
- LVTTL / LVCMOS clock select input
- Full 3.3V, 2.5V or mixed 3.3V, 2.5V supply modes
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
Y Pacakge
7mm x 7mm x 1.4mm package body
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2, 12, 17, 25	GND	Power		Output power supply ground. Connect to ground.
3	LVCMOS_CLK	Input	Pulldown	Clock input. LVCMOS interface levels.
4	CLK_SEL	Input	Pulldown	Clock select input. Select LVCMOS clock input when HIGH. Selects LVPECL clock inputs when LOW.
5	CLK	Input	Pulldown	Non-inverting differential clock input. Any differential inteface levels.
6	nCLK	Input	Pullup	Inverting differential clock input. Any differential inteface levels.
7	VDDI	Power		Input power supply. Connect to 3.3V or 2.5V.
8, 16, 21, 29	VDDO	Power		Output power supply. Connect to 3.3V or 2.5V.
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q17, Q16, Q15, Q14, Q13, Q12, Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Clock outputs. 7Ω typical output impedance. LVCMOS interface levels

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance	CLK0, nCLK0, LVCMOS_CLK				4	pF
		CLK_SEL				4	pF
CPD	Power Dissipation Capacitance (per output)		VDDI, VDDO = 3.465V				pF
			VDDI = 3.465V, VDDO = 2.625V				pF
			VDDI, VDDO = 2.625V				pF
RPULLUP	Input Pullup Resistor				51		KΩ
RPULLDOWN	Input Pulldown Resistor				51		KΩ
ROUT	Output Impedance				7		Ω

TABLE 3A. CLOCK SELECT FUNCTION TABLE

Control Input	Clock	
CLK_SEL	**CLK0, nCLK0**	**LVCMOS_CLK**
0	Selected	De-selected
1	De-selected	Selected

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs				Outputs	Input to Output Mode	Polarity
CLK-SEL	LVCMOS_CLK	CLK0	nCLK0	Q0 thru Q17		
0	—	0	1	LOW	Differential to Single Ended	Non Inverting
0	—	1	0	HIGH	Differential to Single Ended	Non Inverting
0	—	0	Biased; NOTE 1	LOW	Single Ended to Single Ended	Non Inverting
0	—	1	Biased; NOTE 1	HIGH	Single Ended to Single Ended	Non Inverting
0	—	Biased; NOTE 1	0	HIGH	Single Ended to Single Ended	Inverting
0	—	Biased; NOTE 1	1	LOW	Single Ended to Single Ended	Inverting
1	0	—	—	LOW	Single Ended to Single Ended	Non Inverting
1	1	—	—	HIGH	Single Ended to Single Ended	Non Inverting

NOTE 1: Single ended input use requires that one of the differential inputs be biased. The voltage at the biased input sets the switch point for the single ended input. For LVCMOS input levels the recommended input bias network is a resistor to VDDI, a resistor of equal value to ground and a 0.1µF capacitor from the input to ground. The resulting switch point is VDDI/2.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, VDD	4.6V
Inputs, V_I	-0.5V to VDD+0.5 V
Outputs, V_O	-0.5V to VDD+0.5V
Package Thermal Impedance, θ_{JA}	46°C/W (0lfpm)
Storage Temperature, Tstg	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. DC CHARACTERISTICS, VDDI = VDDO = 3.3V±5%, T_A = 0° TO 70°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage		3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage		3.135	3.3	3.465	V
IDD	Power Supply Current	VDDI = VDDO = 3.465V			70	mA

TABLE 4B. LVCMOS DC CHARACTERISTICS, VDDI = VDDO = 3.3V±5%, T_A = 0° TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	REF_CLK	VDDI = 3.465V	2		3.8	V
		CLK_SEL					
VIL	Input Low Voltage	REF_CLK	VDDI = 3.135V	-0.3		1.3	V
		CLK_SEL	VDDI = 3.135V	-0.3		0.8	V
IIH	Input High Current	REF_CLK, CLK_SEL	VDDI = VIN = 3.465V			150	µA
IIL	Input Low Current	REF_CLK, CLK_SEL	VDDI = 3.465V, VIN = 0V	-5			µA
VOH	Output High Voltage		VDDO = 3.135V, IOH = -36mA	2.4			V
VOL	Output Low Voltage		VDDO = 3.135V, IOL = 36mA			0.6	V

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, VDDI = VDDO = 3.3V±5%, T_A = 0° TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	CLK0	VDDI = VIN = 3.465V			150	µA
		nCLK0	VDDI = VIN = 3.465V			5	µA
IIL	Input Low Current	CLK0	VDDI = 3.465V, VIN = 0V	-5			µA
		nCLK0	VDDI = 3.465V, VIN = 0V	-150			µA
VPP	Peak-to-Peak Input Voltage			0.15		1.3	V
VCMR	Input Common Mode Voltage; NOTE 1, 2			GND + 0.5		VDD - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK0, nCLK0 is VDD + 0.3V.
NOTE 2: Common mode voltage is defined as VIH.

TABLE 5A. AC CHARACTERISTICS, VDDI = VDDO = 3.3V±5%, T_A = 0° TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency					200	MHz
tpLH	Propagation Delay; NOTE 1	CLK, nCLK	0 < f ≤ 200MHz	2.3		4	ns
tpHL	Propagation Delay; NOTE 1	CLK, nCLK	0 < f ≤ 200MHz				ns
tsk(o)	Output Skew; NOTE 2, 4		Measured on rising edge @VDDO/2			150	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4		Measured on rising edge @VDDO/2			TBD	ps
tR	Output Rise Time		20% to 80% @ 50MHz				ns
tF	Output Fall Time		20% to 80% @ 50MHz				ns
odc	Output Duty Cycle			45	50	55	%

All parameters measured at fMAX unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at VDDO/2.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages, with equal load conditions, and using the same type of inputs.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4D. POWER SUPPLY DC CHARACTERISTICS, VDDI = 3.3V±5%; VDDO = 2.5V±5%, T_A = 0° TO 70°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage		3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage		2.375	2.5	2.625	V
IDD	Power Supply Current	VDDI = 3.465V, VDDO = 2.625V				mA

TABLE 4E. LVCMOS DC CHARACTERISTICS, VDDI = 3.3V±5%; VDDO = 2.5V±5%, T_A = 0° TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	REF_CLK	VDDI = 3.465V	2		3.8	V
		CLK_SEL					
VIL	Input Low Voltage	REF_CLK	VDDI = 3.135V	-0.3		1.3	V
		CLK_SEL					
IIH	Input High Current	REF_CLK, CLK_SEL	VDDI = VIN = 3.465V			150	µA
IIL	Input Low Current	REF_CLK, CLK_SEL	VDDI = 3.465V, VIN = 0V	-5			µA
VOH	Output High Voltage		VDDO = 2.375V, IOH = -12mA	1.8			V
VOL	Output Low Voltage		VDDO = 2.375V, IOL = 12mA			0.5	V

TABLE 4F. DIFFERENTIAL DC CHARACTERISTICS, VDDI = 3.3V±5%; VDDO = 2.5V±5%, T_A = 0° TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	CLK0	VDDI = VIN = 3.465V			150	µA
		nCLK0	VDDI = VIN = 3.465V			5	µA
IIL	Input Low Current	CLK0	VDDI = 3.465V, VIN = 0V	-5			µA
		nCLK0	VDDI = 3.465V, VIN = 0V	-150			µA
VPP	Peak-to-Peak Input Voltage			0.15		1.3	V
VCMR	Input Common Mode Voltage; NOTE 1, 2			GND + 0.5		VDD - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK0, nCLK0 is VDD + 0.3V.
NOTE 2: Common mode voltage is defined as VIH.

TABLE 5B. AC CHARACTERISTICS, VDDI = 3.3V±5%, VDDO = 2.5V±5%, T_A = 0° TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency						MHz
tpLH	Propagation Delay; NOTE 1	CLK, nCLK	0 < f ≤ 200MHz				ns
tpHL	Propagation Delay; NOTE 1	CLK, nCLK	0 < f ≤ 200MHz				ns
tsk(o)	Output Skew; NOTE 2, 4		Measured on rising edge @VDDO/2				ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4		Measured on rising edge @VDDO/2				ps
tR	Output Rise Time		20% to 80% @ 50MHz				ns
tF	Output Fall Time		20% to 80% @ 50MHz				ns
odc	Output Duty Cycle						%

All parameters measured at fMAX unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at VDDO/2.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages, with equal load conditions, and using the same type of inputs.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4G. POWER SUPPLY DC CHARACTERISTICS, VDDI = VDDO = 2.5V±5%, T_A = 0° TO 70°

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage		2.375	2.5	2.625	V
VDDO	Output Power Supply Voltage		2.375	2.5	2.625	V
IDD	Power Supply Current	VDDI = VDDO = 2.625V				mA

TABLE 4H. LVCMOS DC CHARACTERISTICS, VDDI = VDDO = 2.5V±5%, T_A = 0° TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	REF_CLK	VDDI = 2.625V	2		2.96	V
		CLK_SEL					
VIL	Input Low Voltage	REF_CLK	VDDI = 2.375V			0.8	V
		CLK_SEL					
IIH	Input High Current	REF_CLK, CLK_SEL	VDDI = VIN = 2.625V			150	µA
IIL	Input Low Current	REF_CLK, CLK_SEL	VDDI = 2.625V, VIN = 0V	-5			µA
VOH	Output High Voltage		VDDO = 2.375V, IOH = -12mA	1.8			V
VOL	Output Low Voltage		VDDO = 2.375V, IOL = 12mA			0.5	V

TABLE 4I. DIFFERENTIAL DC CHARACTERISTICS, VDDI = VDDO = 25V±5%, T_A = 0° TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	CLK0	VDDI = VIN = 2.625V			150	µA
		nCLK0	VDDI = VIN = 2.375V			5	µA
IIL	Input Low Current	CLK0	VDDI = 2.625V, VIN = 0V	-5			µA
		nCLK0	VDDI = 2.625V, VIN = 0V	-150			µA
VPP	Peak-to-Peak Input Voltage			0.15		1.3	V
VCMR	Input Common Mode Voltage; NOTE 1, 2			GND + 0.5		VDD - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK0, nCLK0 is VDD + 0.3V.
NOTE 2: Common mode voltage is defined as VIH.

TABLE 5C. AC CHARACTERISTICS, VDDI = VDDO = 2.5V±5%, T_A = 0° TO 70°

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency						MHz
tpLH	Propagation Delay; NOTE 1	CLK, nCLK	0 < f ≤ 200MHz				ns
tpHL	Propagation Delay; NOTE 1	CLK, nCLK	0 < f ≤ 200MHz				ns
tsk(o)	Output Skew; NOTE 2, 4		Measured on rising edge @VDDO/2				ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4		Measured on rising edge @VDDO/2				ps
tR	Output Rise Time		20% to 80% @ 50MHz				ns
tF	Output Fall Time		20% to 80% @ 50MHz				ns
odc	Output Duty Cycle						%

All parameters measured at fMAX unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at VDDO/2.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages, with equal load conditions, and using the same type of inputs.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

PACKAGE OUTLINE - Y SUFFIX

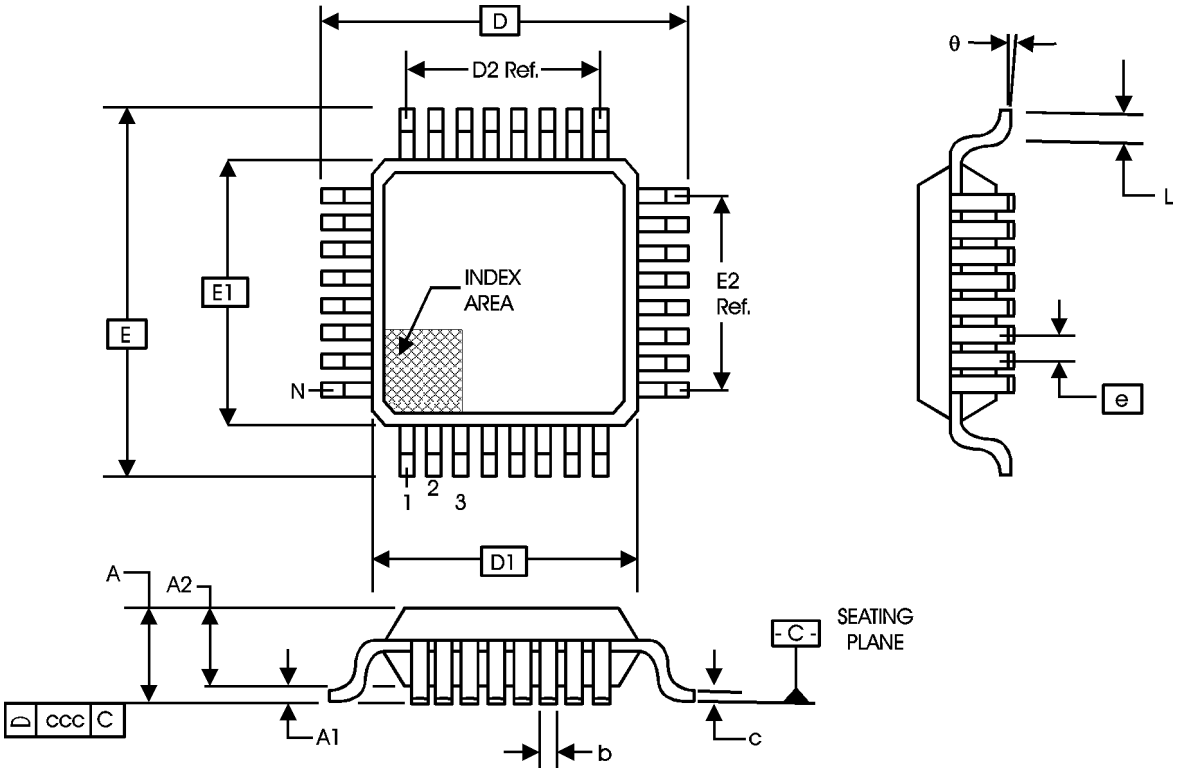


TABLE 6. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

REFERENCE DOCUMENT: JEDEC PUBLICATION 95, MS-026

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS83940AY-02	ICS83940AY-02	32 Lead LQFP	250 per tray	0°C to 70°C
ICS83940AY-02T	ICS83940AY-02	32 Lead LQFP on Tape and Reel	1000	0°C to 70°C