AN1339
APPLICATION NOTE

32-bit Applications Using the M7010, M7020 Network Search Engines

INTRODUCTION

The M7010 and M7020 Search Engines are ideal for Layer 2 and Layer 3 applications requiring word widths from 68 bits to 272 bits. The device was designed optimally for handling the varying widths greater than 64 bits. However, 32-bit addresses are often required in ATM as well as IP addresses. For these 32-bit applications, the results can be achieved in two cycles, and this method ensures that the Search Engine is fully used.

WRITE OPERATIONS USING THE GLOBAL MASK REGISTER

The M7010 and M7020 Search Engines are organized as 68-bit widths. Data is written in the devices by using the Global Mask Register. Setting a “1” in the Global Mask Register allows data to be written into the M7010 and M7020. Setting a “0” in the Global Mask Register does not modify the data. As 34 bits of data are available, one has to write information in the left half and then into the right half of the 68-bit word.

The first step is to write to two of the eight Global Mask Registers with the patterns shown below:

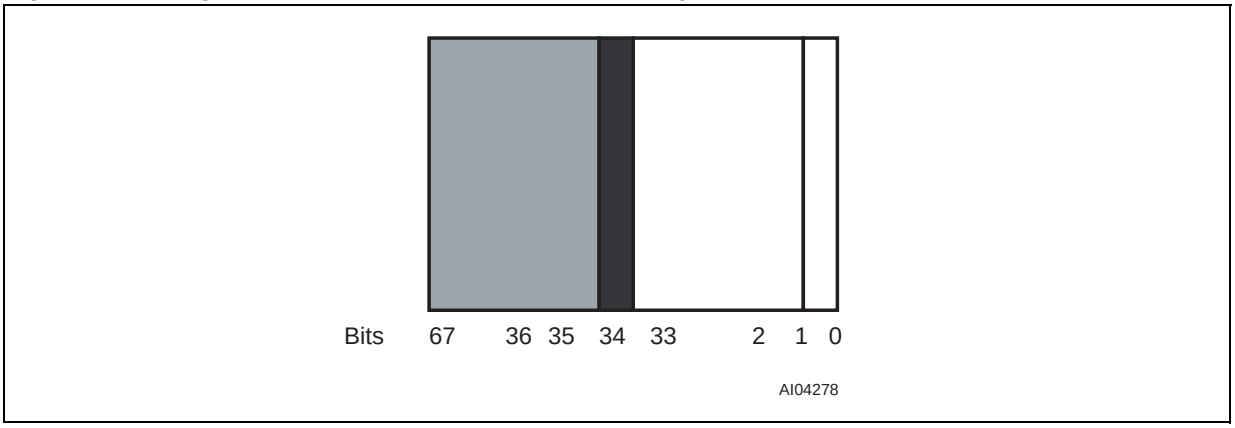
Table 1. Patterns Required in the Global Mask Register

Global Mask Register 0	1 1 1	...1	0 0 0	...0
Global Mask Register 1	0 0 0	...0	1 1 1	...1
Bits:	67	34	33	0

After writing to two of the eight Global 0 Mask Registers, data is loaded in the device by performing a Write operation using Global Mask Register 1 until the left half of the data array is completely full. This operation stores the left half of the 68-bit data word or 34 bits in the Data array.

Bits 67-36 are shown in one section representing a 32-bit word and bits 35 & 34 are shown separately (see Figure 1). For instance bits 67-36 can represent IP addresses. Bits 35 and 34 can be user-defined. In this application 34-bit operations occur in each half section of the Data array and Mask array of the Search Engine.

Figure 1. Storing the left half of the Data or Mask Array



It is recommended that the user define bit 34 to be a valid bit. The M7010 and M7020 are very flexible devices and if another bit position was defined as a valid bit it is also acceptable, and essentially the user has all 34 bits at his disposal. After the left half is completely full, then the right half has to be written. This is done by using Global Mask Register 1 and performing write operations. In this operation the right half of the 68-bit word is stored in the right-most 34 bits of the Data array.

Not all locations have to be written, as the array can be partially full on the right or even the left side.

After this a search operation can proceed. The search operations are performed twice, once on the left half and then on the right half in that order. Note that a “1” in the Global Mask register enables a compare during a search operation and a “0” forces a match condition regardless of the state of the data bit. The search throughput for 34-bit operations is half of that of 68-bit operations. The search is performed by using the Global Mask Register 0 for the left half of the 68-bit word, and after that another search is performed using Global Mask Register 1 for the right half of the 68-bit word. The order is important, as the left half has a higher priority than the right half. For example, if a search on the left half may produce a match and a search on the right half also produces a match, then in that case, the left half has the higher priority. If only one unique match exists in a particular system, then a match on the left side may alleviate the need to do a search on the right half of the Data array.

CASCADING M7010, M7020 SEARCH ENGINES AND 32-BIT OPERATIONS

When depths greater than 32K are desired, the 32-bit operations can be performed in cascaded mode as well. The data has to be written in an ordered manner where the entire left section has to be written across boundaries and then right half section. Table 2 shows the required sequence for writing into the device.

Table 2. Entry Order for Cascaded, 32-bit Operations

CAM 0 LEFT	CAM 0 RIGHT
WRITE FIRST	WRITE THIRD

CAM 1 LEFT	CAM 1 RIGHT
WRITE SECOND	WRITE FOURTH

After the Data arrays have been written using the global mask register, they are ready for searches that are performed using two cycles as explained earlier in this document.

CONCLUSION

The M7010 and M7020 are configurable Search Engines. Although they were optimized for 68-bit, 136-bit, and 272-bit operations, they can efficiently handle 32-bit look-ups as well.

CONTACT INFORMATION

If you have any questions or suggestions concerning the matters raised in this document, please send them to the following electronic mail addresses:

apps.nvram@st.com	(for application support)
ask.memory@st.com	(for general inquiries)

Please remember to include your name, company, location, telephone number, and fax number.