AN1227
APPLICATION NOTE

IMPROVED RF MOSFET RELIABILITY THROUGH PACKAGING ENHANCEMENTS

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1. ABSTRACT

It is well known that temperature is a critical operating state parameter for today's electronic industry. Temperature influences device operating state characteristics and performance. As well, it is a crucial variable in estimating electronic devices' lifetime. Most failure mechanisms of semiconductor devices are accelerated at higher operating temperatures. An antiquated rule of thumb suggests that for every 10ºC rise in temperature, the failure rate doubles. Also, limiting device temperatures can be the key to meeting performance criteria. Higher operating temperatures usually degrade device performance, for example, by reducing gain and efficiency and increasing leakage currents.

2. MOSFET PACKAGING.

Device packaging is the interface between the heat generating semiconductor substrate, and the ambient used to dissipate heat generation during device operation. The device package's thermal properties are therefore essential, and require thermal design considerations to ensure that the device operates at safe operating junction temperatures. Many providers of high power RF discrete devices include derating curves to extrapolate device performance at elevated temperatures in order to compensate for the anticipated operating environment. Steady-state and transient thermal analysis is often performed empirically and analytically to optimize thermal transfer characteristics. Most device manufacturers provide a thermal resistance rating. The following paper discusses two common package styles: differences in their thermal characteristics and the implications thereof.

The P package, which contains a pedestal that supports beryllium oxide (BeO), has been in the mainstay of the industry for many years, while the NP package has been in limited use for bipolar junction transistors (BJT). The NP package will be used for the STMicroelectronics RF power MOSFETs. The justification for this decision will be axiomatic from the following discussion. Figures 1 and 2 depict the geometry and materials of the P and NP package. The P package consists of an Oxygen-Free-High-Conductivity (OHFC) Copper (Cu) flange with a pedestal upon which a disk of BeO ceramic is attached and the semiconductor die is eutecticly mounted to the BeO. The size of the pedestal is limited by the mechanical mismatch stress which can cause the ceramic to crack during assembly or during use over a temperature range.

The pedestal has a diameter of 275 mils, while the BeO has a diameter of 480 mils. The NP package consists of a Cu flange with a Molybdenum (Mo) base insert, to compensate for the mechanical stresses on the BeO. The BeO is attached to the Cu flange and the semiconductor die is eutecticly mounted to the BeO. The die size is 128 mils x 211 mils. The die properties are not modeled exactly in this analysis since we are only interested in comparing the packages for an approximate die size, and it is assumed that the die-BeO interface is constant for both package styles. The only intrinsic material property needed for steady-state thermal analysis is the thermal conductivities of the constituent materials. The thermal conductivity values used for the OHFC Cu, BeO and Mo are 10.1 W/in-ºC, 6.5 W/in-ºC and 3.4 W/in-ºC

respectively. In general, the material properties are a function of temperature and their functional dependence, although not specified here, were included in the nonlinear thermal analysis. In order to compare the thermal dissipation effectiveness of these packages a Finite-Element Analysis (FEA) was performed to solve the steady-state temperature distribution under a given device power dissipation using an evaluation copy of ANSYS/Multiphysics software. Since the die is rectangular, two axes of symmetry were used to perform two separate, two dimensional thermal FEAs. Using these axes of symmetry a three dimensional problem was reduced to a two dimensional problem. The worst case results from the longest die dimension, and thus potentially the highest thermal resistance, are presented in this application note. Some assumptions about the constraints that force the thermal solution include an infinitely thin heat source at the surface of the BeO and a fixed temperature at the bottom of the flange. hus, the boundary conditions required to solve Poisson's equation describing steady-state temperature distribution are: 1) a fixed flange temperature at the boundary of the heat sink (entire bottom); 2) the heat flux from the die which due to the power dissipation was fixed at the same value for the thermal analysis of both packages. This value was based on nominal device power output and efficiency. The remainder of the undefined boundaries were given the Neumann (adiabatic) condition. Thus the assumptions include: 1) the heat source is located at the top surface; 2) cooling is exclusively through the bottom surface; 3) the active area is rectangular and located at the center of the top surface; 4) the power distribution is uniform over the active area of the device.

Figure 1: P Package Style

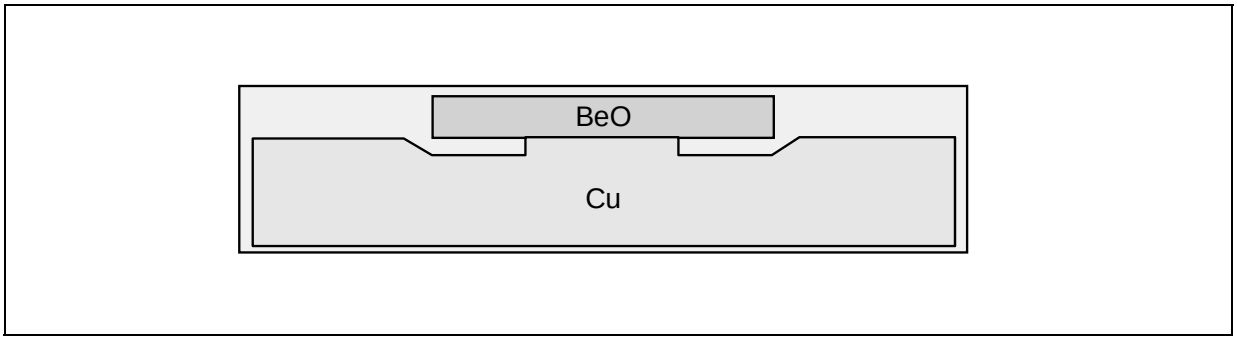
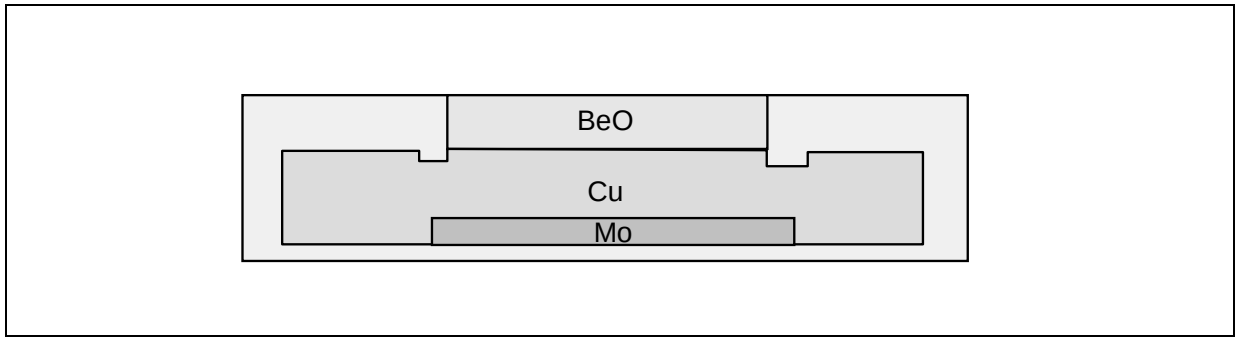


Figure 2: NP Package Style



The results of the thermal FEA in the form of temperature distribution contour maps are shown in figures 3 and 4 for each of the package styles. The temperature contour maps show that the temperature gradient is large near the concentrated heat source, and the temperature gradient is diminishing in the lower regions near the heat sink as expected. However, there are several interesting features that suggest one package has a thermal advantage over the other. The most salient feature is that the NP package style has a 10ºC lower peak temperature than the P package under the conditions of this analysis. It can also be seen that the BeO of the P package has a larger temperature throughout its

volume as compared to the NP package. The edge of the BeO on the P package is in the range of 60-75ºC while the edge of the BeO on the NP package is in the range of 20-35ºC. The isotherm that includes the edge of the BeO in the P package is constricted by the pedestal and not allowed to spread the heat as would naturally occur without the pedestal, and thus the higher temperature. This suggests that the conductive thermal dissipation through the BeO to the flange is more effective in the NP package than the P package. Another interesting feature of the results is that the edge of the flange does not appear to have any significant heating due to the device's power dissipation. Thus modifying the flange would not result in any thermal improvement.

Figure 3: P Package Temperature Map

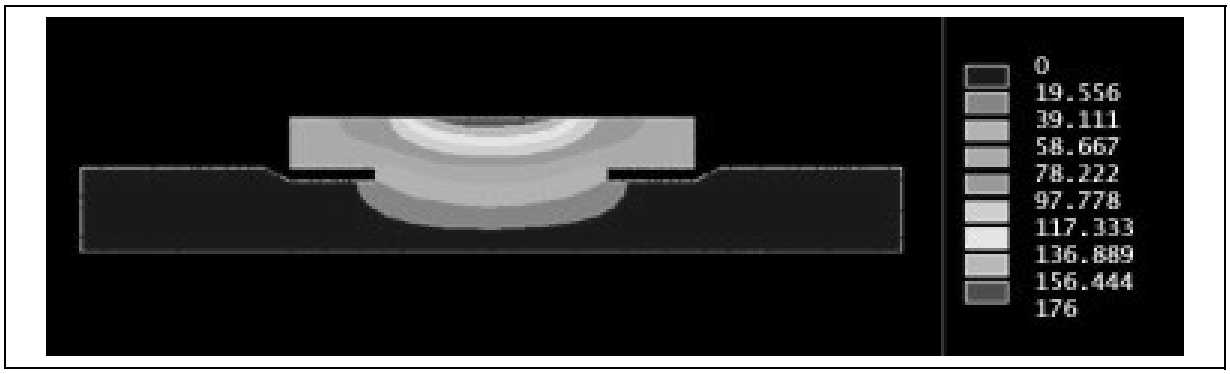
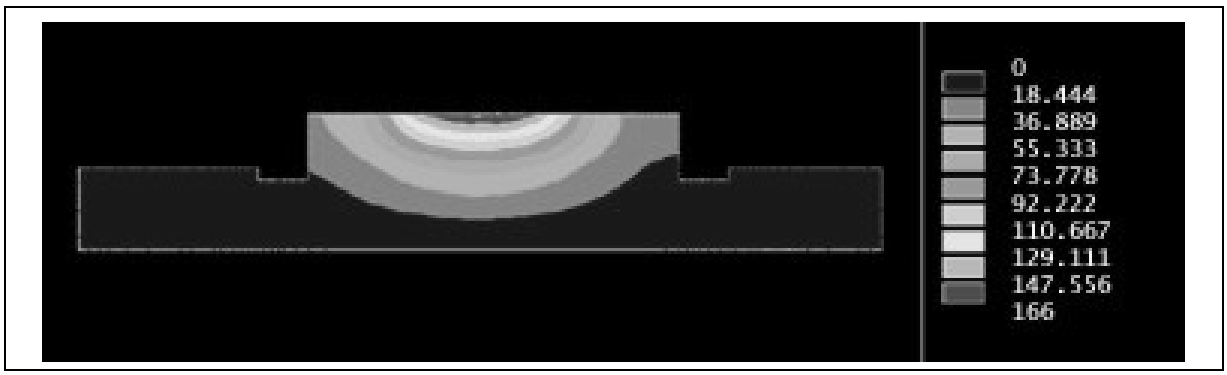


Figure 4: NP Package Temperature Map



The SD2921 and SD2921-10 are large VHF 150W DMOS Power FETS that were used to verify the improvements projected by the thermal modeling. Both devices use the same die and overall mechanical dimensioning but represent the thermal path differences discussed above. The SD2921 uses the conventional pedestal package with a resultant thermal resistance of 0.6 ºC/Watt; the SD2921-10 uses the NP package for a 25% improvement in thermal resistance (0.45 ºC/Watt). Both of these values were determined by InfraRed Imaging and the resultant reduction in junction temperature was actually better than the model projections which were not silicon die specific. With a typical dissipation of 110 Watts and a case temperature of 25 ºC the following junction temperatures and Mean Time to Failure (MTTF) lifetimes can be compared using a metal migration lifetime curve (MTTF for refractory barriered gold metallization) at a drain current I_d=5A for these devices (Table 1):

The temperature reduction results in about a 400% life improvement. Even better improvements can be realized at elevated case temperatures where the fall-off of device performance characteristics with increased junction temperature begin to compound and accentuate the differences in thermal properties.

3. CONCLUSION

In summary, all large devices where the silicon die size approaches or exceeds the conventional pedestal size would benefit in increased lifetime and reduced temperature/parameter effects from the use of the NP package structure. Since MOSFET die sizes are larger than BJT equivalents (for the same power output level), the NP structure would be more appropriate for RF high power MOSFETS.