10BIT 30MSPS ADC ADC1230X

GENERAL DESCRIPTION

The ADC1230X is a CMOS 10-bit low-voltage and high-speed A/D converter (ADC) for video and other applications. It has a four-step pipelined architecture, which consists of sample & hold amplifier, multiplying D/A converters (DACs), and subranging flash ADCs.
The maximum conversion rate of ADC1230 is 30MSPS and supply voltage is 2.5V single.

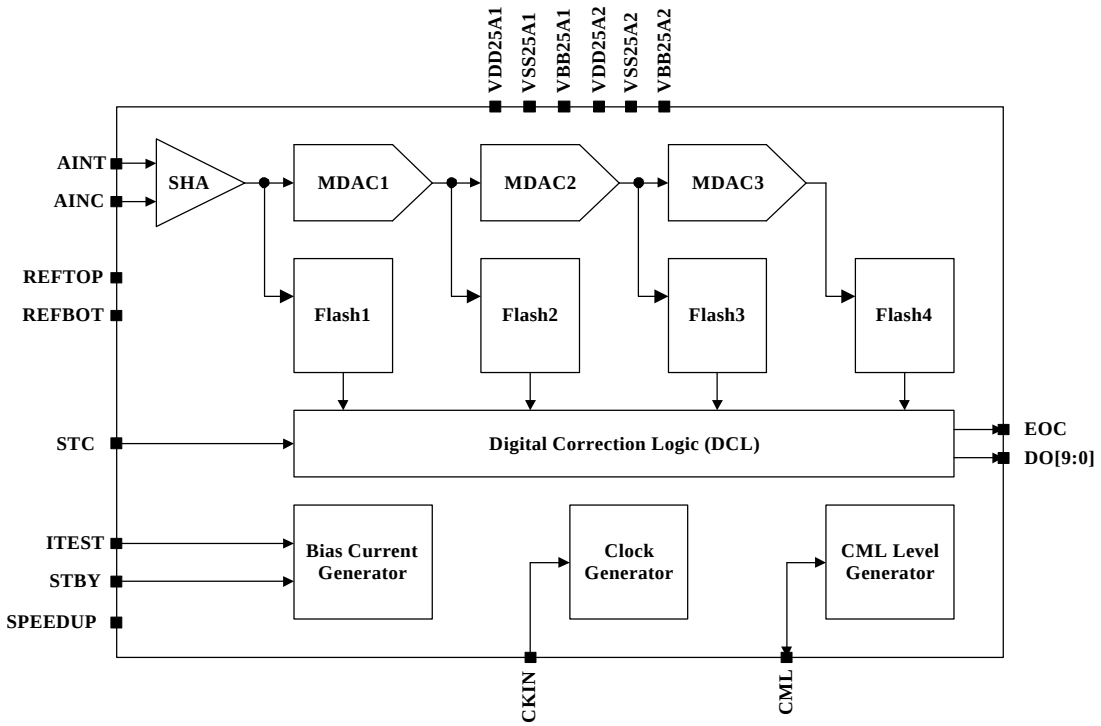
FEATURES

- **Resolution : 10Bit**
- **Differential Linearity Error : ±1.0 LSB**
- **Integral Linearity Error : ±2.0 LSB**
- **Maximum Conversion Rate : 30MSPS**
- **Sample & Hold Function Implemented**
- **Low Power Consumption : 62.5mW(Typ)**
- **Power Supply : 2.5V Single**
- **Operation Temperature Range : 0~70° C**

TYPICAL APPLICATIONS

- CCD imaging processors
  Camcorders, scanners, and security cameras.
- Read channel LSI
  HDD, DVD, and CD-ROM drives
- IF and baseband signal digitizers

FUNCTIONAL BLOCK DIAGRAM



Ver 1.2 (Apr. 2000)

CORE PIN DESCRIPTION

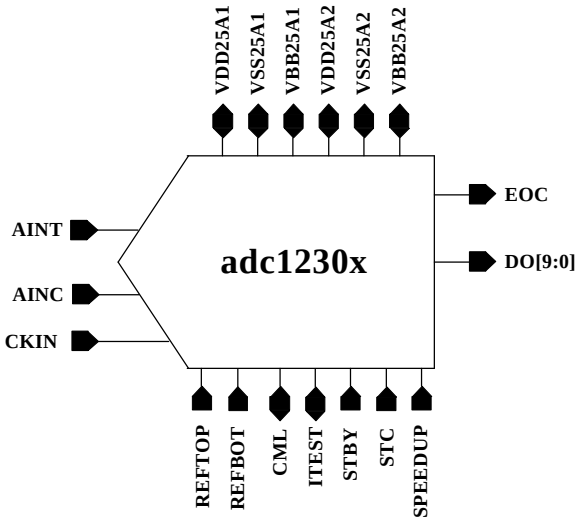
NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
AINT	AI	piar50_abb	AAnalog Input + (Input Range : 0.7V ~ 1.9V)
AINC	AI	piar50_abb	Analog Input : (DC=1.3V)
REFTOP	AI	pia_abb	Reference Top (1.6V)
REFBOT	AI	pia_abb	Reference Bottom(1.0V)
VDD25A1	AP	vdd1t_abb	Analog Power (2.5V)
VSS25A1	AG	vss1t_abb	Analog Ground
VBB25A1	AG	vbb_abb	Analog Sub Bias
ITEST	AB	pia_abb	Open=use internal bias point
STBY	DI	picc_abb	High=power saving standby mode (normally, gnd)
STC	DI	picc_abb	Start of conversion signal (normally, high)
SPEEDUP	DI	picc_abb	Speed test pin (normally, gnd)
CKIN	DI	picc_abb	Sampling Clock Input
CML	AB	pia_abb	Internal Bias Point(Test Pin)
DO[9:0]	DO	poa_abb	Digital Output
EOC	DO	poa_abb	End of conversion signal
VBB25A2	DG	vbb_abb	Digital Sub Bias
VSS25A2	DG	vdd1t_abb	Digital Ground
VDD25A2	DP	vss1t_abb	Digital Power

I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Digital Output
- AB : Analog Bidirectional
- DB : Digital Bidirectional

- AP : Analog Power
- DP : Digital Power
- AG : Analog Ground
- DG : Digital Ground

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	VDD	3.3	V
Analog Input Voltage	AIN	VSS to VDD	V
Digital Input Voltage	CLK	VSS to VDD	V
Digital Output Voltage	V_{OH}, V_{OL}	VSS to VDD	V
Storage Temperature Range	Tstg	-45 to 125	°C

NOTES

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5KΩ resistor (Human body model)

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD25A1 - VSS25A1 VDD25A2 - VSS25A2	2.3	2.5	2.7	V
Supply Voltage Difference	VDD25A1 - VDD25A2	-0.1	0.0	0.1	V
Reference Input Voltage(Externally)	REFTOP REFBOT	- -	1.6 1.0	- -	V
Analog Input Voltage (+)	AINT	0.7	-	1.9	V
Analog Input Voltage (-)	AINC		1.3		V
Operating Temperature	Topr	0	-	70	°C

NOTES

1. It is strongly recommended that all the supply pins (VDD25A1, VDD25A2) be powered from the same source to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Resolution	-	-	10	-	Bits	
Reference Current	IREF	-	2	3	mA	
Differential Linearity Error	DLE	-	-	±1.0	LSB	AINT : 0.7V~1.9V (Ramp Input)
Integral Linearity Error	ILE	-	-	±2.0	LSB	fc : 1MHz
Bottom Offset Voltage Error	EOB	-	-	20	LSB	
Top Offset Voltage Error	EOT	-	-	20	LSB	

NOTES
1. Converter Specifications (unless otherwise specified)
   VDD25A1=2.5V VDD25A2=2.5V
   VSS25A1=GND VSS25A2=GND
   Ta=25° C
2. TBD : To Be Determined

AC ELECTRICAL CHARACTERISTICS

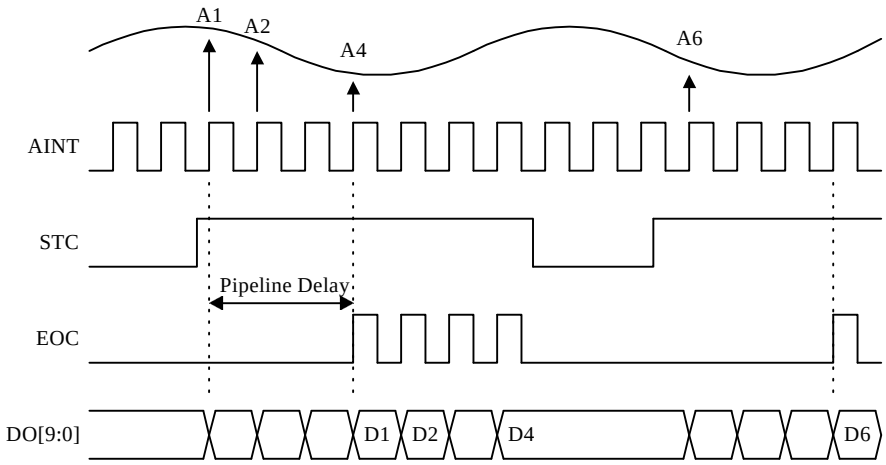
Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Maximum Conversion Rate	fc	-	-	30	MSPS	
Dynamic Supply Current	Ivdd	-	25	30	mA	fc=30MHz (without system load)
Signal - to - Noise Ratio	SNR	48	52	-	dB	AINT = 1MHz fc = 30MHz

I/O CHART

Index	AINT Input (V)	AINC Input (V)	Digital Output	
0	0.7000 ~ 0.7012	1.3	0000000000	
1	0.7012 ~ 0.7023	1.3	0000000001	
2	0.7023 ~ 0.7035	1.3	0000000010	
•••	•••		•••	
511	1.2988 ~ 1.3000	1.3	0111111111	1LSB=1.172mV
512	1.3000 ~ 1.3012	1.3	1000000000	REFTOP=1.6V
513	1.3012 ~ 1.3023	1.3	1000000001	REFBOT=1.0V
•••	•••		•••	
1021	1.8965 ~ 1.8977	1.3	1111111101	
1022	1.8977 ~ 1.8988	1.3	1111111110	
1023	1.8988 ~ 1.9000	1.3	1111111111	

TIMING DIAGRAM

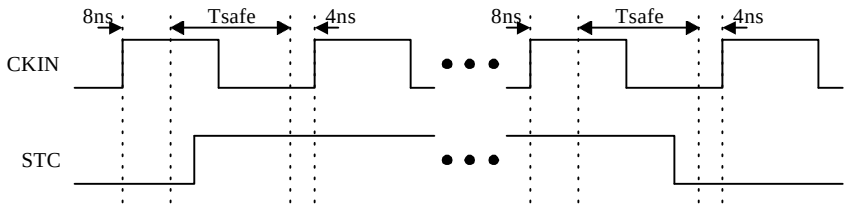
1. Main Waveform



Output code of DO[9:0] is generated during STC (Start of Conversion) signal is just "HIGH". Otherwise, it keeps the current states.

After STC goes "HIGH", the A/D converter requires the pipeline delay of 3 clock period to generate EOC signal and DO[9:0].

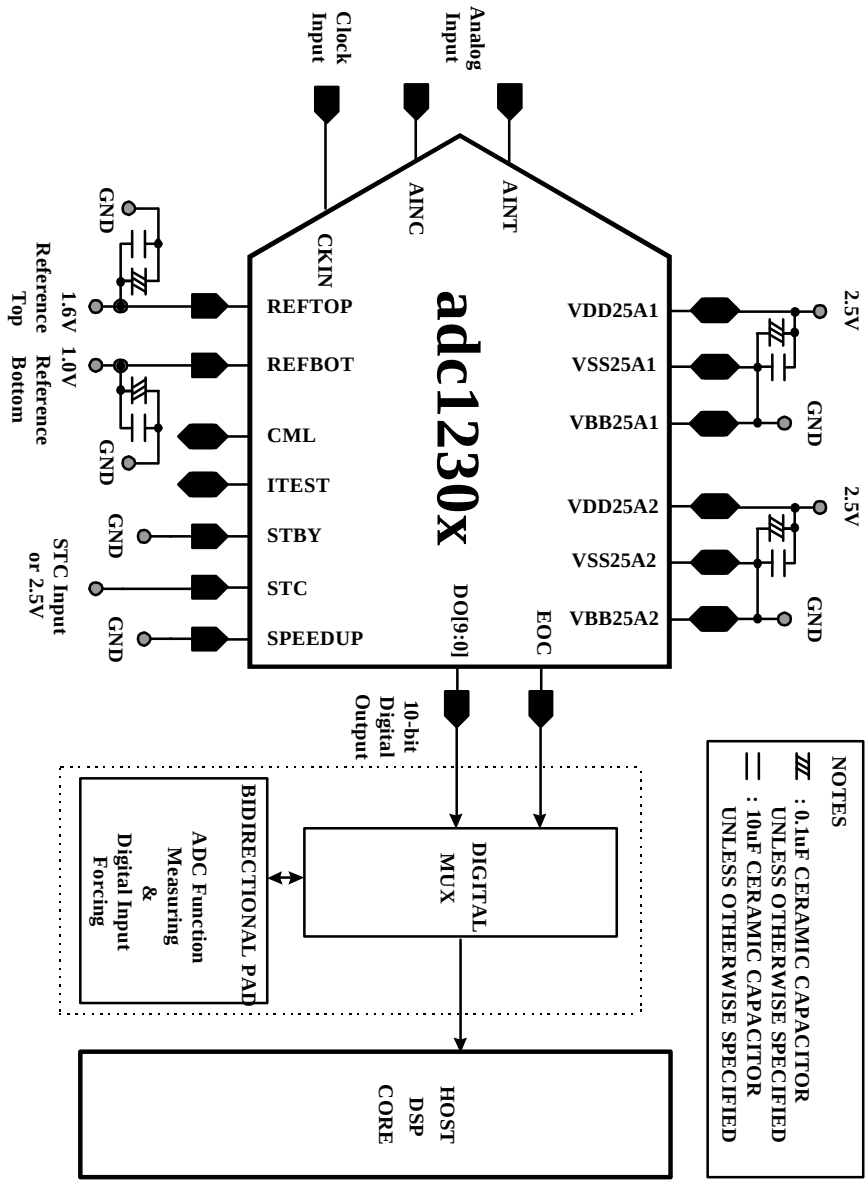
2. STC and CKIN



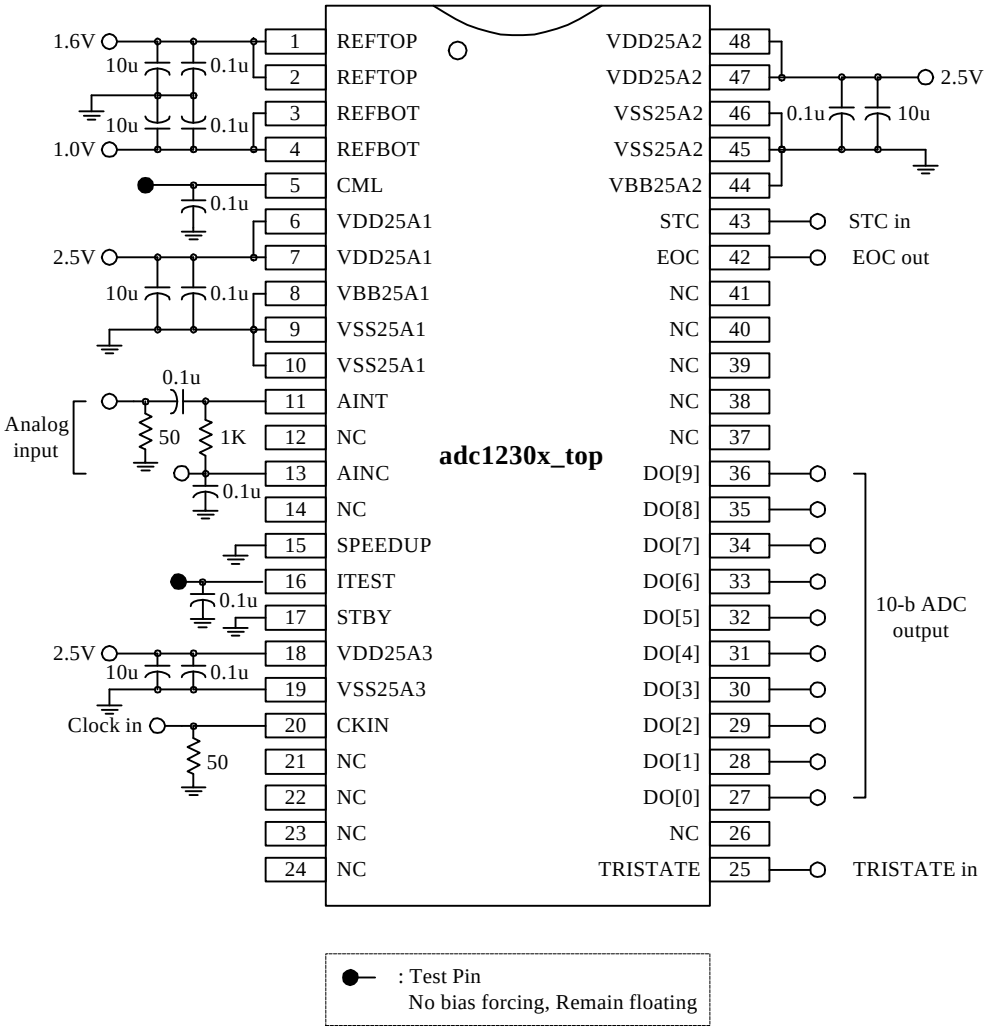
The STC signal is rising-edge triggered, and it should be changed during "Tsafe" region on CKIN .

CORE EVALUATION GUIDE

1. ADC function is evaluated by external check on the bidirectional pads connected to input nodes of HOST DSP back-end circuit.
2. The reference voltages may be biased internally through resistor divider.



PACKAGE CONFIGURATION



NOTES

1. This information is for testing the provided test-chips of ADC1230X.

PACKAGE PIN DESCRIPTION

NAME	PIN NO.	I/O TYPE	PIN DESCRIPTION
REFTOP	1,2	AI	External Reference Top Bias (1.6V)
REFBOT	3,4	AI	External Reference Bottom Bias (1.0V)
CML	5	AB	Internal Bias Point (Test Pin)
VDD25A1	6,7	AP	2.5V Analog Power
VBB25A1	8	AG	Analog Sub Bias
VSS25A1	9,10	AG	Analog Ground
AINT	11	AI	Analog Input (+) Input Range : 0.7~1.9V
AINC	13	AI	Analog Input. (-) DC 1.3V
SPEEDUP	15	DI	Speed test pin. Tie to gnd (VSSA)
ITEST	16	AB	open=use internal bias point
STBY	17	DI	High = power saving standby mode (normally gnd)
VDD25A3	18	PP	Ouput Driver Power (2.5V)
VSS25A3	19	PG	Output Driver Ground
CKIN	20	DI	Sampling Clock Input
TRISTATE	25	DI	high = high impedance digital output (normally gnd)
DO[9:0]	27~36	DO	10bit Digitized Output
EOC	42	DO	End of conversion signal
STC	43	DI	Start of conversion signal
VBB25A2	44	DG	Digital Substrate Bias
VSS25A2	45,46	DG	Digital Ground
VDD25A2	47,48	DP	Digital Power (2.5V)

NOTES

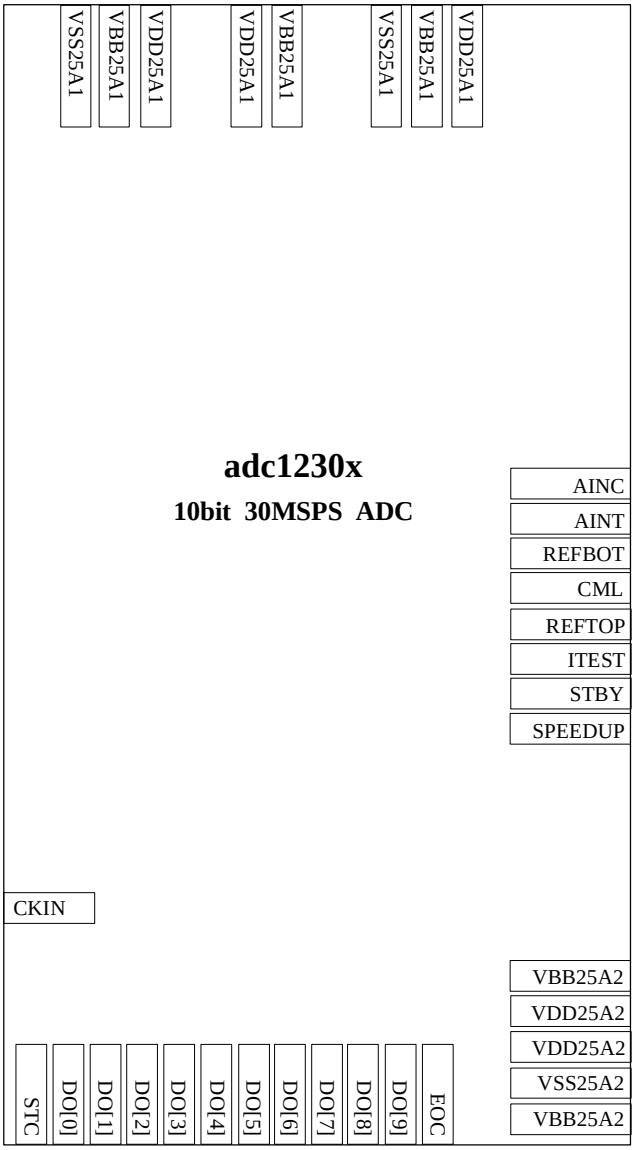
1. This information is for testing the provided test-chips of ADC1230X.
2.. I/O TYPE PP and PG denote PAD Power and PAD Ground respectively.

USER GUIDE

1. Input Range
   - If you want to using the single-ended input, you should use he input range as below.
     AINT : 0.7V ~ 1.9V
     AINC : 1.3V
   - If you want to using the differential input, you should use the input range as below.
     AINT : 1.0V ~ 1.6V
     AINC : 1.6V ~ 1.0V

PHANTOM CELL INFORMATION

- Pins of the core can be assigned externally (Package pins) or internally (internal ports) depending on design methods.
  The term "External" implies that the pins should be assigned externally like power pins.
  The term "External/internal" implies that the applications of these pins depend on the user.



Pin Name	Pin Usage	Pin Layout Guide
VDD25A1	External	- Maintain the large width of lines as far as the pads. - place the port positions to minimize the length of power lines. - Do not merge the analog powers with anoter power from other blocks. - Use good power and ground source on board.
VSS25A1	External	
VBB25A1	External	
VDD25A2	External	
VSS25A2	External	
VBB25A2	External	
AINT	External/Internal	- Do not overlap with digtal lines. - Maintain the shotest path to pads.
AINC	External/Internal	
CKIN	External/Internal	- Separate from all other analog signals
REFTOP	External/Internal	- Maintain the larger width and the shorter length as far as the pads. - Separate from all other digital lines.
REFBOT	External/Internal	
CML	External/Internal	
ITEST	External/Internal	
STBY	External/Internal	
STC	External/Internal	
SPEEDUP	External/Internal	
EOC	External/Internal	- Separated from the analog clean signals if possible. - Do not exceed the length by 1,000um.
DO[9]	External/Internal	
DO[8]	External/Internal	
DO[7]	External/Internal	
DO[6]	External/Internal	
DO[5]	External/Internal	
DO[4]	External/Internal	
DO[3]	External/Internal	
DO[2]	External/Internal	
DO[1]	External/Internal	
DO[0]	External/Internal	

FEEDBACK REQUEST

It should be quite helpful to our ADC core development if you specify your system requirements on ADC in the following characteristic checking table and fill out the additional questions.
We appreciate your interest in our products. Thank you very much.

Characteristic	Min	Typ	Max	Unit	Remarks
Analog Power Supply Voltage				V	
Digital Power Supply Voltage				V	
Bit Resolution				Bit	
Reference Input Voltage				V	
Analog Input Voltage				Vpp	
Operating Temperature				ºC	
Integral Non-linearity Error				LSB	
Differential Non-linearity Error				LSB	
Bottom Offset Voltage Error				mV	
Top Offset Voltage Error				mV	
Maximum Conversion Rate				MSPS	
Dynamic Supply Current				mA	
Power Dissipation				mW	
Signal-to-noise Ratio				dB	
Pipeline Delay				CLK	
Digital Output Format (Provide detailed description & timing diagram)					

1. Between single input-output and differential input-output configurations, which one is suitable for your system and why?

2. Please comment on the internal/external pin configurations you want our ADC to have, if you have any reason to prefer some type of configuration.

3. Freely list those functions you want to be implemented in our ADC, if you have any.

HISTORY CARD

Version	Date	Modified Items	Comments
ver 1.0	98.12.1	Original version published	
ver 1.1	99.12.13	Pin/Port name change - STCB -> STC	The operation is not changed
ver 1.2	00.4.17	Add the PHANTOM CELL INFORMATION (11/12)	