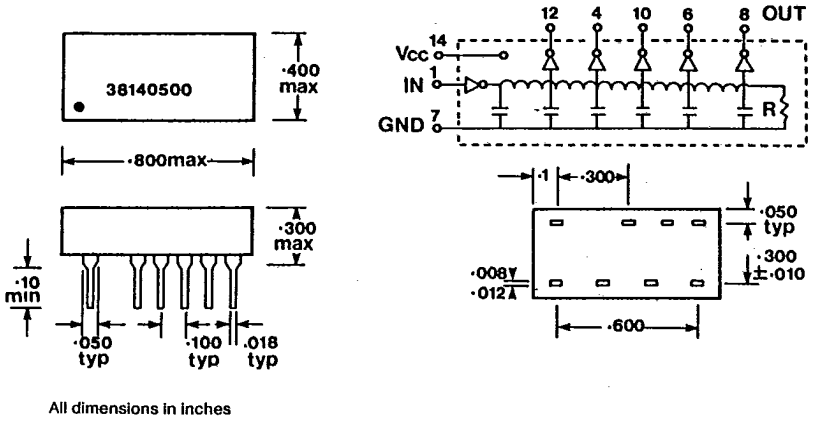
DIGITAL ACTIVE DELAY LINES

5-TAP

(A) (C) Total Delay ns	(A) (C) Tap to Tap Delay ns	(B) (C)) Rise Time Max. ns	14 Pin Code
25	5	3	38140501
30	6	3	38140502
35	7	3	38140503
40	8	3	38140504
45	9	3	38140505
50	10	3	38140506
75	15	3	38140507
100	20	3	38140508
150	30	4	38140509
200	40	4	38140510
250	50	4	38140511

Other delays up to 500 ns available.

16 pin dual-in-line package available on request.

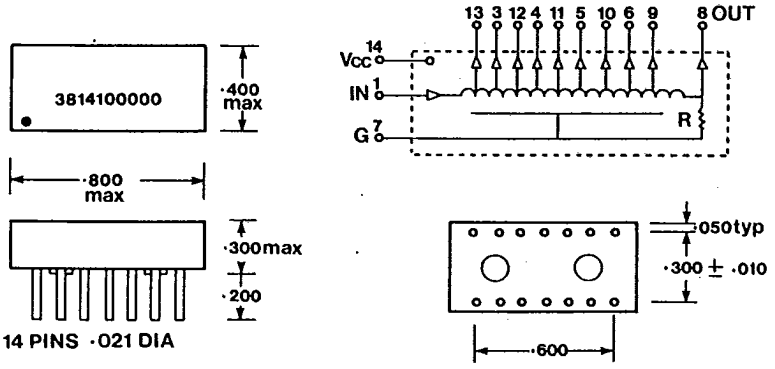


All dimensions in inches

- TTL, DTL COMPATIBLE
- DECOUPLING CAPACITOR INCLUDED
- DELAYS 50 ns to 500 ns

10-TAP

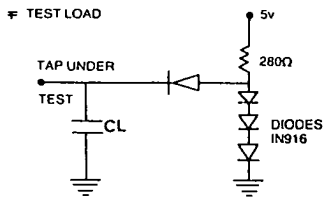
(A) (C) Total Delay ns	(A) (C) Tap to Tap Delay ns	(B) (C)) Rise Time Max. ns	Order Code
50	5	4	3814100050
100	10	4	3814100100
150	15	4	3814100150
200	20	4	3814100200
250	25	4	3814100250
300	30	5	3814100300
350	35	5	3814100350
400	40	5	3814100400
450	45	6	3814100450
500	50	6	3814100500



(A) Measured at 1.5v level on leading edge.
(B) Measured between 0.75v and 2.4v on leading edge.
(C) Measured with one TTL load/tap.

INPUT TEST CONDITIONS

Vcc	5.0v ± 0.25v
Supply Current	60 mA
Pulse Voltage	3.2v
Pulse Width	40% of Total Delay min.



All units are encapsulated in a high grade falem retardent epoxy resin

ELECTRICAL SPECIFICATIONS

Delay Range	25 ns to 250 ns ±5% or ±2 ns whichever is greater
Tap to Tap Tolerance	± 10% of delay between taps or ±1 ns whichever is greater
Logic 0 Input Current	0.2 mA maximum
Logic 1 Input Current	50 us maximum
Logic 0 Voltage Out	0.4 V maximum
Logic 1 Voltage Out	2.7 V minimum
Fan-Out Capabilties	10 TTL Loads/Tap. max. or 20 TTL Loads/ Network max.
Operating Temperature	0°C to + 70°C

Other tolerances, delays, impedances available upon request.