EP910A EPLD

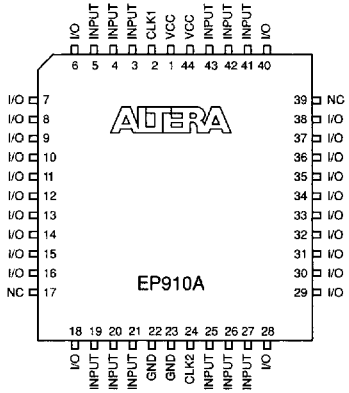
Features

Preliminary Information

- Highest-performance, 24-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} = 10 ns
  - Counter frequencies up to 100 MHz
  - Pipelined data rates up to 125 MHz
- Fabricated on advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture with up to 36 inputs or 24 outputs
- Pin-, function-, and programming file-compatible with Altera's EP910 and EP910T EPLDs
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in a reprogrammable plastic 44-pin J-lead chip carrier (PLCC) package (see Figure 24)

Figure 24. EP910A Package Pin-Out Diagram

Package outline not drawn to scale.



44-Pin J-Lead

General Description

The Altera EP910A EPLD is a high-speed, EEPROM-based version of the EP910 device. Fully compatible with EP910 devices, the EP910A offers enhanced performance for existing EP910 designs with no additional design modifications. For information on the device architecture, refer to Figure 22 earlier in this data sheet.

5 Classic

Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–250	250	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1200	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			25	ns
t_F	Input fall time			25	ns

DC Operating Conditions

Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC3}	V_{CC} supply current (active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *Notes (4), (5)*		120	180 (255)	mA

Capacitance

Note (6)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (3)*

			EP910A-10		EP910A-12		EP910A-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		10		12		15	ns
t_{PD2}	I/O input to non-registered output			10		12		15	ns
t_{PZX}	Input to output enable			11		13		16	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (7)*		11		13		16	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		11		13		16	ns

Global Clock Mode			EP910A-10		EP910A-12		EP910A-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (8)*	125		100.0		83.3		MHz
t_{SU}	Input setup time		7		8		10		ns
t_{H}	Input hold time		0		0		0		ns
t_{CH}	Clock high time		4		5		6		ns
t_{CL}	Clock low time		4		5		6		ns
t_{CO1}	Clock to output delay			6		7		8	ns
t_{CNT}	Minimum clock period			10		12		14	ns
f_{CNT}	Internal maximum frequency	*Note (4)*	100		83.3		71.4		MHz

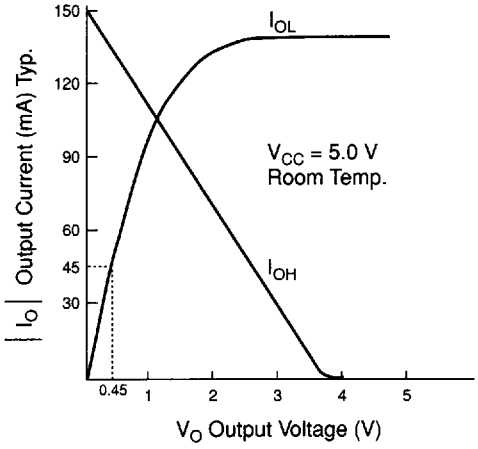
Array Clock Mode			EP910A-10		EP910A-12		EP910A-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (8)*	125		100		83.3		MHz
t_{ASU}	Input setup time		3		4		5		ns
t_{AH}	Input hold time		3		4		5		ns
t_{ACH}	Clock high time		4		5		6		ns
t_{ACL}	Clock low time		4		5		6		ns
t_{ACO1}	Clock to output delay			10		12		14	ns
t_{ACNT}	Minimum clock period			10		12		14	ns
f_{ACNT}	Internal maximum frequency	*Note (4)*	100		83.3		71.4		MHz

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(3) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(4) Measured with a device programmed as a 24-bit counter. I_{CC} measured at 0° C. Actual I_{CC} should be verified during operation because this measurement is sensitive to the operating conditions and the actual pattern in the device.
(5) Numbers in parentheses are for military and industrial temperature versions.
(6) Capacitance measured at 25° C. Sample-tested only. CLK2 (high-voltage pin during programming) has a maximum capacitance of 20 pF.
(7) Sample-tested only for an output change of 500 mV.
(8) The f_{MAX} values represent the highest frequency for pipelined data.

Figure 25 shows the maximum output drive characteristics of EP910A I/O pins.

Figure 25. EP910A Maximum Output Drive Characteristics



Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EP910A-10, EP910A-12, EP910A-15
Industrial Temp.	(–40° C to 85° C)	EP910A-15
Military Temp.	(–55° C to 125° C)	Consult factory