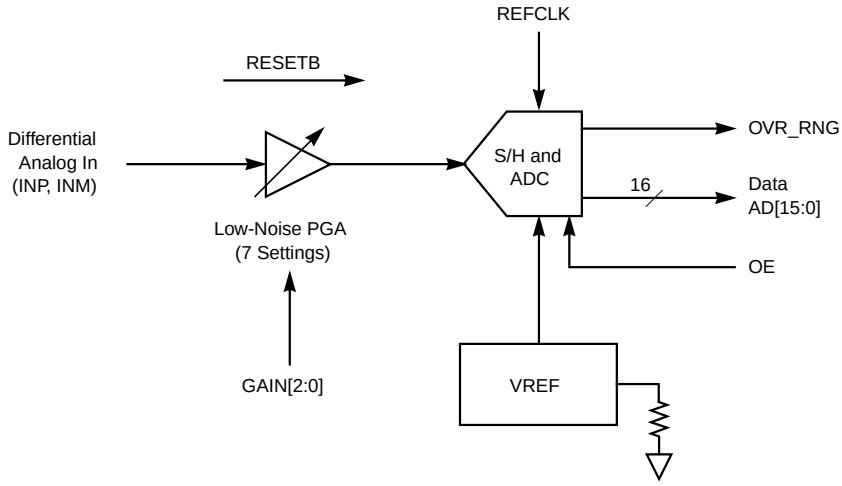
DPS9245
High-Resolution ADC with PGA

Datasheet

The DPS9245 is a versatile, analog front end that combines a high-resolution 5 megasamples per second (MS/s) 16-bit Analog-to-Digital Converter (ADC), a built-in reference, and a Programmable Gain Amplifier (PGA) with resistive input impedance in a 44-pin package.

Figure 1 DPS9245 Block Diagram



The chip includes a digitally-calibrated, pipeline ADC that is calibrated upon assertion of a simple reset signal. The combination of a low-noise, high-linearity, high-input impedance buffer (with programmable gain), wideband S/H, on-board voltage references, and simple digital interface (16-bit parallel output word synchronous with the master sampling clock), makes the chip extremely easy to use in a wide variety of systems. The analog inputs should be driven differentially, and can be AC-coupled or DC-coupled to a source. Typical applications include high-performance data acquisition systems, automatic test equipment, and wideband digital communications receivers present in systems such as wireless basestations. The performance of the device with respect to linearity and noise should be considered separately, as indicated by the THD and SNR specifications provided in this document.

Features

- 16-bit 5 MS/s ADC with on-board voltage reference, programmable gain amplifier and S/H
- Minimal external components: one precision resistor and decoupling capacitors
- 5 V peak-to-peak differential input range
- Resistive inputs > 1 kΩ – easy to drive, without any switched-capacitor kickback transient
- Low-frequency DNL: ±0.5 LSB at 16 bits
- Low-frequency INL: ±1.25 LSB at 16 bits
- Programmable gain amplifier preceding ADC with up to 20 dB of gain (7 settings: 0dB, +3dB, +6dB, +12dB, +15dB, +18dB, +20dB)
- PGA input-referred noise floor at peak gain: 8 nV/√Hz
- Higher performance upgrade from AD9260, AD9240, AD9241, or AD9243
- 5 V 5% power supply; 3.3-V supply for all digital I/O
- User-programmable power dissipation depending on sample rate and linearity required
  - 230 mW at 2.5 MS/s
  - 465 mW at 5 MS/s
- 44-pin LQFP plastic package
- Operating temperature range: –40 °C to +85 °C

Electrical Specifications

Table 1 provides the electrical specifications for the DPS9245. Unless otherwise stated, the following conditions apply:

- Operating temperature range: –40 °C to +85 °C
- VDD_ADC = VDDD_ADC = 5.0 V
- VDD_ADIO = 3.3 V

- 5.0 MS/s
- REXT = 1.43 kW

Table 1 Electrical Specifications

Parameter	Min	Typ	Max	Units	Notes/Conditions
Resolution	15.9	–	–	bits	See "Digital Code Range and Out-of-Range Detection," page 17
Maximum conversion rate	5.0	–	–	MS/s	
Power Supplies					
VDD_ADC, VDDD_ADC[1]	4.75	5.0	5.25	V	
VDD_ADIO[1]	3.0	3.3	5.25	V	Supply for the ADC digital outputs
VDD_ADC, VDDD_ADC combined supply current	–	93	103	mA	With REXT = 1.43 kΩ
PGA Specifications[2]					
Input-referred noise floor	–	45.0 8.0	–	nV/√Hz nV/√Hz	PGA gain = 0dB PGA gain = 20dB At frequencies > 300 kHz
PGA gain		0.0	–	dB	GAIN[2:0] = 000
	–	2.9	–	dB	GAIN[2:0] = 001
	–	5.8	–	dB	GAIN[2:0] = 010
	–	11.8	–	dB	GAIN[2:0] = 011
	–	14.8	–	dB	GAIN[2:0] = 100
	–	17.5	–	dB	GAIN[2:0] = 101
	–	19.5	–	dB	GAIN[2:0] = 110
PGA gain accuracy	–0.3	0	+0.3	dB	
Input resistance[1]	1	–	–	kΩ	On pins INP, INM
Input capacitance[1]	–	–	15	pF	On pins INP, INM

Table 1 Electrical Specifications (Cont.)

Parameter	Min	Typ	Max	Units	Notes/Conditions
DC Specifications					
ADC differential reference	2.375	2.5	2.625	V	Voltage between ADC_REFP (pin 37) and ADC_REFM (pin 36)
ADC positive reference	–	3.65	–	V	Voltage between ADC_REFP (pin 37) and GND
ADC negative reference	–	1.15	–	V	Voltage between ADC_REFM (pin 36) and GND
Input common mode reference (RXCMIN)	2.275	2.400	2.525	V	Minimum load 50 kΩ to ground
Gain Accuracy Specifications					
Gain error	–7.5	–	+7.5	%FSR	Total gain error of PGA and ADC (using internal references) compared to ideal quantizer with perfect 5.0 V full-scale range preceded by an ideal PGA with gain equal to the nominal values (i.e., 0 dB, 2.9 dB, 5.8 dB, 11.8 dB, 14.8 dB, 17.5 dB, 19.5 dB)
Static Linearity Specifications					
DNL	–	±0.5	–	LSB	At 16-bit level
INL	–	±1.25	–	LSB	At 16-bit level

1. Not tested in production, but guaranteed by design or characterization.
2. In the remainder of this document, the PGA gains are often rounded to the nearest integer value. For example, the GAIN[2:0] = 110 setting is referred to as 15 dB even though its typical value is 14.8 dB.

Table 2 Digital I/O DC Electrical Characteristics

Parameter	Min	Typ	Max	Units	Notes/Conditions
V_{OH} (High-level output voltage)	VDD-0.5	–	–	V	At I_{OH} = –2 mA
V_{OL} (Low-level output voltage)	–	–	0.5	V	At I_{OL} = 2 mA
I_{IL} (Input leakage current)	–10	–	+10	µA	
V_{IH} (High-level input voltage)	2.4	–	–	V	
V_{IL} (Low-level input voltage)	–	–	0.8	V	

Note: For all digital outputs, the V_{OH} specification of VDD-0.5V refers to the VDD_ADIO supply (pin 6). The exception is the BUSYB output (pin 33), whose output HIGH level is referenced to the VDDD_ADC power supply (pins 3, 4).

Dynamic Linearity Specifications for Sinusoidal Differential Analog (SDA) Input

Table 3 provides the dynamic linearity specifications for SDA input. The conditions are:

- VDD_ADC = VDDD_ADC = 5.0 V
- VDD_ADIO = 3.3 V
- REXT = 1.43 kΩ.

The following notes apply:

1. The signal level relative to full-scale (dBFS) is given at the ADC input – that is, *after* the PGA – in order to show the dependence on PGA gain.
2. 0 dBFS is 5.0V peak-to-peak differential.
3. Second harmonic distortion (HD2), 3rd harmonic distortion (HD3), total harmonic distortion up to and including the 9th harmonic (THD_9), and spurious free dynamic range (SFDR), are given in dB below the fundamental (carrier).

Table 3 Dynamic Linearity Specifications for Sinusoidal Differential Analog Input

Sample Rate [MS/s]	Signal Frequency [kHz]	PGA Setting [dB]	Composite Signal Level at ADC Input [dBFS][1]	HD2	HD3	THD_9	SFDR
5.0	70	0	–0.5	–94 dB max	–85 dB max	–84 dB max	85 dB min
5.0	70	0	–0.5	–103 dB typ	–97 dB typ	–92 dB typ	94 dB typ
5.0	70	20	–0.5	–101 dB typ	–93 dB typ	–90 dB typ	92 dB typ
8.8	60	0	–0.5	–103 dB typ	–97 dB typ	–92 dB typ	94 dB typ
5.0	900	12	–11.0	–104 dB typ	–97 dB typ	–94 dB typ	97 dB typ
5.0	900	15	–8.1	–104 dB typ	–94 dB typ	–91 dB typ	94 dB typ
5.0	900	18	–5.4	–103 dB typ	–88 dB typ	–88 dB typ	88 dB typ
5.0	900	20	–3.4	–101 dB typ	–85 dB typ	–84 dB typ	85 dB typ
5.0	900	20	–1.1	–99 dB typ	–84 dB typ	–82 dB typ	84 dB typ

1. dBFS is dB below full scale signal level, which is 5 V peak-to-peak differential.

Dynamic Linearity Specifications for Two-Tone Differential Analog Input

Table 4 provides the dynamic linearity specifications for two-tone differential analog input. The following conditions apply:

- VDD_ADC = VDDD_ADC = 5.0 V
- VDD_ADIO = 3.3 V
- REXT = 1.43 kΩ

The following notes apply:

1. The composite signal level relative to full-scale (dBFS) is given at the ADC input – that is, *after* the PGA – in order to show the dependence on PGA gain.
2. 0 dBFS is 5.0V peak-to-peak differential.

3. Third-order and 5th-order intermodulation distortion, IM3 and IM5 respectively, are given in dB below carrier – that is, dB below one tone of the two-tone signal.

Table 4 Dynamic Linearity Specifications for Two-Tone Differential Analog Input

Sample Rate [MS/s]	Signal Frequencies	PGA Setting [dB]	Composite Signal Level at ADC Input [dBFS]	IM3	IM5
4.4	100 kHz, 110 kHz	6	–0.8	–98 dB typ	–101 dB typ
4.4	100 kHz, 110 kHz	20	–0.3	–96 dB typ	–99 dB typ
8.8	100 kHz, 110 kHz	6	–1.8	–97 dB typ	–97 dB typ
8.8	100 kHz, 110 kHz	20	–1.3	–96 dB typ	–98 dB typ
4.4	400 kHz, 410 kHz	6	–0.7	–94 dB typ	–95 dB typ
4.4	400 kHz, 410 kHz	20	–0.2	–92 dB typ	–95 dB typ
8.8	400 kHz, 410 kHz	6	–1.8	–93 dB typ	–96 dB typ
8.8	400 kHz, 410 kHz	20	–1.3	–93 dB typ	–96 dB typ
4.4	890 kHz, 900 kHz	0	–1.9	–89 dB typ	–97 dB typ
8.8	890 kHz, 900 kHz	6	–3.0	–89 dB typ	–98 dB typ
8.8	890 kHz, 900 kHz	20	–1.4	–87 dB typ	–94 dB typ
5.0	1.03 MHz, 1.04 MHz	6	–2.4	–82 dB max	–89 dB max
5.0	1.03 MHz, 1.04 MHz	6	–2.4	–87 dB typ	–97 dB typ
5.0	1.03 MHz, 1.04 MHz	20	–0.8	–84 dB typ	–95 dB typ

SNR Specifications for Balanced Differential Analog Input

Table 5 provides SNR specifications for balanced differential analog input. The following conditions apply:

- 5 MS/s
- VDD = 5.0 V
- VDD_ADIO = 3.3 V

- REXT = 1.43 kΩ.

Note: In Table 5, the signal level is given both at the PGA input (the chip input) and at the ADC input – that is, *after* the PGA – in order to show the dependence on PGA gain or input signal level.

Extrapolated Dynamic Range (EDR) is a measure of overall converter sensitivity. It is obtained from a plot of SNR versus signal amplitude at the chip input, extrapolated to 0 dB. EDR can also be calculated for a given scenario by adding the SNR to the amount in dB by which signal level is below full scale.

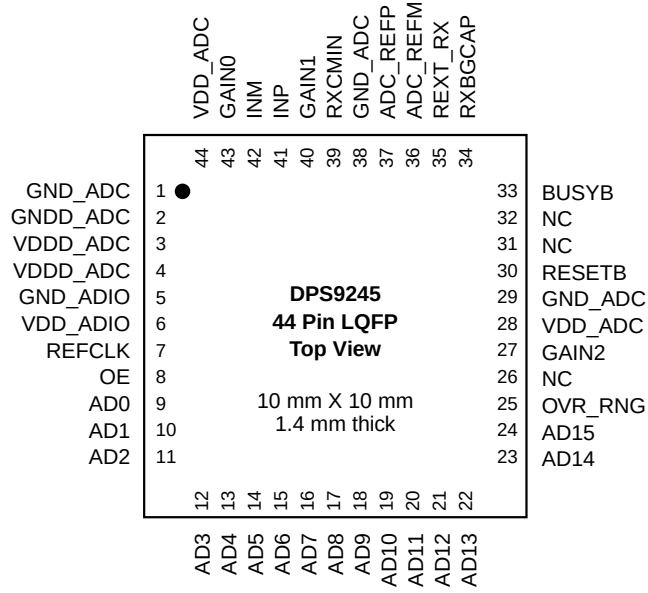
Table 5 SNR Specifications for Balanced Differential Analog Input

Signal Type	Signal Frequency [kHz}	PGA Gain [dB]	Composite Signal Level at PGA Input [dBFS]	Composite Signal Level at ADC Input [dBFS]	SNR	Extrapolated Dynamic Range
Sinusoid	75	0	–1	–1	78 dB min	79 dB min
Sinusoid	75	0	–1	–1	81 dB typ	82 dB typ
Sinusoid	75	19.5	–20.5	–1	76 dB typ	96.5 dB typ
Sinusoid	75	0	–59.5	–59.5	25 dB typ	84.5 dB typ
Sinusoid	75	19.5	–60	–40.5	38.5 dB typ	98.5 dB typ
Sinusoid	900	0	–1	–1	80 dB typ	81 dB typ
Sinusoid	900	0	–40	–40	45.5 dB typ	85.5 dB typ

DPS9245 Pinouts

Figure 2 provides a pinout diagram of the DPS9245.

Figure 2 DPS9245 Pinout Diagram



Pin Descriptions

Table 6 provides a functional definition of each signal pin listed in numerical order.

Table 6 Pin Signal Functions

Pin Number	Pin Name	Type[1]	Pin Function Description
1, 29, 38	GND_ADC	S	Analog ground
2	GNDD_ADC	S	Digital ground
3,4	VDDD_ADC	S	Digital +5.0 V supply
5	GND_ADIO	S	Ground for digital I/O
6	VDD_ADIO	S	Power supply for ADC outputs (+3.3 V or +5 V)
7	REFCLK	DI	Master reference clock
8	OE	DI	Output enable (active HIGH)
9-24	AD0-AD15	DO	Data output bits AD0 is LSB; AD15 is MSB
25	OVR_RNG	DO	Over range indicator bit (active HIGH)
26	NC		No connect
27, 40, 43,	GAIN[2:0]	DI	3-bit PGA gain control
28, 44	VDD_ADC	S	Analog +5.0 V supply
30	RESETB	DI	Resets internal state of chip (active LOW)
31, 32	NC		No connects
33	BUSYB	DO	Initialization in progress indicator (active LOW)
34	RXBGCAP	AO	External bias capacitor connection
35	REXT_RX	AO	External bias resistor connection
36, 37	ADC_REFM, ADC_REFP	AO	ADC reference voltage outputs
39	RXCMIN	AO	Common-mode reference voltage output
41, 42	INP, INM	AI	Analog inputs to the ADC

1. Type definitions:
   AI = analog input
   AIO = analog I/O
   AO = analog output
   DI = digital input
   DIO = digital I/O
   DO = digital output
   S = supply (VDD or GND)

IC Operation and Functionality

The following sections describe in greater detail the individual blocks and functions of the DPS9245:

- Overview
- Chip Startup/Initialization Sequence
- Analog Input Interfacing
- External Connections
- ADC Digital Output Timing
- ADC References
- Other ADC Functions
- Programmable Gain Amplifier

Overview

The incoming analog differential signal (maximum level 5 V peak-to-peak differential) enters the chip at the INP/INM pins. The analog signal path is partitioned into a programmable gain amplifier (PGA) and an ADC. The PGA has maximum gain of +20 dB; the gain is set by the digital control signals GAIN[2:0]. The output of the PGA is fed directly to the ADC, which samples at a rate equal to the REFCLK frequency and outputs a 16-bit wide parallel word.

The ADC uses a pipeline multistage architecture. Latency is 6 clock cycles.

The chip requires a single low-jitter clock to be applied at the REFCLK pin, with nominal 50% duty cycle. All clock generation is performed internally and all converter and S/H clocks in the ADC path are directly derived from REFCLK.

Chip Startup/Initialization Sequence

Warning: This initialization sequence is *required*. Without it, the chip will not work.

Note that the analog blocks on the chip require significant time to power on and come up to their quiescent dc states; for example, the voltage reference power-on time depends on the value of the external reference decoupling capacitance. Allowance may also be needed for thermal time constants associated with the package/board.

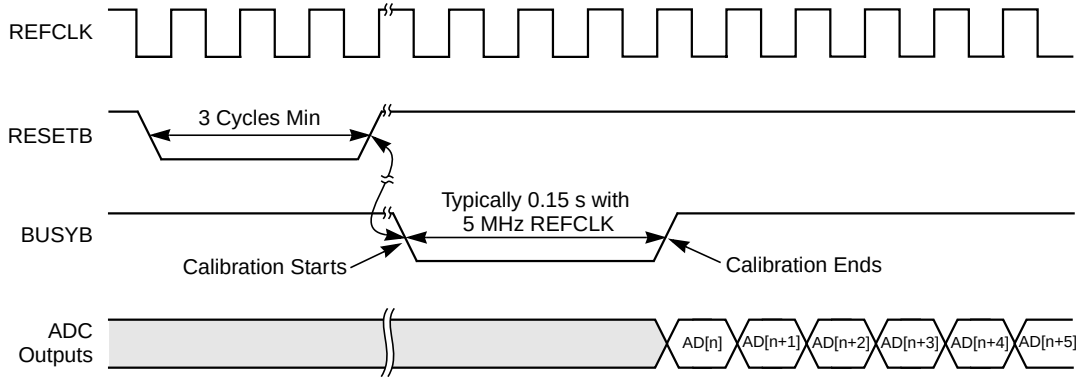
On power-up, RESETB should be held LOW for at least three cycles of the clock signal, REFCLK, as shown in Figure 3 below. The power supply voltages applied to the chip must be stable during this time. REFCLK must be running for at least three clock cycles prior to the rising edge of RESETB, and must continue running.

The initialization phase begins on the rising edge of RESETB. No more than two full REFCLK cycles after the rising edge of RESETB, BUSYB, an active LOW signal (pin 33), is driven LOW. An internal sequencer performs the ADC calibration while BUSYB is LOW. When the initialization is complete, BUSYB is driven HIGH and the chip is ready for normal operation. The duration of the initialization phase, (the time BUSYB is LOW) is 150 ms, assuming a 5 MS/s sampling rate.

Notes:

- The digital output BUSYB cannot be 3-stated: it is always driven either HIGH or LOW.
- The REFCLK clock must be constantly running throughout the initialization phase until BUSYB goes HIGH.
- Initialization will restart whenever RESETB is cycled; thus, for initialization to complete correctly, RESETB should not be cycled while BUSYB is LOW.
- Although typically the chip is initialized when power is first applied, the initialization only occurs when the RESETB is cycled. There is no “power-on-reset” circuitry on the chip.

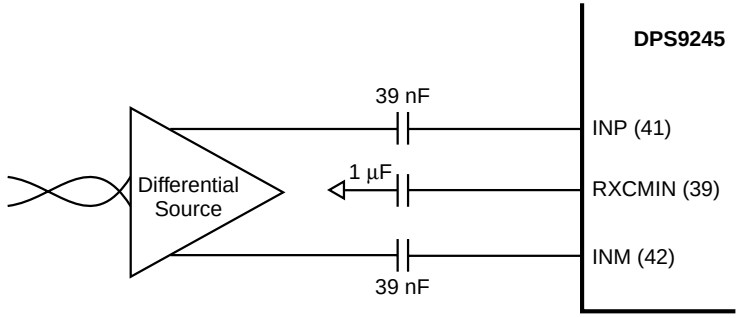
Figure 3 Chip Initialization Timing



Analog Input Interfacing

The differential analog inputs (INP, INM) have a resistive input impedance of 1kΩ minimum. For best performance, the input source should be capacitively coupled into the chip, as shown below in Figure 4. To avoid clipping, signal swing at the inputs should not exceed 5 V peak-to-peak differential (2.5 V peak-to-peak single ended). The chip provides its own common-mode voltage (on the pin marked RXCMIN), and the input common mode is established internally.

Figure 4 Recommended Analog Input Interface – Using An AC-Coupling Approach



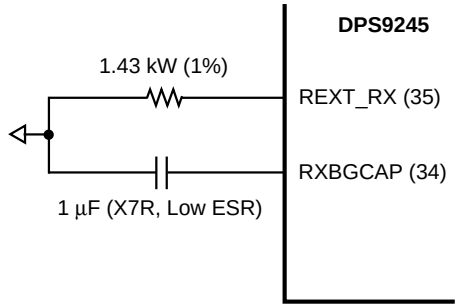
Alternatively, the inputs may be dc-coupled by using an external network to reference the input common mode to the voltage on pin RXCMIN.

Output drive capability of RXCMIN is a maximum of 47 µA (50 kΩ to ground). Output impedance of the RXCMIN voltage reference is typically 1 kΩ, and hence the 1 µF decoupling capacitor should always be present, as shown in Figure 4.

External Connections

The connections to the two pins {REXT_RX, RXBGCAP} are critical and should be routed very carefully on the board. The connections are as shown in Figure 5 below. The traces to/from these pins should be as short as possible.

Figure 5 Recommended Connection for Pins 34–35



External Resistor (REXT)

REXT, shown in Figure 5 above, sets the power dissipation of the chip and may be used to trade off power dissipation against linearity at high sample rates, and/or at high input frequencies. Nominally, at 5 MS/s, REXT=1.43 kΩ is recommended. If linearity for large signal levels at an analog bandwidth of 2 MHz is critical, the value should be decreased to REXT=1.24 kΩ; and for even higher-frequency analog inputs, REXT=1.0 kΩ can be used. At lower sample rates (for example 2 MS/s), and lower analog input frequencies, the value may be increased to REXT=2 kΩ. The section, "Typical Performance Characteristics" (on page 18) contains performance characteristics that show how dynamic linearity depends on the REXT value.

As a general guideline, REXT should always be in the range 800 Ω to 2.5 kΩ. Contact LSI Logic for the most up-to-date recommended values for a given application.

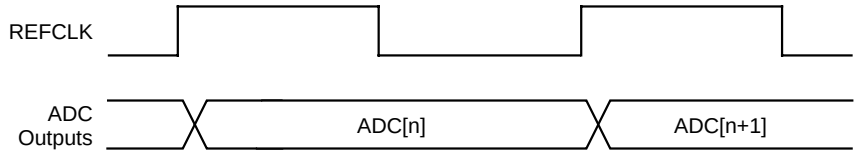
External Capacitor (CEXT)

CEXT is used only for noise filtering of an internal voltage associated with the references. Its value is not critical. 1 µF is recommended.

ADC Digital Output Timing

The chip implements a simple interface: the 16 ADC outputs appear on the pins AD[15:0] as a parallel word synchronous with the ADC sampling clock. AD0 is the LSB and AD15 is the MSB. The timing diagram for the ADC digital outputs is shown in Figure 6. The ADC sampling clock is at the same frequency as REFCLK.

Figure 6 Waveform for ADC Outputs



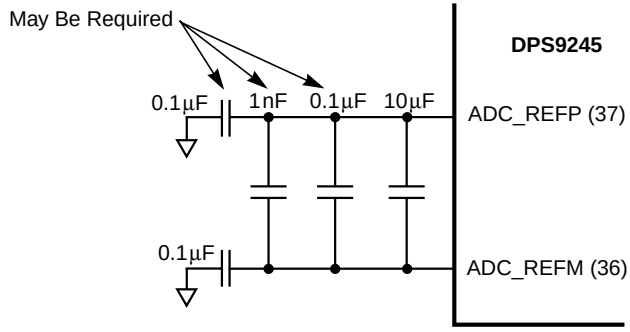
The data changes on the rising edge of REFCLK and can be latched by a DSP on the falling edge. The latency through the ADC from the PGA output to the digital outputs is 6 clock cycles of the ADC clock. The voltage levels on the AD[15:0] lines are CMOS levels. The HIGH level is determined by the power supply voltage on the VDD_ADIO pin, which can be set independently of the other supply pins on the chip over the range from 3.0 V to 5.25 V. Typically, VDD_ADIO should be +3.3 V, which ensures that the ADC outputs are both TTL-compatible and 3.3 V-CMOS compatible.

ADC References

The ADC full scale range is set by reference voltages generated on chip. These two reference voltages appear on pins ADC_REFP and ADC_REFM; nominally their difference is 2.5 V. The references are not designed to be overdriven. The ADC_REFP and ADC_REFM pins

should be very carefully decoupled on the board using a 10 µF low-ESR capacitor and as short a trace as possible. Some optimization of the decoupling may be required, as shown in Figure 7.

Figure 7 Recommended Decoupling of ADC_REFP and ADC_REFM Pins



Other ADC Functions

Output Enable

The ADC digital outputs are enabled by the active HIGH output enable pin (OE).

OE = 1, ADC digital outputs AD[15:0] are enabled

OE = 0, ADC digital outputs AD[15:0] are high-impedance (3-stated)

Output Format

The output format of the ADC digital data is offset binary. Therefore, for the nominal differential range of 5 V peak-to-peak differential, the following values apply:

Output	Corresponds to
0000H	–2.5 V differential
8000H	0 V differential
FFFFH	+2.5 V differential

Digital Code Range and Out-of-Range Detection

Due to the calibration algorithm used, there is a slight loss in digital code range from the ADC. So, instead of FFFFH and 0000H at the extremes of the range, the actual maximum and minimum codes are less than that by a few percentage points, and vary from chip to chip. Effectively, this is a loss in dynamic range of a few tenths of a dB, and is negligible in many applications. The out-of-range function is defined accordingly, and sets the state of the active HIGH digital output, OVR_RNG, as follows:

OVR_RNG is HIGH if the ADC digital code is greater-than-or-equal-to FC00H or less-than-or-equal-to 03FFH.

Programmable Gain Amplifier

From the block diagram in Figure 1, there is a programmable gain amplifier (PGA), that precedes the ADC inputs. The differential inputs, which are resistive, are at pins INP and INM. The maximum input range is 5V peak-to-peak differential (2.5 V peak-to-peak single ended). To achieve maximum overall system noise performance, the source driving these inputs needs to be as low-noise as possible, while maintaining the required distortion performance.

The internal 0 dB analog signal level and ADC full-scale reference level is 5 V peak-to-peak differential (2.5 V peak-to-peak single ended). Thus, if the ADC input level does not exceed 5 V peak-to-peak differential, the PGA may be used to provide gain.

The gain of the PGA can be programmed using a three bit control, available at pins GAIN[2:0]. Table 7 provides a gain chart.

Important: *The GAIN[2:0] = 111 setting is not allowed*. Note that the input resistance is a function of the gain setting.

Table 7 PGA Gain Control

GAIN2	GAIN1	GAIN0	Nominal PGA Gain [dB]	Input Resistance [kΩ]	Comments
0	0	0	0	5.57	Min. gain
0	0	1	3	4.65	
0	1	0	6	3.97	
0	1	1	12	2.23	
1	0	0	15	1.66	
1	0	1	18	1.25	
1	1	0	20	1.00	Max. gain
1	1	1	–	–	Forbidden

Typical Performance Characteristics

Figure 8 shows the Spurious Free Dynamic Range (SFDR), in dB below the carrier, plotted as a function of ADC input amplitude, (post-PGA), in dB below full scale, at 5 V and 25 °C. *The ADC sample rate is 10 MS/s throughout.* The data is given for sinusoidal inputs at 3 frequencies: 0.9 MHz, 2 MHz, and 3 MHz. For each frequency, the SFDR is given for 3 bias conditions: (i) low, using REXT = 1.43 kΩ; (ii) medium, using REXT = 1.24 kΩ, and (iii) high, using REXT = 1 kΩ. The corresponding chip power supply currents for these three bias conditions are 96 mA, 109 mA, and 129 mA, respectively. Note that 0 dBFS corresponds to 5.0 V peak-to-peak differential.

Figure 8 Spurious Free Dynamic Range (SFDR)

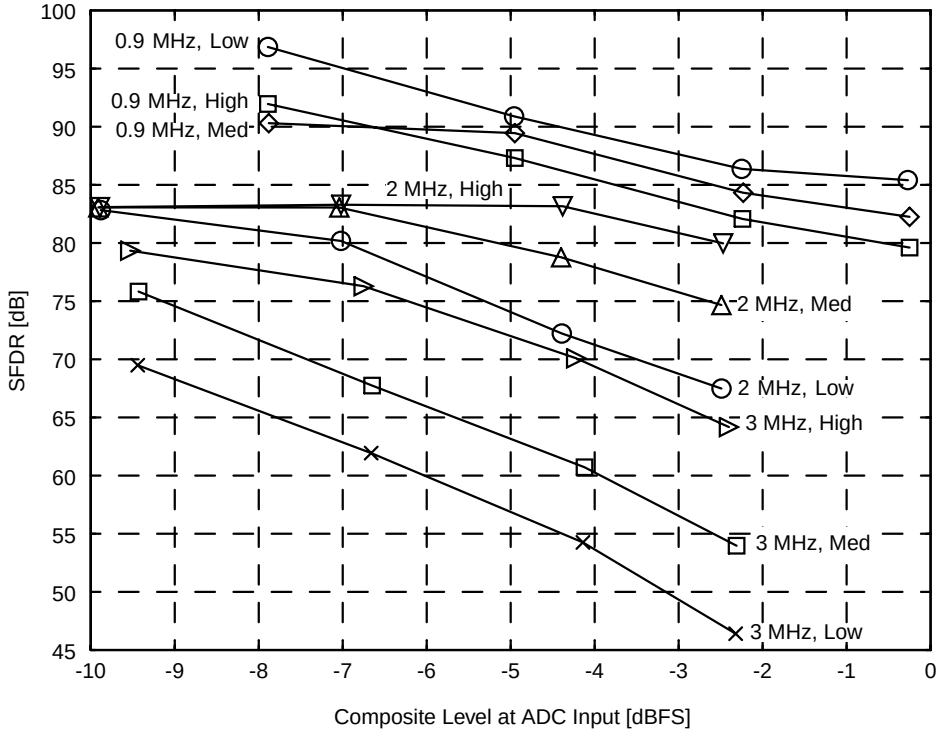


Figure 9 shows the ADC output spectrum for a 900 kHz sine wave input, at 25 °C. The sample rate is 10 MS/s; signal level at ADC input is –5.0 dBFS (i.e., post PGA); REXT = 1.43 kΩ; the PGA is set to 15 dB. The spectrum is generated by averaging multiple FFTs in order to indicate clearly the distortion harmonics.

Figure 9 ADC Output Spectrum (900-kHz Sine Wave Input)

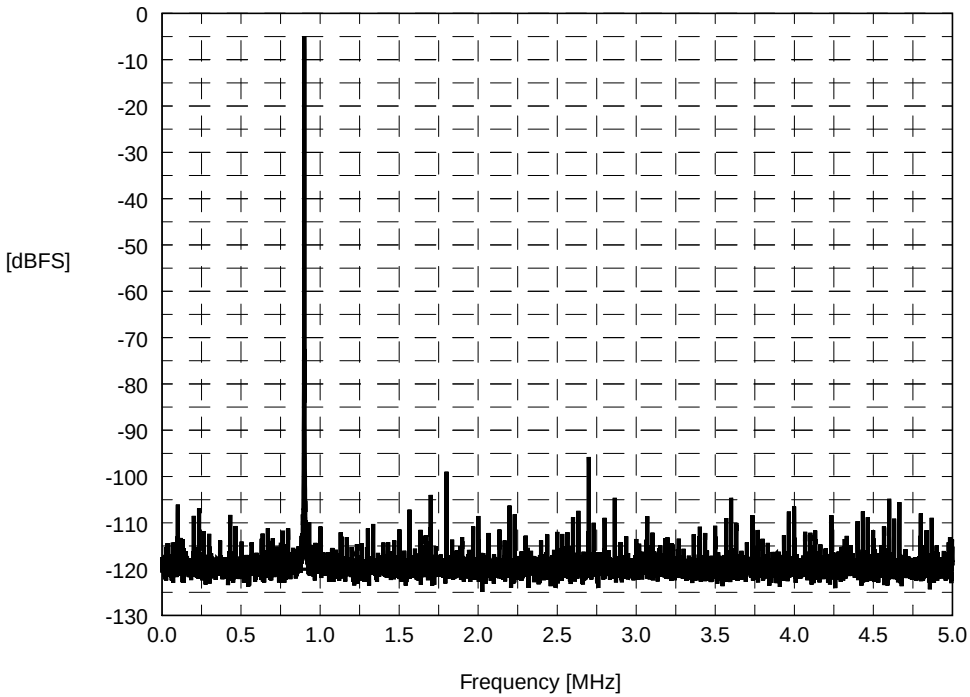


Figure 10 shows the ADC output spectrum for a 2 MHz sine wave input, at 25 °C. The sample rate is 4.4 MS/s; signal level at ADC input is –5.4 dBFS (i.e., post PGA); REXT = 1.08 kΩ; the PGA is set to 18 dB. The spectrum is generated by averaging multiple FFTs in order to indicate clearly the distortion harmonics.

Figure 10 ADC Output Spectrum (2-MHz Sine Wave Input)

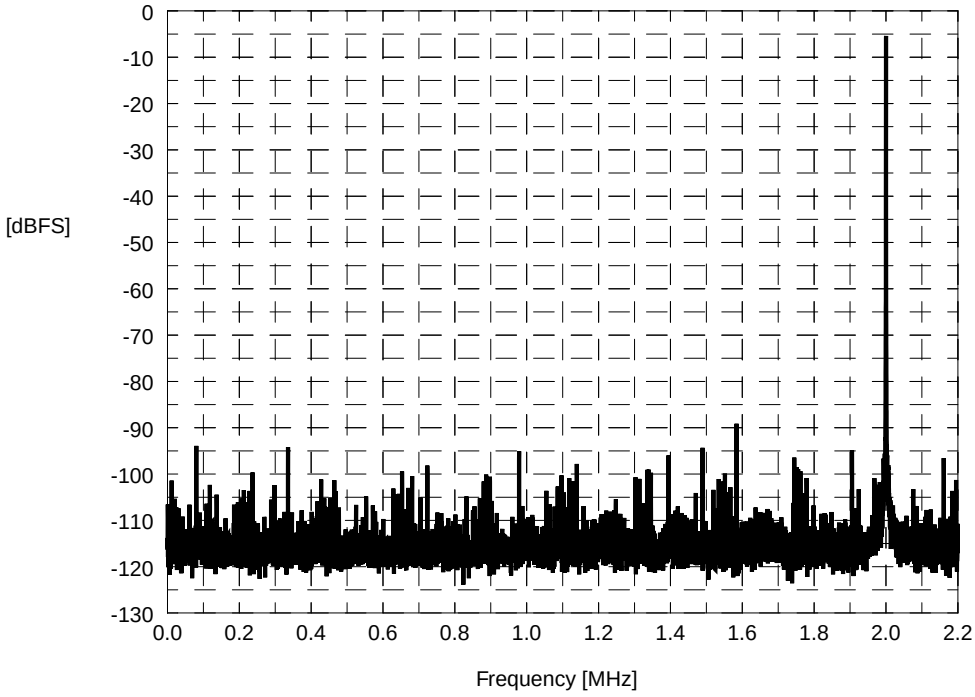


Figure 11 shows a zoomed-in portion of the ADC output spectrum for a 890 kHz/900 kHz two-tone input, at 25 °C. The sample rate is 4.4 MS/s; at the ADC input (i.e., post PGA) the signal level of each tone is –8.0 dBFS and the composite signal level is –2.0 dBFS; REXT = 1.43 kΩ; the PGA is set to 6 dB. The spectrum is generated by averaging multiple FFTs in order to indicate clearly the intermodulation distortion products.

Figure 11 Zoomed-in Portion of ADC Output Spectrum (890/900 kHz Two-Tone Input)

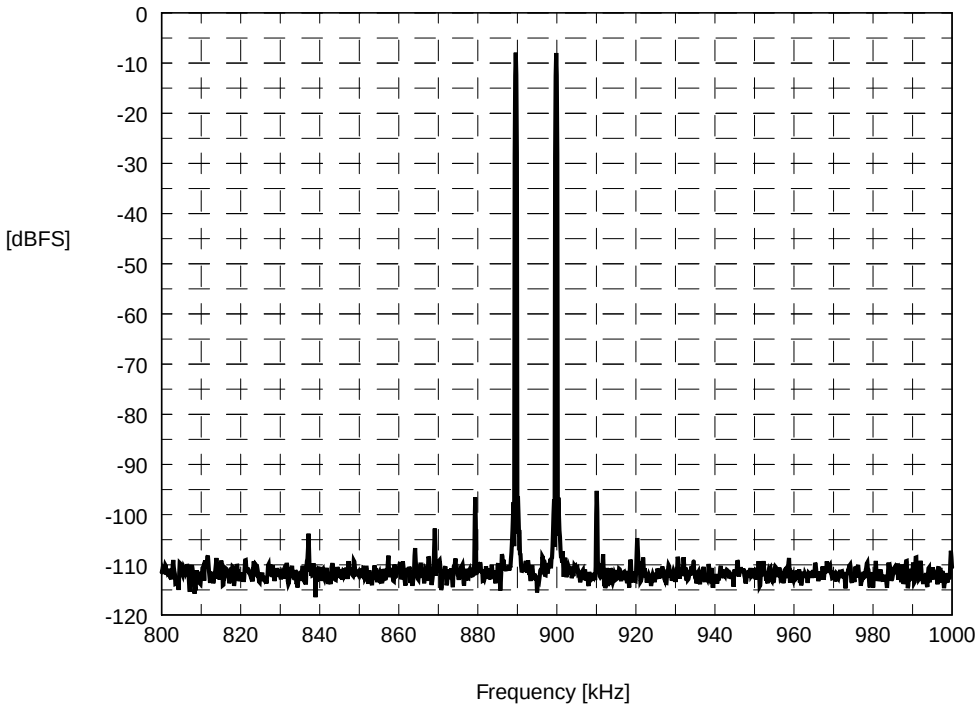
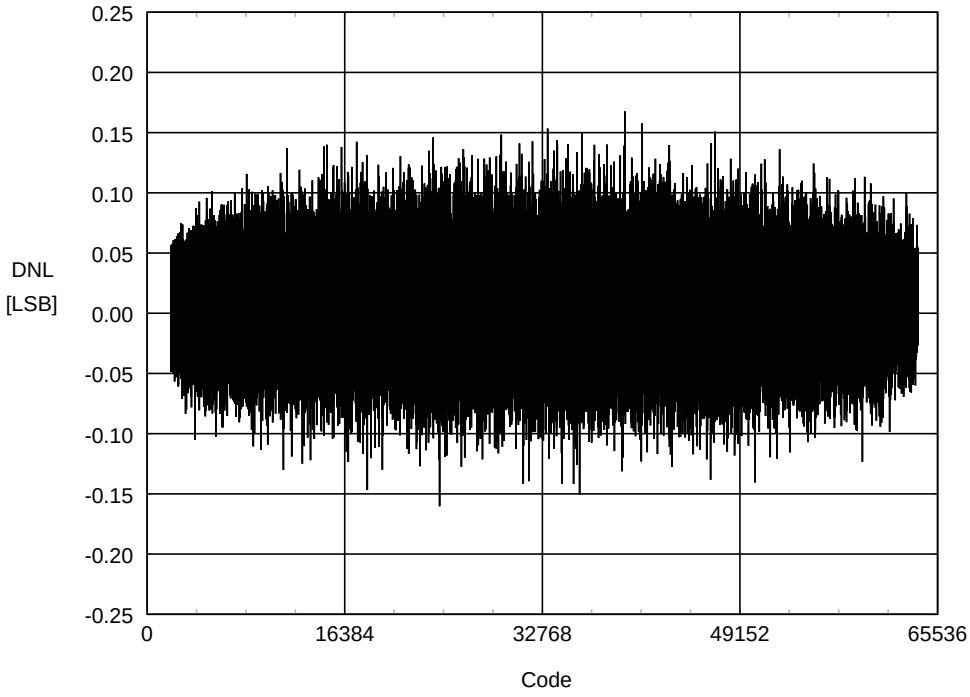


Figure 12 shows the typical Differential Nonlinearity (DNL), at the 16-bit level, measured using a histogram test with a near-full-scale 75 kHz sinusoid input, at 25 °C. The sample rate is 4.4 MS/s, and the PGA is set to 0 dB.

Figure 12 Typical Differential Nonlinearity (DNL) – 16-Bit Level



Timing Specifications

Figure 13 and Table 8 provide timing specifications for the various digital interfaces on the chip.

Figure 13 ADC Timing

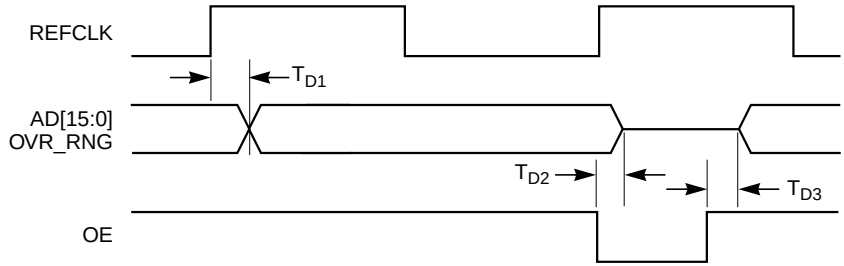


Table 8 ADC Timing

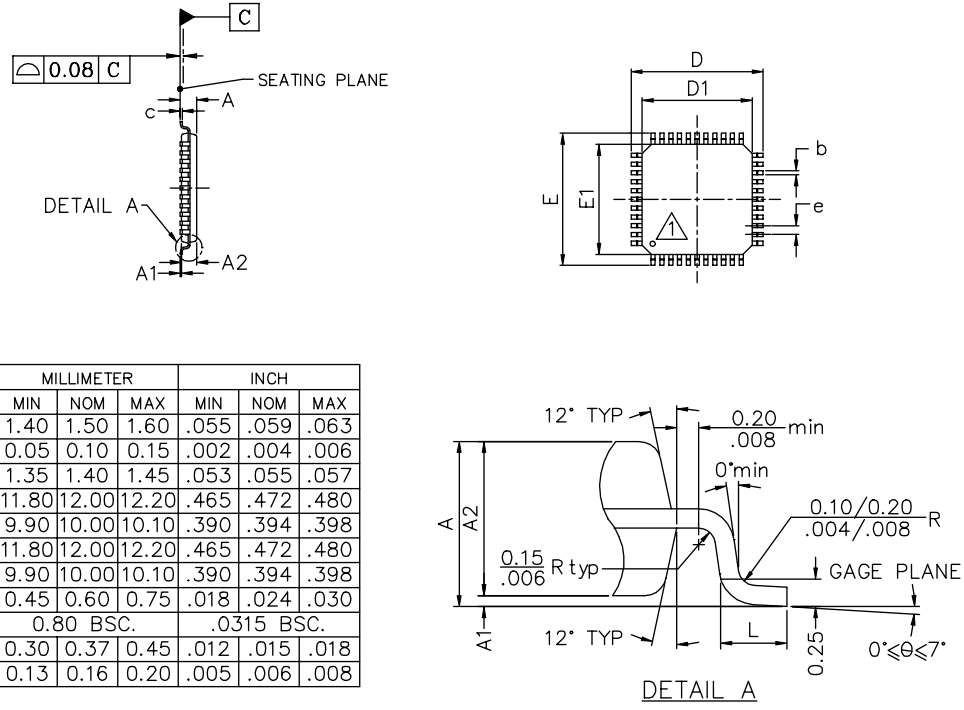
Parameter	Symbol	Min	Typ	Max	Units
REFCLK HIGH to Data Valid	T_{D1}	18	24	40[1]	ns
OE inactive to HiZ	T_{D2}	10	16	30	ns
OE active to Data Valid	T_{D3}	10	16	30	ns

1. Conditions: load capacitance = 20 pF, VOH = 3.3 V

Package Drawing

Figure 14 provides the DPS9245 package drawing.

Figure 14 DPS9245 Package Drawing – 44-Pin LQFP



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.40	1.50	1.60	.055	.059	.063
A1	0.05	0.10	0.15	.002	.004	.006
A2	1.35	1.40	1.45	.053	.055	.057
D	11.80	12.00	12.20	.465	.472	.480
D1	9.90	10.00	10.10	.390	.394	.398
E	11.80	12.00	12.20	.465	.472	.480
E1	9.90	10.00	10.10	.390	.394	.398
L	0.45	0.60	0.75	.018	.024	.030
e	0.80 BSC.			.0315 BSC.		
b	0.30	0.37	0.45	.012	.015	.018
c	0.13	0.16	0.20	.005	.006	.008

NOTE: 1. PIN 1 INDICATOR.
2. REFER TO JEDEC MS–026 BCB FOR DATUMS, FEATURES AND DIMENSIONS NOT SHOWN.
3. CONTROLLING DIMENSION IN MM.

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