Ordering number: EN 4363C

CMOS IC

LC6527N/F/L, 6528N/F/L

Single-chip 4-bit Microcomputer for Small-scale Control-oriented Applications

Overview

The LC6527N/F/L, LC6528N/F/L belong to our single-chip 4-bit microcomputer LC6500 series fabicated using CMOS process technology and are suited for use in small-scale control-oriented applications. Their basic architecture and instruction set are the same. Application areas include the standard logic circuits and applications where the number of controls is small. The LC6527N/F/L, LC6528N/F/L have relation to the LC6527C/H, LC6528C/H. The C version can be replaced by N version, and the H version by F version (a part of the function is different). The L version is added as a low voltage version. The following show the careful difference of C and N version when you replace C version with N version.

Item			C version	N version
Operating Temperature			–30°C to +70°C	–40°C to +85°C
1-pin C oscillation			exist	not exist
CF oscillation constant	400 kHz MURATA		C1 = C2 = 330 pF R = 0 Ω	C1 = C2 = 220 pF R = 2.2 kΩ
	800 kHz	MURATA	C1 = C2 = 220 pF R = 0 Ω	C1 = C2 = 100 pF R = 2.2 KΩ
		KYOCERA	C1 = C2 = 220 pF R = 0 Ω	C1 = C2 = 100 pF R = 0 Ω
	1MHz MURATA		C1 = C2 = 220 pF R = 0 Ω	C1 = C2 = 100 pF R = 2.2 kΩ

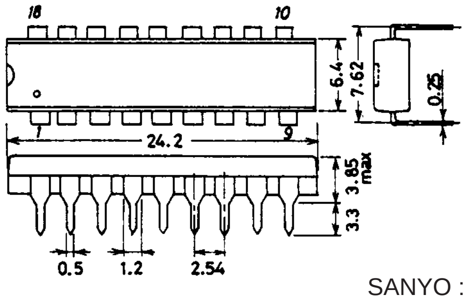
(Note) The suffix of recommend oscillation is changed C version and N version, but the characteristics are no change.

Package Dimensions

unit : mm

3007A-DIP18

[LC6527N/F/L, 6528N/F/L]

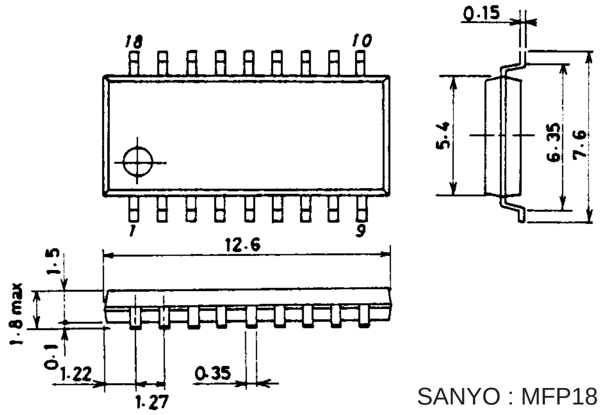


SANYO : DIP18

unit : mm

3095-MFP18

[LC6527N/F/L, 6528N/F/L]



SANYO : MFP18

(Note) The package is the reference figure without the description of the rank. Please inquire us for the formal package.

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Features

1) CMOS technology for a low-power operation (with instruction-controlled standby function)
2) ROM/RAM
   LC6527N/F/L ROM : 1 K × 8 bits, RAM : 64 × 4 bits
   LC6528N/F/L ROM : 0.5 K × 8 bits, RAM : 32 × 4 bits
3) Instruction set : 51 kinds selectable from 80 instructions common to the LC6500 series
4) Wide operationg voltage range form 2.2 V to 6.0 V (L version)
5) Instruction cycle time of 0.92µs (F version)
6) Flexible I/O port
   - Number of ports : 4 ports/13 pins max.
   - All ports : Input/output common
     Input/output voltage 15V max. (open drain type)
     Output current 20mA max. (sink current) (LED direct drivable)
   - Option selectable for your intended system
   A. Open drain output, pull-up resistor : Single-bit select for all ports
   B. Output level at the reset mode : 4-bit select of H/L level for port C/D
7) Stack level : 4 levels
8) Timer : 4-bit prescaler + 8-bit programmable timer
9) Clock oscillation option selectable for your intended system
   - Oscillator option : 2-pin RC oscillaion (N, L version)
     2-pin ceramic resonator oscillation, 1-pin external clock input (N, F, L version)
   - Predivider option : No predivider, 1/3 predivider, 1/4 predivider (N, L version)

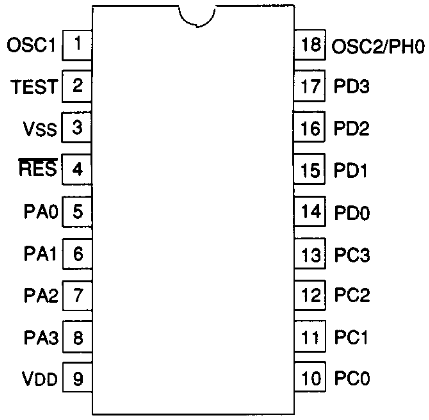
Function Table

Item		LC6527N/28N	LC6527F/28F	LC6527L/28L
Memory	ROM	1024 x 8 bits (27N) 512 x 8 bits (28N)	1024 x 8 bits (27F) 512 x 8 bits (28F)	1024 x 8 bits (27L) 512 x 8 bits (28L)
	RAM	64 x 4 bits (27N) 32 x 4 bits (28N)	64 x 4 bits (27F) 32 x 4 bits (28F)	64 x 4 bits (27L) 32 x 4 bits (28L)
In-struc-tion	Instruction set	51	51	51
On-chip function	Timer	4-bit prescaler + 8-bit timer	4-bit prescaler + 8-bit timer	4-bit prescaler + 8-bit timer
	Stack level	4	4	4
	Standby function	Standby available by HALT instruction	Standby available by HALT instruction	Standby available by HALT instruction
Input/output port	Number of ports	I/O 13 max.	I/O 13 max.	I/O 13 max.
	I/O voltage	15V max.	15V max.	15V max.
	Output current	10mA typ. 20mA max.	10mA typ. 20mA max.	10mA typ. 20mA max.
	I/O circuit configuration	Open drain (N channel) or pull-up resistor-provided output selectable bit by bit.		
	Output level at reset mode	"H" or "L" level selectable port by port (port C, D only)		
Characteristic	Minimum cycle time	2.77µs (V_{DD}≥4V) 6.0µs (V_{DD}≥3V)	0.92µs (V_{DD}≥4.5V)	3.84µs (V_{DD}≥2.2V)
	Supply voltage	3 to 6V	4.5 to 6V	2.2 to 6V
	Current dissipation	2.5mA typ.	4mA typ.	2.5mA typ.
Oscillation	Resonator	RC (850kHz,400kHz typ.) ceramic (400k,800k,1MHz, 4MHz)	ceramic 4MHz	RC (400kHz typ.) ceramic (400k, 800k, 1MHz, 4MHz)
	predivider option	1/1 ,1/3, 1/4	1/1	1/1, 1/3, 1/4
Other	Package	DIP18, MFP18	DIP18, MFP18	DIP18, MFP18

(Note) Information on the resonator and oscillation circuit constants will be presented as soon as the recommended circuit is determined.

Pin Assignment

LC6527N/F/L
LC6528N/F/L



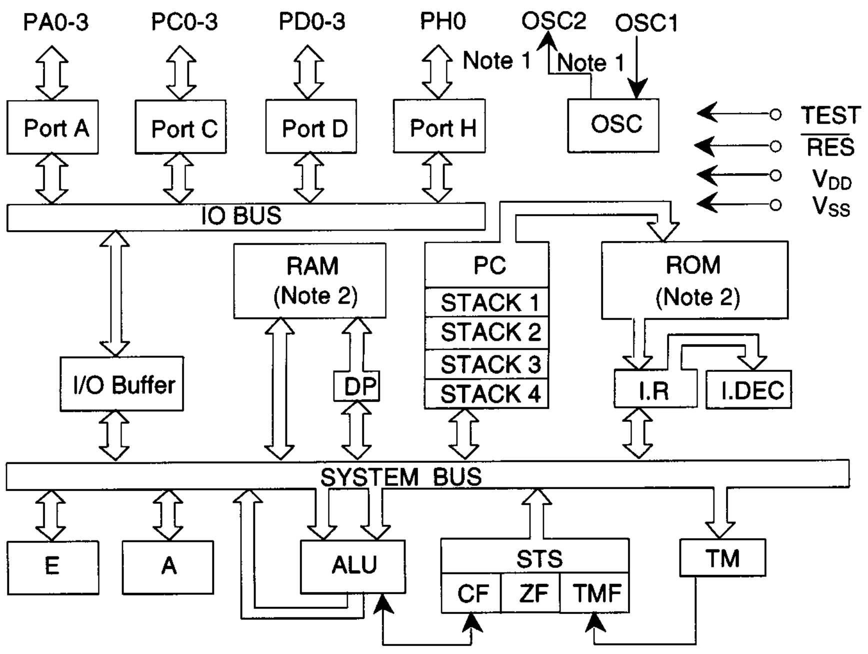
Common to DIP • MFP **Top view**

Pin Name

OSC1, OSC2 :	C, R or ceramic resonator for OSC		PH 0 :	Input/output common port H 0
RES:	Reset		TEST :	Test
PA 0 to 3:	Input/output common port A 0 to 3			
PC 0 to 3:	Input/output common port C 0 to 3			
PD 0 to 3:	Input/output common port D 0 to 3			

System Block Diagram

LC6527N/F/L, LC6528N/F/L



Note 1. The PH0 pin or OSC2 pin is selected by the mask option.
Note 2. LC6527N/F/L ROM : 1024 bytes RAM : 64 words
LC6528N/F/L ROM : 512 bytes RAM : 32 words

Development Support Tools

The following are available to support the program development for the LC6527, LC6528.

(1) User's Manual
"LC6527, LC6528 User's Manual" No. 24-6016 ('86.10.1.)
Note : Do not use "LC6523 Series User's Manual" No. 16A-7015 and No. 16-9064.
(2) Development Tool Manual
For the EVA-800 or the EVA-850 system, refer to "EVA-800-LC6527, LC6528 Development Tool Manual".
(3) Development Tools
A. For program evaluation
1. Piggy back (LC65PG23/26)
2. 23T27 ; The pin-to-pin conversion socket for the piggy back LC65PG23/26.
B. EVA-86000 system for program development.
C. For program evaluation
microcomputer built-in EPROM (LC65E29) + conversion substrate (29T027)

Note.	For notes for program evaluation, do not fail to refer to '4-3. Notes when evaluating programs' in "LC6527, LC6528 User's Manual".

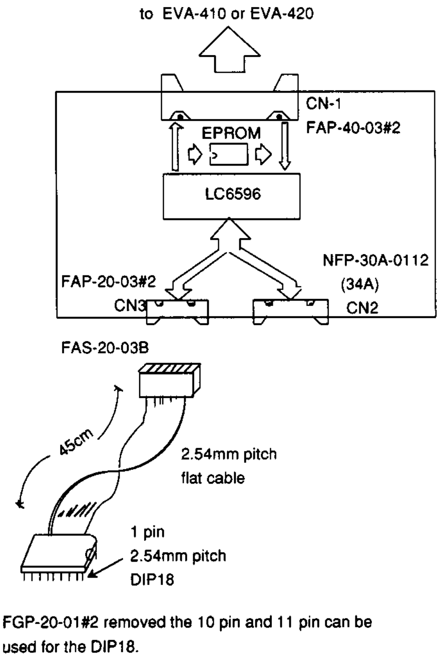


Figure 1 Evaluation kit target board (EVA-TB6523C/26C/27C/28C)

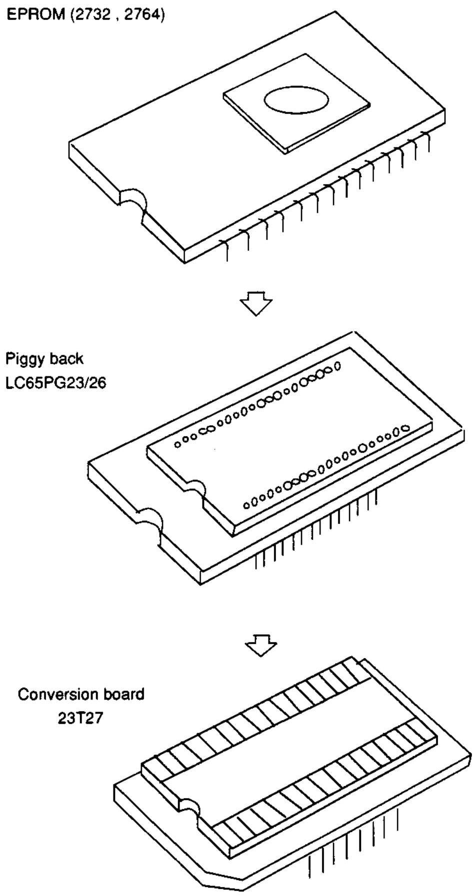
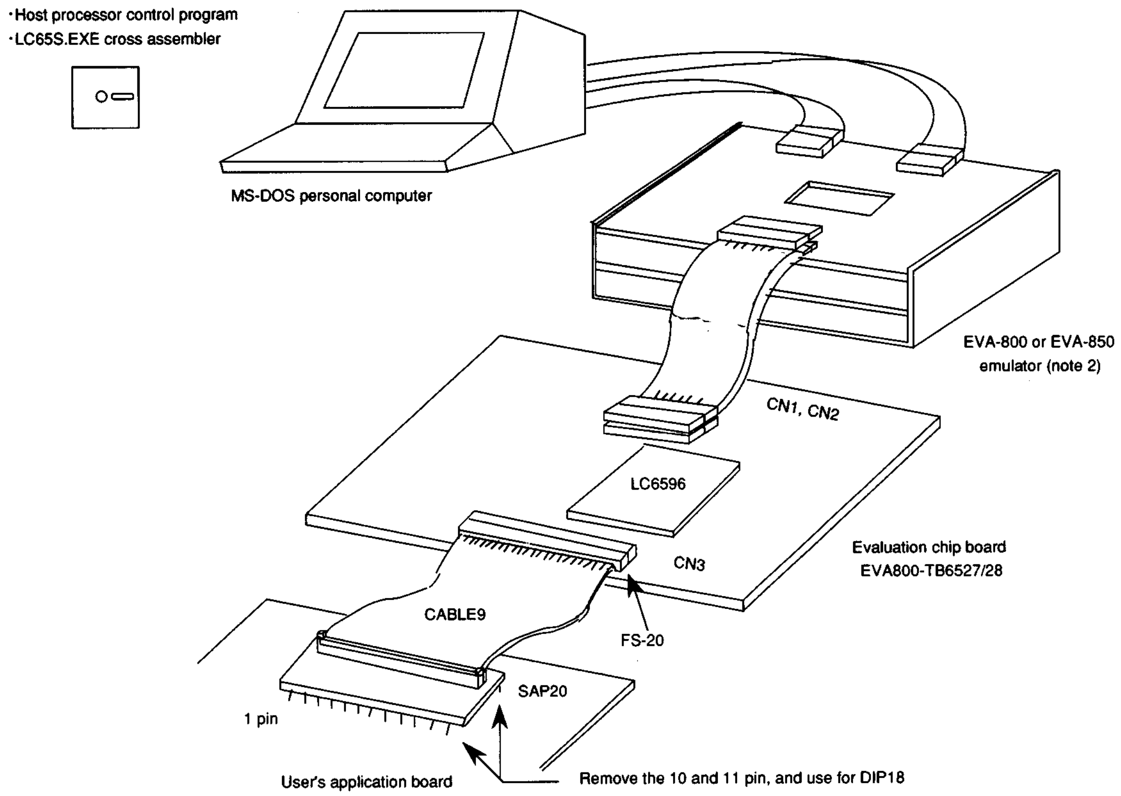


Figure 2 Program evaluation

D. For program development (EVA-800 or EVA-850 system)
1. MS-DOS for host system (Note 1)
2. Cross assembler……MS-DOS base cross assembler : <LC65S. EXE>
3. Host control program
4. Evaluation chip: LC6596
5. Emulator: EVA-800 or EVA-850 emulator and evaluation boards EVA800-TB6527/28

Appearance of Development Support System

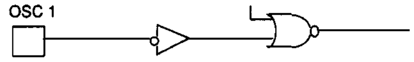
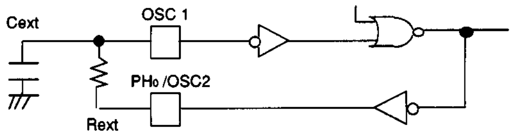
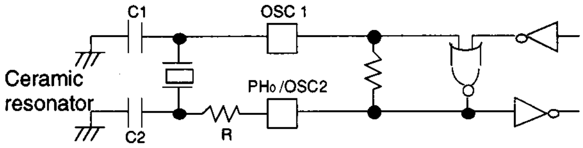


(Note 1) MS-DOS : Tradmark of Microsoft Corporation
(Note 2) The EVA-800, EVA-850 are general term for emulator. A suffix (A, B,…) is added at the end of EVA-800 and EVA-850 as they are improved to be a newer version. Do not use the EVA-800 and EVA-850 with no suffix added.

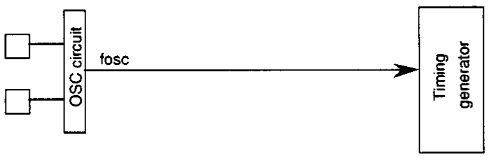
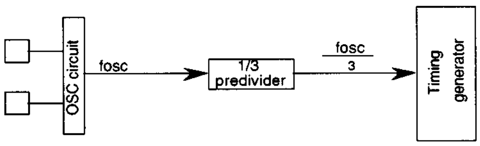
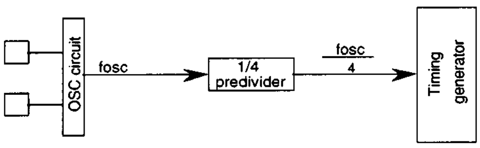
Pin Description

Pin Name	Pins	I/O	Function	Option	Reset Mode
V_{DD} V_{SS}	1 1	— —	Power supply	—	—
OSC1	1	Input	• Pin for externally connecting RC,ceramic resonator for system clock generation. • For 1-pin external clock input, the PH0/OSC2 pin is used as I/O port PH0. • For 2-pin RC OSC, 2-pin ceramic resonator OSC, the PH0/OSC2 pin is used as OSC pin OSC2.	1) 1-pin external clock input 2) 2-pin RC OSC 3) 2-pin ceramic resonator OSC 4) Predivider option 1. No predivider 2. 1/3 predivider 3. 1/4 predivider	—
PA 0 to PA 3	4	Input/output	• I/O port A0 to A3 4-bit input (IP instruction) 4-bit output (OP instruction) Single-bit decision (BP, BNP instruction) Single-bit set/reset (SPB, RPB instruction) • Standby is controlled by PA3. • The PA3 pin must be free from chattering during the HALT instruction execution cycle.	1) Open drain type output 2) With pull-up resistor 1), 2) : Specified bit by bit	• "H"output (Out put Nch transistor : OFF)
PC 0 to PC 3	4	Input/output	• I/O port C0 to C3 Same as for PA0 to PA3 (Note) • Option permits output at thereset mode to be "H" or "L". (Note) No standby control function is provided.	1) Open drain type output 2) With pull-up resistor 3) Output at reset mode:"H" 4) Output at reset mode:"L" • 1), 2): Specified bit by bit • 3), 4): Specified in a group of 4 bits	• "H" output • "L" output (Option-selectable)
PD 0 to PD 3	4	Input/output	• I/O port D0 to D3 Same as for PC0 to PC3	Same as for PC0 to PC3	Same as for PC0 to PC3
PH 0 / OSC2	1	Input/output	• I/O port H0 Same as for PA0 to PA3 (Note) • Single-bit configuration • For 2-pin OSC, this pin is used as the OSC2 pin, providing no function as I/O port. (Note) No standby control function is provided.	Same as for PA0 to PA3	Same as for PA0 to PA3
$\overline{RES}$	1	Input	• Systen reset input • For power-up reset, C is connected externally. • For reset restart, "L" level is applied for 4 clock cycles or more.		
TEST	1	Input	• LSI test pin Normally connected to V_{SS}		

Oscillator circuit option

Option Name	Circuit	Conditions , etc.
1. External clock		The PH 0 / OSC2 pin is used as port PH0.
2. 2-pin RC OSC		The PH 0 / OSC2 pin is used as OSC pin OSC2, providing no function as port.
3. Ceramic resonator OSC		The PH 0 / OSC2 pin is used as OSC pin OSC2, providing no function as port.

Predivider Option

Option Name	Circuit	Conditions , etc.
1. No predivider (1/1)		• Applicable to all of 3 OSC options. • The OSC frequency, external clock do not exceed 1444 kHz. (LC6527N, 6528N) • The OSC frequency, external clock do not exceed 4330 kHz. (LC6527F, 6528F) • The OSC frequency, external clock do not exceed 1040 kHz. (LC6527L, 6528L)
2. 1/3 predivider		• Applicatable to only 2 OSC options of external clock, ceramic resonator OSC. • The OSC frequency, external clock do not exceed 4330 kHz.
3. 1/4 predivider		• Applicatable to only 2 OSC options of external clock, ceramic resonator OSC. • The OSC frequency, external clock do not exceed 4330 kHz.

Note : The OSC option and predivider option are summarized below. Full care must be exercised.

Table of OSC, predivider Option of LC6527N/28N, 27F/28F and 27L/28L

LC6527N, LC6528N

Circuit configuration	Frequency	Predivide option (Cycle time)	V_{DD} range	Remarks
Ceramic resonator OSC	400 kHz	1/1 (10 µs)	3 to 6 V	Unusable with 1/3, 1/4 predivider
	800 kHz	1/1 (5 µs) 1/3 (15 µs) 1/4 (20 µs)	4 to 6 V 4 to 6 V 4 to 6 V	
	1 MHz	1/1 (4 µs) 1/3 (12 µs) 1/4 (16 µs)	4 to 6 V 4 to 6 V 4 to 6 V	
	4 MHz	1/3 (3 µs) 1/4 (4 µs)	4 to 6 V 4 to 6 V	Unusable with 1/1 predivider
1-pin external clock	200 k to 667 kHz 600 k to 2000 kHz 800 k to 2667 kHz 200 k to 1444 kHz 600 k to 4330 kHz 800 k to 4330 kHz	1/1 (20 to 6 µs) 1/3 (20 to 6 µs) 1/4 (20 to 6 µs) 1/1 (20 to 2.77 µs) 1/3 (20 to 2.77 µs) 1/4 (20 to 3.70 µs)	3 to 6 V 3 to 6 V 3 to 6 V 4 to 6 V 4 to 6 V 4 to 6 V	
External clock by 2-pin RC OSC circuit	Same as above			
2-pin RC	Used with 1/1predivider,recommended constants. If used with other than recommended constants, the frequency, predivider option, V_{DD} range must be the same as for 1-pin external clock.		3 to 6 V 4 to 6 V	
External clock input to the ceramic oscillation circuit	The ceramic oscillation circuit cannot be driven by external clock. To drive the circuit with external clock, select the external clock option or the 2-pin RC option.			

LC6527F, LC6528F

Circuit configuration	Frequency	Predivider option	V_{DD} Range (Cycle time)	Remarks
Ceramic resonator OSC	4 MHz	1/1 (1 µs)	4.5 to 6 V	
1-pin external clock	200 k to 4330 kHz	1/1 (20 to 0.92 µs)	4.5 to 6 V	
External clock input to the ceramic oscillation circuit	The ceramic oscillation circuit cannot be driven by external clock. To drive the circuit with external clock, select the external clock option.			

LC6527L, LC6528L

Circuit configuration	Frequency	Predivider option (Cycle Time)	V_{DD} range	Remarks
Ceramic resonator OSC	400 kHz	1/1 (10 µs)	2.2 to 6 V	Unusable with 1/3, 1/4 predivider
	800 kHz	1/1 (5 µs) 1/3 (15 µs) 1/4 (20 µs)	2.2 to 6 V 2.2 to 6 V 2.2 to 6 V	
	1 MHz	1/1 (4 µs) 1/3 (12 µs) 1/4 (16 µs)	2.2 to 6 V 2.2 to 6 V 2.2 to 6 V	
	4 MHz	1/4 (4 µs)	2.2 to 6 V	Unusable with 1/1, 1/3 predivider
1-pin external clock	200 k to 1040 kHz 600 k to 3120 kHz 800 k to 4160 kHz	1/1 (20 to 3.84 µs) 1/3 (20 to 3.84 µs) 1/4 (20 to 3.84 µs)	2.2 to 6 V 2.2 to 6 V 2.2 to 6 V	
External clock by 2-pin RC OSC circuit	Same as above			
2-pin RC	Used with 1/1predivider, recommended constants. If used with other than recommended constants, the frequency, predivider option, V_{DD} range must be the same as for 1-pin external clock.		2.2 to 6 V	
External clock input to the ceramic oscillation circuit	The ceramic oscillation circuit cannot be driven by external clock. To drive the circuit with external clock, select the external clock option or the 2-pin RC option.			

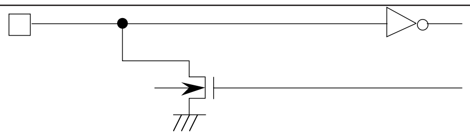
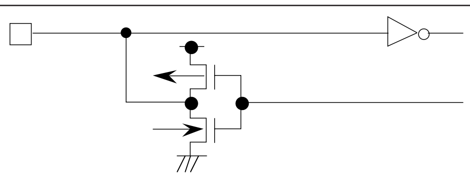
Option of ports C, D Output Level at the Reset Mode

For input/output common ports C, D either of the following two output levels may be selected in a group of 4 bits during reset by option.

Option Name	Conditions , etc.
1. Output at the reset mode : "H" level	All of 4 bits of ports C, D
2. Output at the reset mode : "L" level	All of 4 bits of ports C, D

Option of Port Output Configuration

For each input/output common port, either of the following two output configurations may be selected by option.

Option Name	Circuit	Conditions , etc.
1. Open drain output		• Unapplicable to port PH0/OSC2 when 2-pin RC OSC or ceramic resonator OSC is selected.
2. Output with pull-up resistor		

Specifications

LC6527N, LC6528N

1. Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Pins	Ratings	Unit
Maximum supply voltage	V_{DD} max		V_{DD}	–0.3 to +7.0	V
Output voltage	V_O		OSC2	Allowable up to voltage generated	V
Input voltage	V_I(1)		OSC1 (*1)	–0.3 to V_{DD}+0.3	V
	V_I(2)		TEST, $\overline{RES}$	–0.3 to V_{DD}+0.3	V
Input/output voltage	V_{IO}(1)		Port of OD type	–0.3 to +15	V
	V_{IO}(2)		Port of PU type	–0.3 to V_{DD}+0.3	V
Peak output current	I_{OP}		I/O port	–2 to +20	mA
Average output current	I_{OA}	Per pin over the period of 100 ms	I/O Port	–2 to +20	mA
	ΣI_{OA}(1)	Total current of PA0 to PA3, (*2)	PA0 to PA3	–6 to +40	mA
	ΣI_{OA}(2)	Total current of PC0 to PC3, PD0 to PD3, PH0 (*2)	PC0 to PC3 PH0 PD0 to PD3	–14 to +90	mA
Allowable power dissipation	Pd max (1)	Ta = –40 to +85°C (DIP package)		250	mW
	Pd max (2)	Ta = –40 to +85°C (MFP package)		150	mW
Operating temperature	Topr			–40 to +85	°C
Storage temperature	Tstg			–55 to +125	°C

2. Allowable Operating Conditions at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 3.0 to 6.0 V

Parameter	Symbol	Conditions		Pins	Ratings			Unit
			V_{DD} [V]		min	typ	max	
Operating supply voltage	V_{DD}			V_{DD}	3.0		6.0	V
Standby supply voltage	V_{ST}	RAM, register hold (*3)		V_{DD}	1.8		6.0	V
"H"-level input voltage	V_{IH}(1)	Output Nch transistor OFF		Port of ODtype (except H0)	0.7V_{DD}		13.5	V
	V_{IH}(2)	Output Nch transistor OFF		Port of PU type (except H0)	0.7V_{DD}		V_{DD}	V
	V_{IH}(3)	Output Nch transistor OFF		H0 of OD type	0.8V_{DD}		13.5	V
	V_{IH}(4)	Output Nch transistor OFF		H0 of PU type	0.8V_{DD}		V_{DD}	V
	V_{IH}(5)			$\overline{RES}$	0.8V_{DD}		V_{DD}	V
	V_{IH}(6)	External clock mode		OSC1	0.8V_{DD}		V_{DD}	V
"L"-level input voltage	V_{IL}(1)	Output Nch transistor OFF	V_{DD} = 4 to 6	Port	V_{SS}		0.3V_{DD}	V
	V_{IL}(2)	Output Nch transistor OFF	V_{DD} = 3 to 6	Port	V_{SS}		0.25V_{DD}	V
	V_{IL}(3)	External clock mode	V_{DD} = 4 to 6	OSC1	V_{SS}		0.25V_{DD}	V

Parameter	Symbol	Conditions		Pins	Ratings			Unit
			V_{DD} [V]		min	typ	max	
"L"-level input voltage	$V_{IL}(4)$	External clock mode	V_{DD} = 3 to 6	OSC1	V_{SS}		$0.2V_{DD}$	V
	$V_{IL}(5)$		V_{DD} = 4 to 6	TEST	V_{SS}		$0.3V_{DD}$	V
	$V_{IL}(6)$		V_{DD} = 3 to 6	TEST	V_{SS}		$0.25V_{DD}$	V
	$V_{IL}(7)$		V_{DD} = 4 to 6	$\overline{RES}$	V_{SS}		$0.25V_{DD}$	V
	$V_{IL}(8)$		V_{DD} = 3 to 6	$\overline{RES}$	V_{SS}		$0.2V_{DD}$	V
Operating frequency (cycle time)	fop (tCYC)	When the 1/3 or 1/4 predivider option is selected, clock must not exceed 4.33 MHz.	V_{DD} = 4 to 6		200 (20) 200 (20)		1444 (2.77) 667 (6.0)	kHz (µs) kHz (µs)
External clock conditions Frequency	text	Figure 1. When clock exceeds 1.444 MHz, the 1/3 or 1/4 pre-divider option is selected.	V_{DD} = 4 to 6 3 to 6	OSC1	200 200		4330 2667	kHz kHz
Pulse width	textH, textL		V_{DD} = 4 to 6 3 to 6	OSC1	69 180			ns ns
Rise/Fall time	textR, textF		V_{DD} = 4 to 6 3 to 6	OSC1			50 100	ns ns
Oscillation guaranty constants 2-pin RC oscillation	Cext Cext	Figure 2 Figure 2	V_{DD} = 3 to 6 V_{DD} = 4 to 6	OSC1, OSC2 OSC1, OSC2		220 ±5% 220 ±5%		pF pF
	Rext Rext	Figure 2 Figure 2	V_{DD} = 3 to 6 V_{DD} = 4 to 6	OSC1, OSC2 OSC1, OSC2		12 ±1% 4.7 ±1%		kΩ kΩ
Ceramic resonator OSC		Figure 3				Table 1		

3. Electrical Characteristics at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 3.0 V to 6.0 V

Parameter	Symbol	Conditions	Pins	Ratings			Unit
				min	typ	max	
"H"-level input current	$I_{IH}(1)$	Output Nch transistor OFF (including OFF leak current of Nch transistor) V_{IN} = +13.5 V	Port of OD type			+5.0	µA
	$I_{IH}(2)$	External clock mode, $V_{IN} = V_{DD}$	OSC1			+1.0	µA
"L"-level input current	$I_{IL}(1)$	Output Nch transistor OFF $V_{IN} = V_{SS}$	Port of OD type	–1.0			µA
	$I_{IL}(2)$	Output Nch transistor OFF $V_{IN} = V_{SS}$	Port of PU type	–1.3	–0.35		mA
	$I_{IL}(3)$	$V_{IN} = V_{SS}$	$\overline{RES}$	–45	–10		µA
	$I_{IL}(4)$	External clock mode, $V_{IN} = V_{SS}$	OSC1	–1.0			µA
"H"-level output voltage	$V_{OH}(1)$	I_{OH} = –50 µA V_{DD} = 4.0 to 6.0 V	Port of PU type	V_{DD}–1.2			V
	$V_{OH}(2)$	I_{OH} = –10 µA	Port of PU type	V_{DD}–0.5			V

Parameter	Symbol	Conditions	Pins	Ratings			Unit
				min	typ	max	
"L"-level output voltage	$V_{OL}(1)$	I_{OL} = 10 mA, V_{DD} = 4.0 to 6.0 V	Port			1.5	V
	$V_{OL}(2)$	I_{OL} = 1.8 mA, I_{OL} of each port: 1mA or less	Port			0.4	V
Hysteresis voltage	V_{HIS}		$\overline{RES}$, OSC1 of schmitt type (*4)		$0.1V_{DD}$		V
Current drain 2-pin RC oscillation	$I_{DDOP}(1)$	Output Nch transistor OFF at operating, Port = V_{DD} Figure 2 fosc = 850 kHz (typ) V_{DD} = 4 to 6 V	V_{DD}		1.0	2.5	mA
	$I_{DDOP}(2)$	Figure 2 fosc = 400 kHz (typ)	V_{DD}		0.8	2.5	mA
Ceramic resonator oscillation	$I_{DDOP}(3)$	Figure 3 4 MHz, 1/3 predivider V_{DD} = 4 to 6 V	V_{DD}		1.2	3	mA
	$I_{DDOP}(4)$	Figure 3 4 MHz, 1/4 predivider V_{DD} = 4 to 6 V	V_{DD}		1.2	2.5	mA
	$I_{DDOP}(5)$	Figure 3 400 kHz	V_{DD}		0.5	2	mA
	$I_{DDOP}(6)$	Figure 3 800 kHz V_{DD} = 4 to 6 V	V_{DD}		1.0	2.5	mA
External clock	$I_{DDOP}(7)$	200 kHz to 667 kHz, 1/1 predivider 600 kHz to 2000 kHz, 1/3 predivider 800kHz to 2667kHz, 1/4 predivider	V_{DD}		1.0	2.5	mA
	$I_{DDOP}(8)$	200 kHz to 1444 kHz, 1/1 predivider 600 kHz to 4330 kHz, 1/3 predivider 800 kHz to 4330 kHz, 1/4 predivider, V_{DD} = 4 to 6 V	V_{DD}		1.2	3	mA
Standby mode	$I_{DD}st$	Output Nch transistor OFF V_{DD} = 6 V Port = V_{DD} V_{DD} = 3 V	V_{DD} V_{DD}		0.05 0.025	10 5	µA
Oscillation characteristics Ceramic OSC Frequency	fCFOSC (*5)	Figure 3 fo = 400 kHz Figure 3 fo = 800 kHz, V_{DD} = 4 to 6 V Figure 3 fo = 1 MHz V_{DD} = 4 to 6 V Figure 3 fo = 4 MHz, 1/3 predivider 1/4 predivider V_{DD} = 4 to 6 V	OSC1, OSC2 OSC1, OSC2 OSC1, OSC2 OSC1, OSC2	384 768 960 3840	400 800 1000 4000	416 832 1040 4160	kHz kHz kHz kHz
Stable time	tCFS	Figure 4 fo = 400 kHz Figure 4 fo = 800 kHz, 1 MHz, 4 MHz, 1/3 predivider, 1/4 predivider V_{DD} = 4 to 6 V				10 10	ms ms
2-pin RC oscillation Frequency	fMOSC	Figure 2 Cext = 220 pF ± 5% Figure 2 Rext = 4.7 kΩ ±1% V_{DD} = 4 to 6 V	OSC1, OSC2	646	850	1117	kHz
		Figure 2 Cext = 220 pF ±5% Figure 2 Rext = 12 kΩ ±1% V_{DD} = 3 to 6 V	OSC1, OSC2	304	400	580	kHz

Parameter	Symbol	Conditions	Pins	Ratings			Unit
				min	typ	max	
Pull-up resistance I/O port pull-up resistance	RPP	V_{DD}=5V	Port of PU type		14		kΩ
External reset characteristics Reset time	tRST				See Figure 5.		
Pin capacitance	Cp	f = 1 MHz Other than pins to be tested, $V_{IN} = V_{SS}$			10		pF

(*1) When oscillated internally under the oscillating conditions in Figure 3, up to the oscillation amplitude generated is allowable.
(*2) Average over the period of 100 ms.
(*3) Operating supply voltage V_{DD} must be held until the standby mode is entered after the execution of the HALT instruction. The PA3 pin must be free from chattering during the HALT instruction execution cycle.
(*4) The OSC1 pin can be schmitt-triggered when the 2-pin RC oscillation option or external clock oscillation option has been selected.
(*5) fCFOSC: oscillation frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic resonator mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.

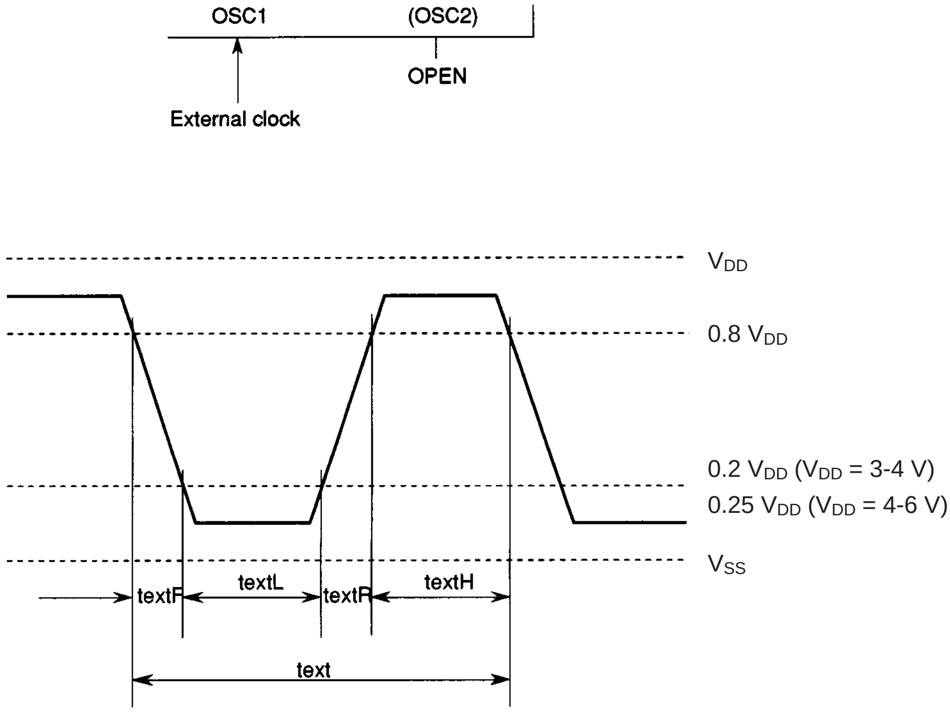


Figure 1 External Clock Input Waveform

* External clock can be used at selecting 2-pin RC option or 1-pin external clock option, and cannot be used at ceramic resonator oscillation.

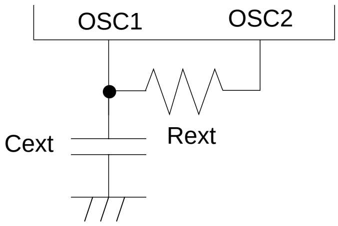


Figure 2 2-pin RC Oscillation Circuit

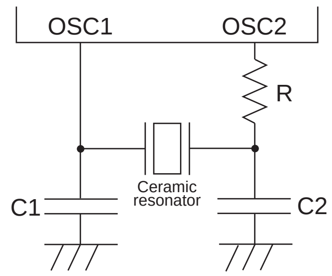


Figure 3 Ceramic Resonator Oscillation Circuit

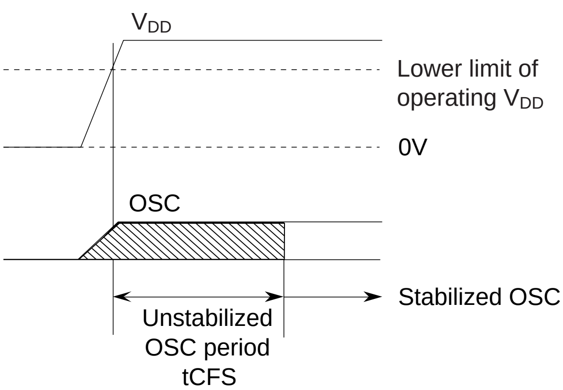


Figure 4 Oscillation Stabilizing Period

Table 1 Constants Guaranteed for Ceramic Resonator OSC

4MHz (Murata)	C1	33 pF ±10%
CSA4.00MG	C2	33 pF ±10%
CST4.00MGW (built-in C)	R	0 Ω
4 MHz (Kyocera)	C1	33 pF ±10 %
KBR4.0MSA	C2	33 pF ±10%
KBR4.0MKS (built-in C)	R	0 Ω
1 MHz (Murata)	C1	100 pF±10%
CSB1000J	C2	100pF±10%
	R	2.2 kΩ
1 MHz (Kyocera)	C1	100 pF ±10%
KBR1000F	C2	100 pF ±10%
	R	0 Ω
800 kHz (Murata)	C1	100 pF ±10%
CSB800J	C2	100 pF ±10%
	R	2.2 kΩ
800 kHz (Kyocera)	C1	100 pF±10%
KBR800F	C2	100 pF±10%
	R	0 Ω
400 kHz (Murata)	C1	220 pF ±10%
CSB400P	C2	220 pF ±10%
	R	2.2 kΩ
400 kHz (Kyocera)	C1	330 pF ±10%
KBR400BK	C2	330 pF ±10%
	R	0 Ω

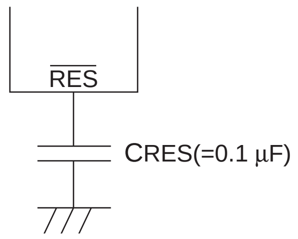


Figure 5 Reset Circuit

(Note) When the rise time of the power supply is 0, the reset time becomes 10 ms to 100 ms at C_{RES} = 0.1 µF. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10 ms or more.

RC Oscillation Characteristics of the LC6527N, LC6528N

Figure 6 shows the RC oscillation characteristics of the LC6527N, 6528N. For the variation range of RC OSC frequency of the LC6527N, LC6528N, the following are guaranteed at the external constants only shown below.

1) V_{DD} = 3.0 V to 6.0 V, Ta = –40°C to +85°C
External constants Cext = 220 pF
Rext = 12 kΩ
304 kHz ≤ fMOSC ≤ 580 kHz

2) V_{DD} = 4.0 V to 6.0 V, Ta = –40°C to +85°C
Cext = 220 pF
Rext = 4.7 kΩ
646 kHz ≤ fMOSC ≤ 1117 kHz

If any other constants than specified above are used, the range of Rext = 3 kΩ to 20 kΩ, Cext = 150 pF to 390 pF must be observed. (See Figure 6.)

(*6) : The oscillation frequency at V_{DD} = 5.0 V, Ta = +25°C must be in the range of 350 kHz to 750 kHz.
(*7) : The oscillation frequency at V_{DD} = 4.0 to 6.0 V, Ta = –40°C to +85°C and V_{DD} = 3.0 V to 6.0 V, Ta = –40°C to 85°C must be within the operation clock frequency range.

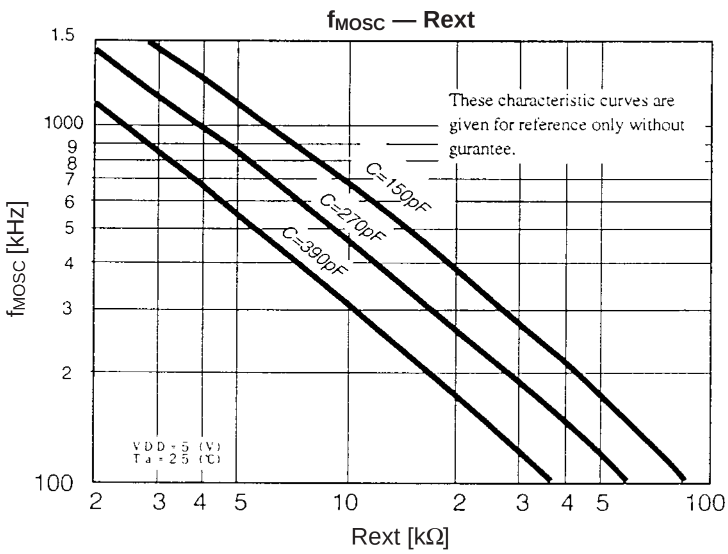


Figure 6 RC Oscillation Frequency Data (typ)

LC6527F, LC6528F

1. Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Pin	Ratings	Unit
Maximum supply voltage	V_{DD} max		V_{DD}	–0.3 to +7.0	V
Output voltage	V_O		OSC2	Allowable up to voltage generated	V
Input voltage	V_I (1)		OSC1 (*1)	–0.3 to V_{DD}+0.3	V
	V_I (2)		TEST, $\overline{RES}$	–0.3 to V_{DD}+0.3	V
Input/output voltage	V_{IO} (1)		Port of OD type	–0.3 to +15	V
	V_{IO} (2)		Port of PU type	–0.3 to V_{DD}+0.3	V
Peak output current	I_{OP}		I/O Port	–2 to +20	mA
Average output current	I_{OA}	Per pin over the period of 100 ms	I/O Port	–2 to +20	mA
	ΣI_{OA} (1)	Total current of PA0 to PA3, (*2)	PA0 to PA3	–6 to +40	mA
	ΣI_{OA} (2)	Total current of PC0 to PC3, PD0 to PD3, PH0 (*2)	PC0 to PC3 PH0 PD0 to PD3	–14 to +90	mA
Allowable power dissipation	Pd max (1)	Ta = –40 to +85°C (DIP package)		250	mW
	Pd max (2)	Ta = –40 to +85°C (MFP package)		150	mW
Operating temperature	Topr			–40 to +85	°C
Storage temperature	Tstg			–55 to +125	°C

2. Allowable Operating Conditions at Ta = –40 to +85°C, V_{SS} = 0 V, V_{DD} = 4.5 to 6.0 V

Parameter	Symbol	Conditions	Pin	Ratings			Unit
				min	typ	max	
Operating supply voltage	V_{DD}		V_{DD}	4.5		6.0	V
Standby supply voltage	V_{ST}	RAM, register hold (*3)	V_{DD}	1.8		6.0	V
"H"-level input voltage	V_{IH}(1)	Output Nch transistor OFF	Port of OD type (except H0)	0.7V_{DD}		13.5	V
	V_{IH}(2)	Output Nch transistor OFF	Port of PU type (except H0)	0.7V_{DD}		V_{DD}	V
	V_{IH}(3)	Output Nch transistor OFF	H0 of OD type	0.8V_{DD}		13.5	V
	V_{IH}(4)	Output Nch transistor OFF	H0 of PU type	0.8V_{DD}		V_{DD}	V
	V_{IH}(5)		$\overline{RES}$	0.8V_{DD}		V_{DD}	V
	V_{IH}(6)	External clock mode	OSC1	0.8V_{DD}		V_{DD}	V

Parameter	Symbol	Conditions	Pin	Ratings			Unit
				min	typ	max	
"L"-level input voltage	$V_{IL}(1)$	Output Nch transistor OFF	Port	V_{SS}		$0.3V_{DD}$	V
	$V_{IL}(2)$	External clock mode	OSC1	V_{SS}		$0.25V_{DD}$	V
	$V_{IL}(3)$		TEST	V_{SS}		$0.3V_{DD}$	V
	$V_{IL}(4)$		$\overline{RES}$	V_{SS}		$0.25V_{DD}$	V
Operating frequency (Cycle time)	fOP (tCYC)			200 (20)		4330 (0.92)	kHz (µs)
External clock conditions Frequency	text	Figure 1	OSC1	200		4330	kHz
Pulse width	textH, textL	Figure 1	OSC1	69			ns
Rise/fall time	textR, textF	Figure 1	OSC1			50	ns
Oscillation guaranteed constants Ceramic resonator OSC		Figure 2		See Table 1.			

3. Electrical Characteristics at Ta = –40°C to +85°C, V_{SS} = 0 V, V_{DD} = 4.5 to 6.0 V

Parameter	Symbol	Conditions	Pin	Ratings			Unit
				min	typ	max	
"H"-level input current	$I_{IH}(1)$	Output Nch transistorOFF (including OFF leak current of Nch transistor) V_{IN} = +13.5 V	Port of OD type			+5.0	µA
	$I_{IH}(2)$	External clock mode, V_{IN} = V_{DD}	OSC1			+1.0	µA
"L"-level input current	$I_{IL}(1)$	Output Nch transistor OFF V_{IN} = V_{SS}	Port of OD type	–1.0			µA
	$I_{IL}(2)$	Output Nch transistor OFF V_{IN} = V_{SS}	Port of PU type	–1.3	–0.35		mA
	$I_{IL}(3)$	V_{IN} = V_{SS}	$\overline{RES}$	–45	–10		µA
	$I_{IL}(4)$	External clock mode, V_{IN} = V_{SS}	OSC1	–1.0			µA
"H"-level output voltage	$V_{OH}(1)$	I_{OH} = –50 µA	Port of PU type	V_{DD}–1.2			V
	$V_{OH}(2)$	I_{OH} = –10 µA	Port of PU type	V_{DD}–0.5			V
"L"-level output voltage	$V_{OL}(1)$	I_{OL} = 10 mA	Port			1.5	V
	$V_{OL}(2)$	I_{OL} = 1.8 mA, I_{OL} of each port : 1 mA or less	Port			0.4	V
Hysteresis voltage	V_{HIS}		$\overline{RES}$, OSC1 of schmitt type (*4)		$0.1V_{DD}$		V

Parameter	Symbol	Conditions	Pin	Ratings			Unit
				min	typ	max	
Current drain Ceramic resonator OSC	$I_{DDOP}(1)$	Figure 2 4 MHz *1	V_{DD}		1.5	3.5	mA
External clock	$I_{DDOP}(2)$	200 kHz to 4330 kHz *1 *1 Output Nch transistor OFF at Operating mode Port = V_{DD}	V_{DD}		1.5	3.5	mA
Standby mode	$I_{DD}st$	Output Nch transistor OFF Port = V_{DD} V_{DD} = 6 V	V_{DD}		0.05	10	µA
		V_{DD} = 3 V	V_{DD}		0.025	5	µA
Oscillation characteristics Ceramic resonator OSC Frequency	fCFOSC	Figure 2 fo = 4 MHz (*5)	OSC1, OSC2	3840	4000	4160	kHz
Stable time	tCFS	Figure 3 fo = 4 MHz				10	ms
Pull-up resistance I/O port pull-up resistance	RPP	V_{DD} = 5 V	Port of PU type		14		kΩ
External reset characteristics Reset time	tRST				See Figure 4		
Pin capacitance	Cp	f = 1 MHz, other than pins to be tested, V_{IN} = V_{SS}			10		pF

(*1) When oscillated internally under the oscillating conditions in Fig.2, up to the oscillation amplitude generated is allowable.
(*2) Average over the period of 100 ms.
(*3) Operating supply voltage V_{DD} must be held until the standby mode is entered after the execution of the HALT instruction. The PA3 pin must be free from chattering during the HALT instruction execution cycle.
(*4) The OSC1 pin can be schmitt-triggered when the external clock oscillation option has been selected.
(*5) fCFOSC : Oscillatable frequency.

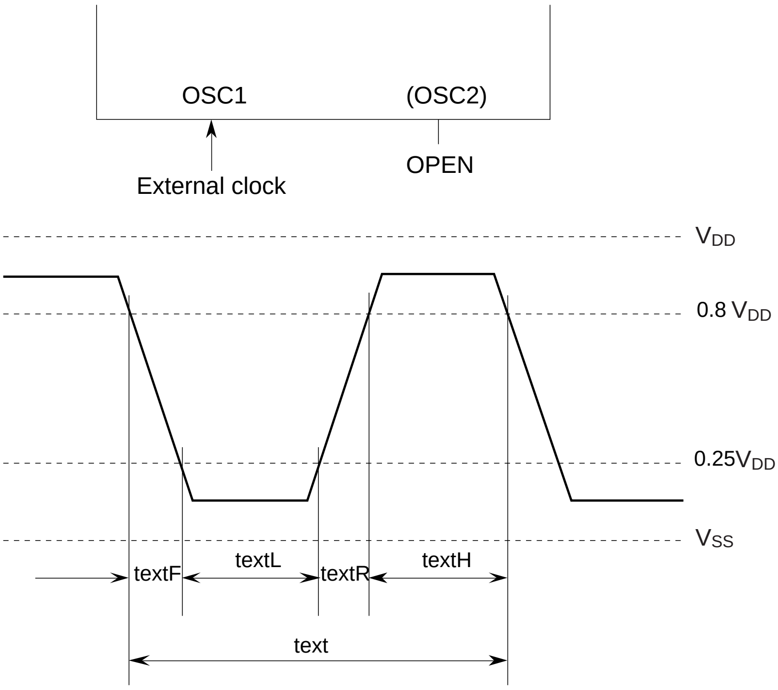


Figure 1 External Clock Input Waveform

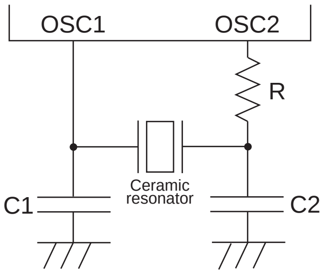


Figure 2 Ceramic resonator OSC circuit

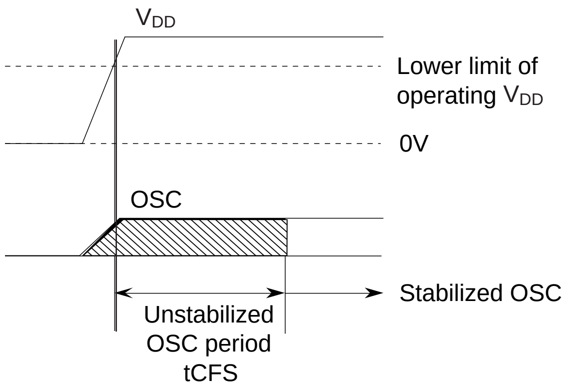


Figure 3 OSC Stabilizing Period

Table 1 Constants Guaranteed for Ceramic Resonator OSC

4MHz (Murata)	C1	33 pF ± 10%
CSA4.00MG	C2	33 pF ± 10%
CST4.00MGW (built-in C)	R	0 Ω
4MHz (Kyocera)	C1	33 pF ± 10%
KBR4.0MSA	C2	33 pF ± 10%
KBR4.0MKS (built-in C)	R	0 Ω

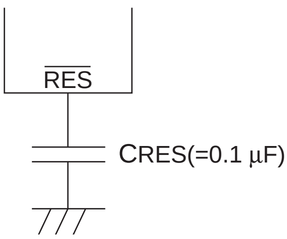


Figure 4 Reset Circuit

(Note) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at C_{RES} = 0.1 µF. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10ms or more.

LC6527L, LC6528L

1. Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Pin	Ratings	Unit
Maximum V_{DD} max supply voltage	V_{DD} max		V_{DD}	–0.3 to +7.0	V
Output voltage	V_O		OSC2	Allowable up to voltage generated	V
Input voltage	$V_I(1)$		OSC1 (*1)	–0.3 to V_{DD}+0.3	V
	$V_I(2)$		TEST, $\overline{RES}$	–0.3 to V_{DD}+0.3	V
Input/output voltage	$V_{IO}(1)$		Port of OD type	–0.3 to +15	V
	$V_{IO}(2)$		Port of PU type	–0.3 to V_{DD}+0.3	V
Peak output current	I_{OP}		I/O Port	–2 to +20	mA
Average output current	I_{OA}	Per pin over the period of 100 ms	I/O Port	–2 to +20	mA
	$\Sigma I_{OA}(1)$	Total current of PA0 to PA3, (*2)	PA0 to PA3	–6 to +40	mA
	$\Sigma I_{OA}(2)$	Total current of PC0 to PC3, PD0 to PD3, PH0 (*2)	PC0 to PC3 PH0 PD0 to PD3	–14 to +90	mA
Allowable power dissipation	Pd max(1)	Ta = –40 to +85°C (DIP package)		250	mW
	Pd max(2)	Ta = –40 to +85°C (MFP package)		150	mW
Operating temperature	Topr			–40 to +85	°C
Storage temperature	Tstg			–55 to +125	°C

2. Allowable Operating Conditions at Ta = –40°C to 85°C, V_{SS} = 0 V, V_{DD} = 2.2 to 6.0 V

Parameter	Symbol	Conditions	Pin	Ratings			Unit
				min	typ	max	
Operating supply voltage	V_{DD}		V_{DD}	2.2		6.0	V
Standby supply voltage	V_{ST}	RAM, register hold (*3)	V_{DD}	1.8		6.0	V
"H"-level input voltage	$V_{IH}(1)$	Output Nch transistor OFF	Port of OD type (except H0)	0.7V_{DD}		13.5	V
	$V_{IH}(2)$	Output Nch transistor OFF	Port of PU type (except H0)	0.7V_{DD}		V_{DD}	V
	$V_{IH}(3)$	Output Nch transistor OFF	H0 of OD type	0.8V_{DD}		13.5	V
	$V_{IH}(4)$	Output Nch transistor OFF	H0 of PU type	0.8V_{DD}		V_{DD}	V
	$V_{IH}(5)$		$\overline{RES}$	0.8V_{DD}		V_{DD}	V
	$V_{IH}(6)$	External clock	OSC1	0.8V_{DD}		V_{DD}	V
"L"-level input voltage	$V_{IL}(1)$	Output Nch transistor OFF	Port	V_{SS}		0.2V_{DD}	V
	$V_{IL}(2)$	External clock	OSC1	V_{SS}		0.15V_{DD}	V
	$V_{IL}(3)$		TEST	V_{SS}		0.2V_{DD}	V
	$V_{IL}(4)$		$\overline{RES}$	V_{SS}		0.15V_{DD}	V

Parameter	Symbol	Conditions	Pin	Ratings min	Ratings typ	Ratings max	Unit
Operating frequency (cycle time)	fOP (tCYC)	When the 1/3 or 1/4 predivider option is selected, clock must not exceed 4.16 MHz.		200 (20)		1040 (3.84)	kHz (µs)
External Clock conditions							
Frequency	text	Figure 1 When clock exceeds 1.040 MHz, the 1/3 or 1/4 predivider option is selected.	OSC1	200		4160	kHz
Pulse width	textH, textL		OSC1	120			ns
Rise/fall time	textR, textF		OSC1			100	ns
Oscillation guaranteed constants 2-pin RC oscillation	Cext	Figure 2	OSC1, OSC2	220 ± 5%			pF
	Rext			12 ± 1%			kΩ
Ceramic oscillation		Figure 3		See Table 1.			

3. Electrical Characteristics at Ta = –40°C to +85°C, V_{SS} = 0 V, V_{DD} = 2.2 to 6.0 V

Parameter	Symbol	Conditions	Pin	Ratings min	Ratings typ	Ratings max	Unit
"H"-level input current	$I_{IH}(1)$	Output Nch transistor OFF (including OFF leak current of Nch transistor) V_{IN} = +13.5 V	Port of OD type			+5.0	µA
	$I_{IH}(2)$	External clock mode, $V_{IN} = V_{DD}$	OSC1			+1.0	µA
"L"-level input current	$I_{IL}(1)$	Output Nch transistor OFF $V_{IN} = V_{SS}$	Port of OD type	–1.0			µA
	$I_{IL}(2)$	Output Nch transistor OFF $V_{IN} = V_{SS}$	Port of PU type	–1.3	–0.35		mA
	$I_{IL}(3)$	$V_{IN} = V_{SS}$	$\overline{RES}$	–45	–10		µA
	$I_{IL}(4)$	External clock mode, $V_{IN} = V_{SS}$	OSC1	–1.0			µA
"H"-level output voltage	V_{OH}	I_{OH} = –10 µA	Port of PU type	V_{DD}–0.5			V
"L"-level output voltage	$V_{OL}(1)$	I_{OL} = 3 mA	Port			1.5	V
	$V_{OL}(2)$	I_{OL} = 1 mA, I_{OL} of each port: 1 mA or less	Port			0.4	V
Hysteresis voltage	V_{HIS}		$\overline{RES}$, OSC1 of Schmitt type (*4)		0.1V_{DD}		V

Parameter	Symbol	Conditions	Pin	Ratings			Unit
				min	typ	max	
Current drain 2-pin RC OSC	$I_{DDOP}(1)$	Output Nch transistor OFF at operating, Port = V_{DD} Figure 2 fOSC = 400 kHz (typ)	V_{DD}		0.8	2.5	mA
Ceramic OSC	$I_{DDOP}(2)$	Figure 3 4 MHz, 1/4 predivider	V_{DD}		1.2	2.5	mA
	$I_{DDOP}(3)$	Figure 3 4 MHz, 1/4 predivider V_{DD} = 2.2 V	V_{DD}		0.5	1	mA
	$I_{DDOP}(4)$	Figure 3 400 kHz	V_{DD}		0.5	2	mA
	$I_{DDOP}(5)$	Figure 3 800 kHz	V_{DD}		1.0	2.5	mA
External clock	$I_{DDOP}(6)$	200 kHz to 667 kHz, 1/1 predivider 600 kHz to 2000 kHz, 1/3 predivider 800 kHz to 2667 kHz, 1/4 predivider	V_{DD}		1.0	2.5	mA
Standby mode	$I_{DD}st$	Output Nch transistor OFF V_{DD} = 6 V Port = V_{DD} V_{DD} = 2.2 V	 V_{DD} V_{DD}		 0.05 0.025	 10 5	 µA µA
Oscillation characteristics Ceramic OSC Frequency	fCFOSC (*5)	Figure 3 fo = 400 kHz Figure 3 fo = 800 kHz Figure 3 fo = 1 MHz Figure 3 fo = 4 MHz, 1/4 predivider	OSC1, OSC2 OSC1, OSC2 OSC1, OSC2 OSC1, OSC2	384 768 960 3840	400 800 1000 4000	416 832 1040 4160	kHz kHz kHz kHz
Stable time	tCFS	Figure 4 fo = 400 kHz Figure 4 fo = 800 kHz, 1 MHz, 4 MHz, 1/4 predivider				10 10	ms ms
2-pin RC OSC Frequency	fMOSC	Figure 2 Cext = 220 pF ±5% Figure 2 Rext = 12 kΩ ±1%	OSC1, OSC2	281	400	580	kHz
Pull-up resistance I/O port pull-up resistance	RPP	V_{DD} = 5 V	Port of PU type		14		kΩ
External reset characteristics Reset time	tRST			See Figure 5.			
Pin capacitance	Cp	f = 1 MHz, Other than pins to be tested, V_{IN} = V_{SS}			10		pF

(*1) When oscillated internally under the oscillating conditions in Fig.3, up to the oscillation amplitude generated is allowable.
(*2) Average over the period of 100ms.
(*3) Operating supply voltage VDD must be held until the standby mode is entered after the execution of the HALT instruction. The PA3 pin must be free from chattering during the HALT instruction execution cycle.
(*4) The OSC1 pin can be schmitt-triggered when the 2-pin RC oscillation option, or external clock oscillation option has been selected.
(*5) fCFOSC : Oscillatable frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic resonator mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.

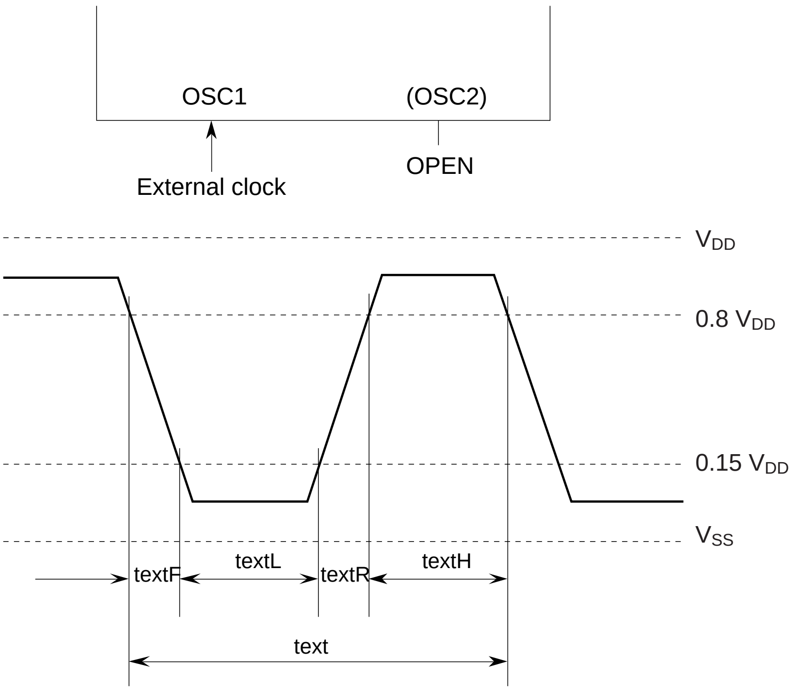


Figure 1 External Clock Input Waveform

* External clock can be used at selecting 2-pin RC option or 1-pin external clock option, and cannot be used at ceramic resonator oscillation.

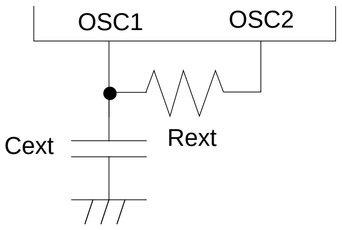


Figure 2 2-pin RC Oscillation Circuit

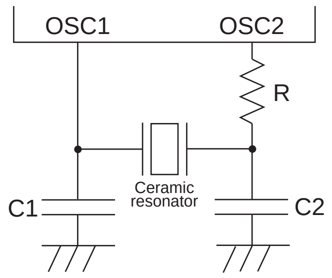


Figure 3 Ceramic Resonator Oscillation Circuit

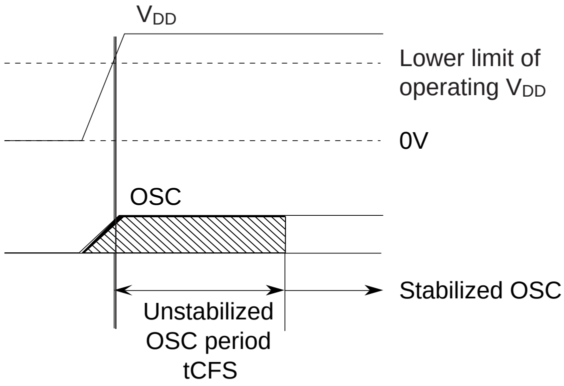


Figure 4 Oscillation Stabilizing Period

Table 1 Constants Guaranteed for Ceramic Resonator OSC

4MHz (Murata)	C1	33 pF±10%
CSA4.00MGU	C2	33 pF±10%
CST4.00MGWU (built-in C)	R	0 Ω
1MHz (Murata)	C1	100 pF±10%
CSB1000J	C2	100 pF±10%
	R	2.2 kΩ
1MHz (Kyocera)	C1	100 pF ±10%
KBR1000F	C2	100 pF ±10%
	R	0 Ω
800kHz (Murata)	C1	100 pF±10%
CSB800J	C2	100 pF±10%
	R	2.2 kΩ
800kHz (Kyocera)	C1	100 pF±10%
KBR800F	C2	100 pF±10%
	R	0 Ω
400kHz (Murata)	C1	220 pF±10%
CSB400P	C2	220 pF±10%
	R	2.2 kΩ
400kHz (Kyocera)	C1	330 pF±10%
KBR400BK	C2	330 pF±10%
	R	0 Ω

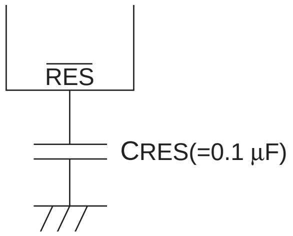


Figure 5 Reset Circuit

(Note) When the rise time of the power supply is 0, the reset time becomes 10 ms to 100 ms at C_{RES} = 0.1 µF.
If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10ms or more.

RC Oscillation Characteristic of the LC6527L, 6528L

Fig. 6 shows the RC oscillation characteristic of the LC6527L, 6528L. For the variation range of RC OSC frequency of the LC6527L, 6528L, the following are guaranteed at the external constants only shown below.

V_{DD} = 2.2 V to 6.0 V, Ta = –40°C to +85°C
External constants Cext = 220 pF
Rext = 12 kΩ
281 kHz ≤ fMOSC ≤ 580 kHz

If any other constants than specified above are used, the range of Rext = 3 kΩ to 20 kΩ, Cext = 150 pF to 390 pF must be observed. (See Figure 6.)

(*6) : The oscillation frequency at V_{DD} = 5.0 V, Ta = +25°C must be in the range of 350 kHz to 500 kHz.
(*7) : The oscillation frequency at V_{DD} = 2.2 to 6.0 V and Ta = –40°C to +85°C must be within the operation clock frequency range.

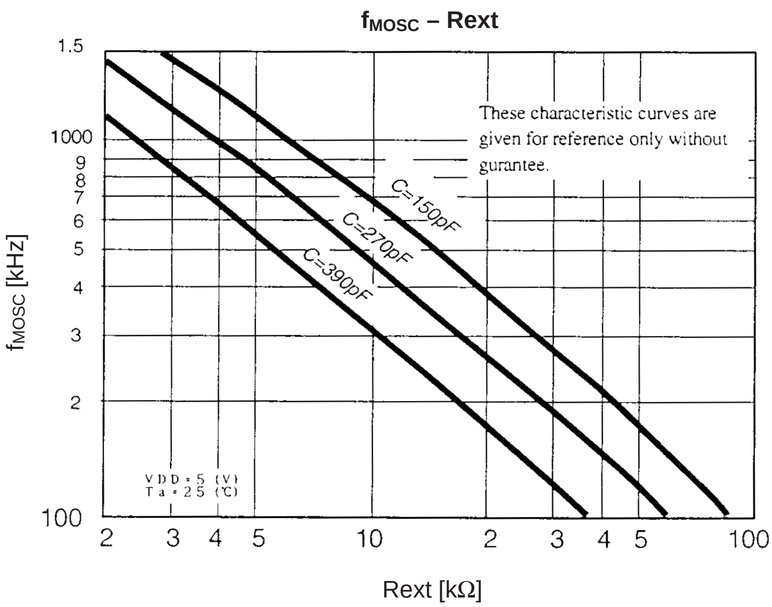


Figure 6 RC Oscillation Frequency Data (typ.)

Notes for Program Evaluation

• When evaluating the LC6527/28 with the evaluation chip (LC6596, LC65PG23/26), the following must be observed.

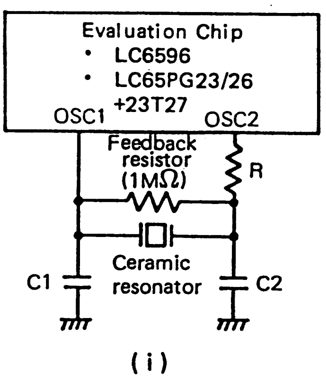
Classi-fication	Item	Function		Notes for evaluation
		Mass-production chip	Evaluation chip	
Notes for option	2-pin OSC	PH_0 and OSC2 share one pin (PH_0/OSC2). Either of them is selected exclusively by user option. When 2-pin OSC is selected, PH_0/OSC2 pin provides OSC2 and performs no function as PH_0 port. Data input to PH_0/OSC2 by mistake is always read as "0".	Evaluation chip has PH_0 and OSC2 separately. Pin required for option is selected as required. Even when OSC2 pin is selected by option, PH_0 circuit is present and functions as complete port PH_0.	Since input/output at PH_0 on evaluation chip results in difference between evaluation chip operation and mass-production chip operation, input/output at PH_0 is prohibited.
	OSC predivider	3 selections (1/1, 1/3, 1/4) by option.	3 selections (1/1, 1/3, 1/4) available by 2 pins of DIV pin, 3OR4 pin.	DIV pin, 3OR4 pin must be set according to option specified for mass-production chip.
	Ports C, D output level at reset mode	Ports C, D can be brought to "H" or "L" in a group of 4 bits.	Port C and port D can be brought to "H" and "L" by CHL pin and DHL pin respectively.	CHL pin and DHL in must be set according to option specified for mass-production chip.
	Port output configuration PU/OD	PU or OD can be selected bitwise.	Only OD without PU.	[LC6596-applied evaluation] External resistor (15kΩ) on evaluation board must be connected to necessary port. [Piggyback-applied evalutaion] Resistor must be connected to necessary port on application board.
	PU resistor configuration	PU resistor brought to Hi-Z (Pch Tr to turn OFF) at "L" output mode.	PU resistor, being external resistor, whose impedance remains unchanged at "L" output mode.	For mass-production chip, leakage current only flows in Pch Tr at "L" output mode; for evaluation chip, current continues flowing in PU resistor at "L" output mode.
Notes for OSC	OSC constants-1	[2-pin RC OSC] Catalog-guaranteed constants provide OSC at frequency specified in catalog.	[2-pin RC OSC] Different from mass-production chip in circuit design and characteristic.	[2-pin RC OSC] Frequency must be adjusted to OSC frequency of mass-production chip by adjusting variable rest iro.
		[2-pin ceramic resonator OSC] Catalog-guaranteed constants provide OSC at frequency specified in catalog.	[2-pin ceramic resonator OSC] Different from mass-production chip in circuit design and characteristic. Wiring capacitance may provide unstable OSC.	[2-pin ceramic resonator OSC] External constants must be fine-adjusted according to service conditions.
	OSC constants-2 (Note)	[2-pin ceramic resonator OSC] Feedback resistor is contained.	[2-pin ceramic resonator OSC] No feedback resistor is contained.	[2-pin ceramic resonator OSC] For evaluation chip, feedback resistor of 1MΩ must be connected externally.

Continued on next page.

Continued from preceding page.

Classi-fication	Item	Function		Notes for evaluation
		Mass-production chip	Evaluation chip	
Notes for electrical characteristics	OSC frequency	OSC frequency characteristic as indicated in catalog.	Different from mass-production chip in circuit design, and characteristic.	ES, CS must be used to evaluate characteristic in detail.
	Operating current, standby current	Current characteristic as indicated in catalog.	Different from mass-production chip in circuit design, characteris-tic.	
Other notes	Type No. setting	LC6527/28 differ in ROM, RAM.	ROM, RAM to be used according to Type No. are set by INSTC, MEMC.	INSTC, MEMC are set according to Type No. of mass-production chip.
	Evaluation chip pin setting		Input pin RSTC, which is not provided in mass-production chip, is provided.	SW4 on evaluation board must remain turned OFF.

Note) When the evaluation chip is used in the 2-pin ceramic resonator OSC mode, no feedback resistor is contained unlike the mass-production chip. Connect a feedback resistor of 1 MΩ externally as shown below.
Since constants R, C also differ from those for the mass-production chip, refer to Table 1 and adjust the capacitor value according to the stray capacitance of the circuit.



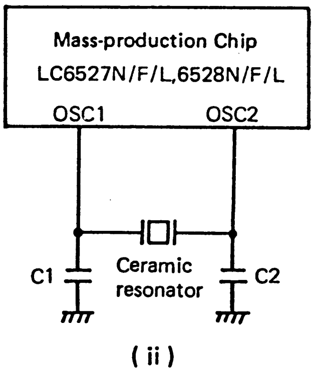


Figure 1 2-Pin Ceramic Resonator OSC Circuit for Evaluation Chip and Mass-production Chip

Ceramic resonator		Mass-production chip C1 = C2	Evaluation chip (*)			
			Including capacitance of standard cable (FAS-20-03B)		Including no capacitance of standard cable (FAS-20-03B)	
			C1 = C2	R	C1 = C2	R
4 MHz	CSA4.00MG (Murata)	30 pF	8 pF	0 Ω	33 pF	0 Ω
	KBR4.0MS (Kyocera)	33 pF	8 pF	0 Ω	33 pF	0 Ω
1 MHz	CSB1000K (Murata)	(Using CSB1000D) 100 pF	82 pF	2.2 kΩ	100 pF	2.2 kΩ
	KBR1000H (Kyocera)	100 pF	82 pF	2.2 kΩ	100 pF	2.2 kΩ
800 kHz	CSB800K (Murata)	(Using CSB800D) 100 pF	120 pF	2.2 kΩ	150 pF	2.2 kΩ
	KBR800H (Kyocera)	100 pF	120 pF	2.2 kΩ	150 pF	2.2 kΩ
400 kHz	CSB400P (Murata)	330 pF	220 pF	3.3 kΩ	270 pF	3.3 kΩ
	KBR400B, KBR400H (Kyocera)	150 pF	330 pF	1.0 kΩ	330 pF	1.0 kΩ

Table 1 Reference Values of Constants R, C

(*) Standard cable (FAS-20-03B) is a cable attached to target board EVA-TB6523C/26C/27C/28C.
Table 1 shows two cases where the capacitance of the cable is included and no capacitance of the cable is included.

- Example where the capacitance of the cable is included
  The capacitance of the cable is included when the resonator is connected to the user's applciation board through the cable from the EVA-TB6523C/26C/27C/28C.
- Example where no capacitance of the cable is included
  No capacitance of the cable is included when the resonator is placed near the evaluation chip (on the EVA-TB6523C/26C / 27C/28C).

When using any other cable than the attached cable, adjust the capacitor value according to the stray capacitance.

LC6527, 6528 Instruction Set (by function)

Symbol	Description				
AC	: Accumulator	$P(DP_L)$	: Input/output port addressed by DP_L	( ), [ ]	: Contents
ACt	: Accumulator bit t			←	: Transfer and direction
CF	: Carry flag	PC	: Program counter	+	: Addition
DP	: Data pointer	STACK	: Stack register	–	: Subtraction
E	: E register	TM	: Timer	Y	: Exclusive OR
M	: Memory	TMF	: Timer (internal) interrupt request flag		
M (DP)	: Memory addressed by DP	ZF	: Zero flag		

Instruction group	Mnemonic		Instruction code D_7 D_6 D_5 D_4	Instruction code D_3 D_2 D_1 D_0	Bytes	Cycles	Function	Description	Status flag affected	Remarks
Accumulator manipulation instructions	CLA	Clear AC	1 1 0 0	0 0 0 0	1	1	AC ← 0	The AC contents are cleared.	ZF	*1
	CLC	Clear CF	1 1 1 0	0 0 0 1	1	1	CF ← 0	The CF contents are cleared.	CF	
	STC	Set CF	1 1 1 1	0 0 0 1	1	1	CF ← 1	The CF is set.	CF	
	CMA	Complement AC	1 1 1 0	1 0 1 1	1	1	AC ← $(\overline{AC})$	The AC contents are complemented.	ZF	
	INC	Increment AC	0 0 0 0	1 1 1 0	1	1	AC ← (AC) + 1	The AC contents are incremented +1.	ZF CF	
	DEC	Decrement AC	0 0 0 0	1 1 1 1	1	1	AC ← (AC) – 1	The AC contents are decremented –1.	ZF CF	
	TAE	Transfer AC to E	0 0 0 0	0 0 1 1	1	1	E ← (AC)	The AC contents are transferred to the E.		
	XAE	Exchange AC with E	0 0 0 0	1 1 0 1	1	1	(AC) ⇆ (E)	The AC contents and the E contents are exchanged.		
Memory manipulation instructions	INM	Increment M	0 0 1 0	1 1 1 0	1	1	M(DP) ← [M (DP)] + 1	The M(DP) contents are incremented +1.	ZF CF	
	DEM	Decrement M	0 0 1 0	1 1 1 1	1	1	M(DP) ← [M(DP)] – 1	The M(DP) contents are decremented –1.	ZF CF	
	SMB bit	Set M data bit	0 0 0 0	1 0 B_1 B_0	1	1	M(DP, B_1B_0) ← 1	A single bit of the M(DP) specified with B_1B_0 is set.		
	RMB bit	Reset M data bit	0 0 1 0	1 0 B_1 B_0	1	1	M(DP, B_1B_0) ← 0	A single bit of the M(DP) specified with B_1B_0 is reset.	ZF	
Arithmetic operation/comparison instructions	AD	Add M to AC	0 1 1 0	0 0 0 0	1	1	AC ← = (AC) + [M(DP)]	Binary addition of the AC contents and the M(DP) contents is performed and the result is stored in the AC.	ZF CF	
	ADC	Add M to AC with CF	0 0 1 0	0 0 0 0	1	1	AC ← (AC) + [M(DP)] +(CF)	Binary addition of the AC, CF contents and the M(DP) contents is performed and the result is stored in the AC.	ZF CF	
	DAA	Decimal adjust AC in addition	1 1 1 0	0 1 1 0	1	1	AC ← (AC) + 6	6 is added to the AC contents.	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 1 0	1 0 1 0	1	1	AC ← (AC) + 10	10 is added to the AC contents.	ZF	
	EXL	Exclusive or M to AC	1 1 1 1	0 1 0 1	1	1	AC ← (AC) Y [M(DP)]	The AC contents and the M(DP) contents are exclusive OR ad and the result is stored in the AC.	ZF	
	CM	Compare AC with M	1 1 1 1	1 0 1 1	1	1	$\overline{[M(DP)]}$ + (AC) + 1	The AC contents and the M(DP) contents are compared and the CF and ZF are set/ reset. Comparison result / CF / ZF [M(DP)] > (AC) / 0 / 0 [M(DP)] = (AC) / 1 / 1 [M(DP)] < (AC) / 1 / 0	ZF CF	

Instruction group	Mnemonic		Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks
			D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0						
	CI data	Compare AC with immediate data	0 0 1 0 0 1 0 0	1 1 0 0 I_3 I_2 I_1 I_0	2	2	$\overline{I_3I_2I_1I_0}$ + (AC) + 1	The AC contents and the immediate data $I_3I_2I_1I_0$ are compared and the ZF and CF are set/reset. Comparison result / CF / ZF: $I_3I_2I_1I_0$ > (AC): 0, 0 $I_3I_2I_1I_0$ = (AC): 1, 1 $I_3I_2I_1I_0$ < (AC): 1, 0	ZF CF	
Load/store instructions	LI data	Load AC with immediate data	1 1 0 0	I_3 I_2 I_1 I_0	1	1	AC ← $I_3I_2I_1I_0$	The immediate data $I_3I_2I_1I_0$ is loaded in the AC.	ZF	*1
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	M(DP) ← (AC)	The AC contents are stored in the M(DP).		
	L	Load AC from M	0 0 1 0	0 0 0 1	1	1	AC ← [M(DP)]	The M(DP) contents are loaded in the AC.	ZF	
Data pointer manipulation instructions	LDZ data	Load DP_H with Zero and DP_L with immediate data respectively	1 0 0 0	I_3 I_2 I_1 I_0	1	1	DP_H ← 0 DP_L ← $I_3I_2I_1I_0$	The DP_H and DP_L are loaded with 0 and the immediate data $I_3I_2I_1I_0$ respectively.		
	LHI data	Load DP_H with immediate data	0 1 0 0	0 0 I_1 I_0	1	1	DP_H ← I_1I_0	The DP_H is loaded with the immediate data I_1I_0.		
	IND	Increment DP_L	1 1 1 0	1 1 1 0	1	1	DP_L ← (DP_L) + 1	The DP_L contents are incremented + 1.	ZF	
	DED	Decrement DP_L	1 1 1 0	1 1 1 1	1	1	DP_L ← (DP_L) – 1	The DP_L contents are decremented – 1.	ZF	
	TAL	Transfer AC to DP_L	1 1 1 1	0 1 1 1	1	1	DP_L ← (AC)	The AC contents are transferred to the DP_L.		
	TLA	Transfer DP_L to AC	1 1 1 0	1 0 0 1	1	1	AC ← (DP_L)	The DP_L contents are transferred to the AC.	ZF	
Jump/subroutine instructions	JMP addr	Jump	0 1 1 0 P_7 P_6 P_5 P_4	1 0 P_9 P_8 P_3 P_2 P_1 P_0	2	2	PC ← $P_9P_8P_7P_6P_5$ $P_4P_3P_2P_1P_0$	A jump to the address specified with immediate data $P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$ occurs.		
	CZP addr	Call subroutine in the zero page	1 0 1 1	P_3 P_2 P_1 P_0	1	1	STACK ← (PC) + 1 PC_{9-6} PC_{1-0} ← 0 PC_{5-2} ← $P_3P_2P_1P_0$	A subroutine is page 0 is called.		
	CAL addr	Call subroutine	1 0 1 0 P_7 P_6 P_5 P_4	1 0 P_9 P_8 P_3 P_2 P_1 P_0	2	2	STACK ← (PC) + 2 PC_{9-0} ← $P_6P_5P_4P_3P_2P_1P_0$	A subroutine is called.		
	RT	Return from subroutine	0 1 1 0	0 0 1 0	1	1	PC ← (STACK)	A return from a subroutine occurs.		
Branch instructions	BA_t addr	Branch on AC bit	0 1 1 1 P_7 P_6 P_5 P_4	0 0 t_1 t_0 P_3 P_2 P_1 P_0	2	2	PC_{7-0} ← $P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if AC_t = 1	If a single bit of the AC specified with the immediate data t_1t_0 is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BA0 to BA3 according to the value of t.
	BNA_t addr	Branch on no AC bit	0 0 1 1 P_7 P_6 P_5 P_4	0 0 t_1 t_0 P_3 P_2 P_1 P_0	2	2	PC_{7-0} ← $P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if AC_t = 0	If a single bit of the AC specified with the immediate data t_1t_0 is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BNA0 to BÑA3 according to the value of t.
	BM_t addr	Branch on M bit	0 1 1 1 P_7 P_6 P_5 P_4	0 1 t_1 t_0 P_3 P_2 P_1 P_0	2	2	PC_{7-0} ← $P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if [M(DP, t_1t_0)] = 1	If a single bit of the M(DP) specified with the immediate data t_1t_0 is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BM0 to BM3 according to the value of t.

Instruction group	Mnemonic		Instruction code $D_7 D_6 D_5 D_4$	Instruction code $D_3 D_2 D_1 D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
	BNM_t addr	Branch on no M bit	0 0 1 1 $P_7 P_6 P_5 P_4$	0 1 t_1 t_0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7-0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if [M(DP, t_1t_0)] = 0	If a single bit of the M(DP) specified with the immediate data t_1t_0 is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BNM0 to BNM3 according to the value of t.
	BP_t addr	Branch on Port bit	0 1 1 1 $P_7 P_6 P_5 P_4$	1 0 t_1 t_0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7-0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if [P(DP_L t_1t_0)] = 1	If a single bit of port P(DP_L) specified with the immediate data t_1t_0 is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BP0 to BP3 according to the value of t.
	BNP_t addr	Branch on no Port bit	0 0 1 1 $P_7 P_6 P_5 P_4$	1 0 t_1 t_0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7-0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if [P(DP_L, t_1t_0)] = 0	If a single bit of port P(DP_L) specified with the immediate data t_1t_0 is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BNP0 to BNP3 according to the value of t.
	BTM addr	Branch on timer	0 1 1 1 $P_7 P_6 P_5 P_4$	1 1 0 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7-0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if TMF = 1 then TMF ← 0	If the TMF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs. The TMF is reset.	TMF	
	BNTM addr	Branch on no timer	0 0 1 1 $P_7 P_6 P_5 P_4$	1 1 0 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7-0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if TMF = 0 then TMF ← 0	If the TMF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs. The TMF is reset.	TMF	
	BC addr	Branch on CF	0 1 1 1 $P_7 P_6 P_5 P_4$	1 1 1 1 $P_3 P_2 P_1 P_0$	2	2	$PC_{7-0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if CF = 1	If the CF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BNC addr	Branch on no CF	0 0 1 1 $P_7 P_6 P_5 P_4$	1 1 1 1 $P_3 P_2 P_1 P_0$	2	2	$PC_{7-0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if CF = 0	If the CF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BZ addr	Branch on ZF	0 1 1 1 $P_7 P_6 P_5 P_4$	1 1 1 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7-0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if ZF = 1	If the ZF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
	BNZ addr	Branch on no ZF	0 0 1 1 $P_7 P_6 P_5 P_4$	1 1 1 0 $P_3 P_2 P_1 P_0$	2	2	$PC_{7-0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if ZF = 0	If the ZF is 0 a branch to the addressd specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
Input/output instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	AC ← [P(DP_L)]	Port P(DP_L) contents are loaded in the AC.	ZF	
	OP	Output AC to port	0 1 1 0	0 0 0 1	1	1	P(DP_L) ← (AC)	The AC contents are outputted to port P(DP_L).		
	SPB bit	Set port bit	0 0 0 0	0 1 B_1B_0	1	2	P(DP_L, B_1B_0) ← 1	A single bit in prot P(DP_L) specified with the immediate data B_1B_0 is set.		When this instruction is executed, the E contents are destroyed.
	RPB bit	Reset port bit	0 0 1 0	0 1 B_1B_0	1	2	P(DP_L, B_1B_0) ← 0	A single bit in port P(DP_L) specified with the immediate data B_1B_0 is reset.	ZF	When this instruction is executed, the E contents are destroyed.

Instruction group	Mnemonic		Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks
			D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0						
Other instructions	WTTM	Write timer	1 1 1 1	1 0 0 1	1	1	TM ← (E), (AC) TMF ← 0	The E and AC contents are loaded in the timer. The TMF is reset.	TMF	
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt	All operations stop.		Only when all pins of port PA are set at L stop.
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	No operation is performed, but 1 machine cycle is consumed.		

*1 If the CLA instruction is used continuously in such a manner as CLA, CLA, ---, the first CLA instruction only is effective and the following CLA instructions are changed to the NOP instructions. This is also true of the LI instruction.

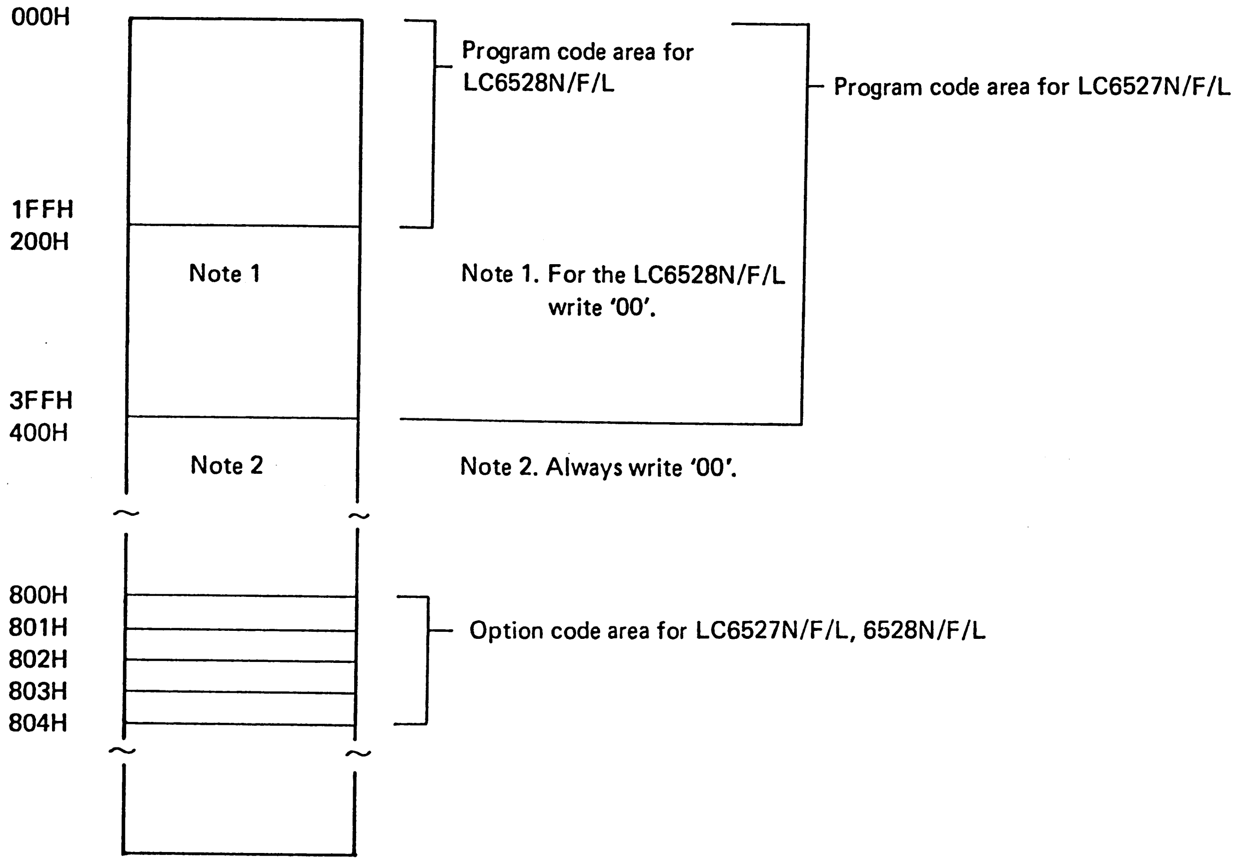
(The following instructions, which are included in the instruction set of the LC6523, 6526, are excluded.
AND, BFn, BI, BNFn, BNI, CLI, JPEA, OR RAL, RCTL, RFB, RTI, RTBL, SCTL, SFB, X, XAH, XA0, XA1, XA2, XA3, XD, XH0, XH1, XI, XL0, XL1, XM)

LC6527N/F/L, 6528N/F/L Option Code Specifying Method

General Description

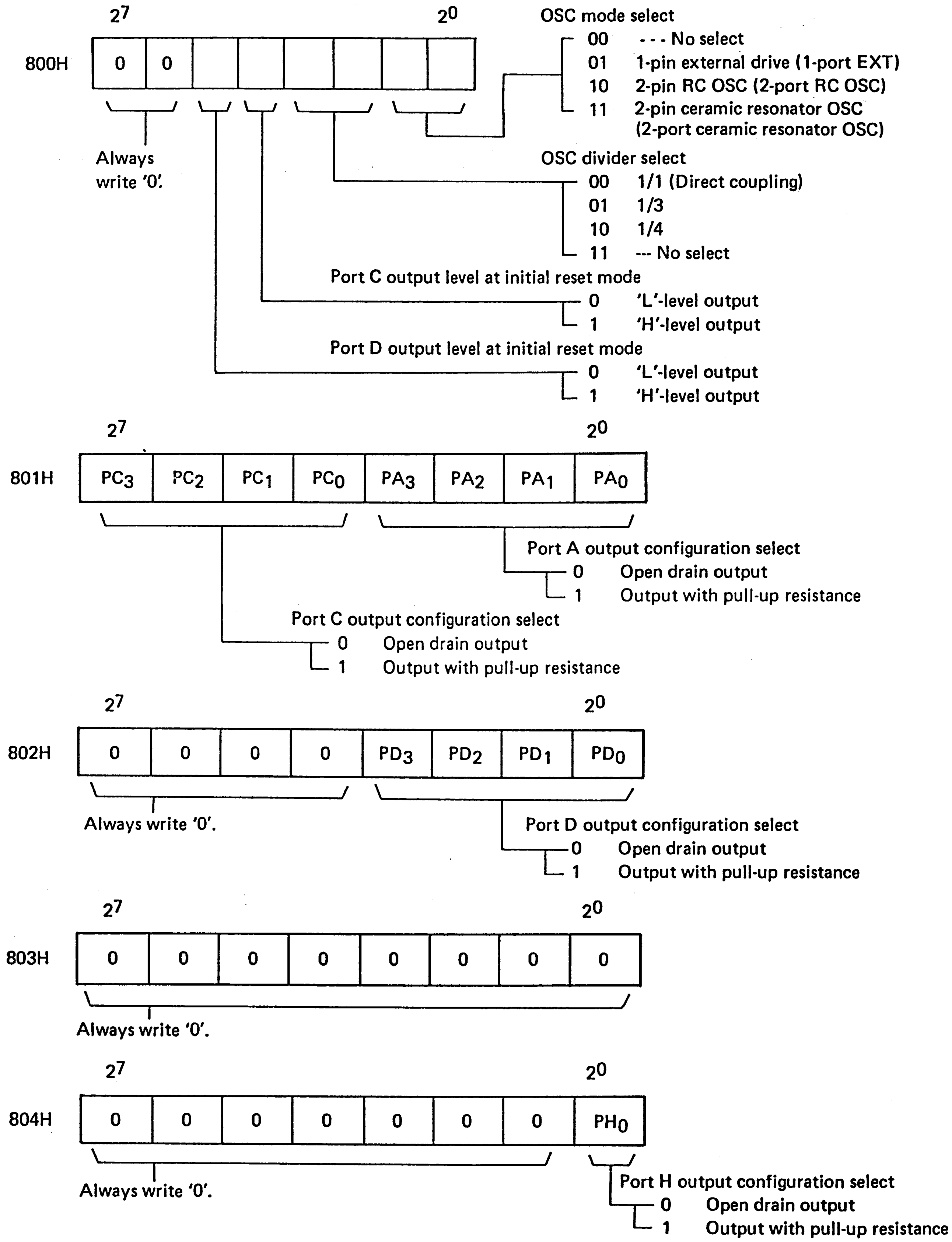
It is requested that you should submit to us various mask options of the LC6527N/F/L, LC6528N/F/L together with the program code which are stored in an EPROM.
By using our cross assembler for the LC6527, 6528, the option code can be specified interactively and stored in the EPROM.
If our cross assembler is not used, specify the option code as shown below. (This is the same as the method where the cross assembler is creasted automatically.)

The Type No. of the EPROM to be submitted is 2732 or 2764.



LC6527N/L, LC6528N/L Option Code Specifying Method

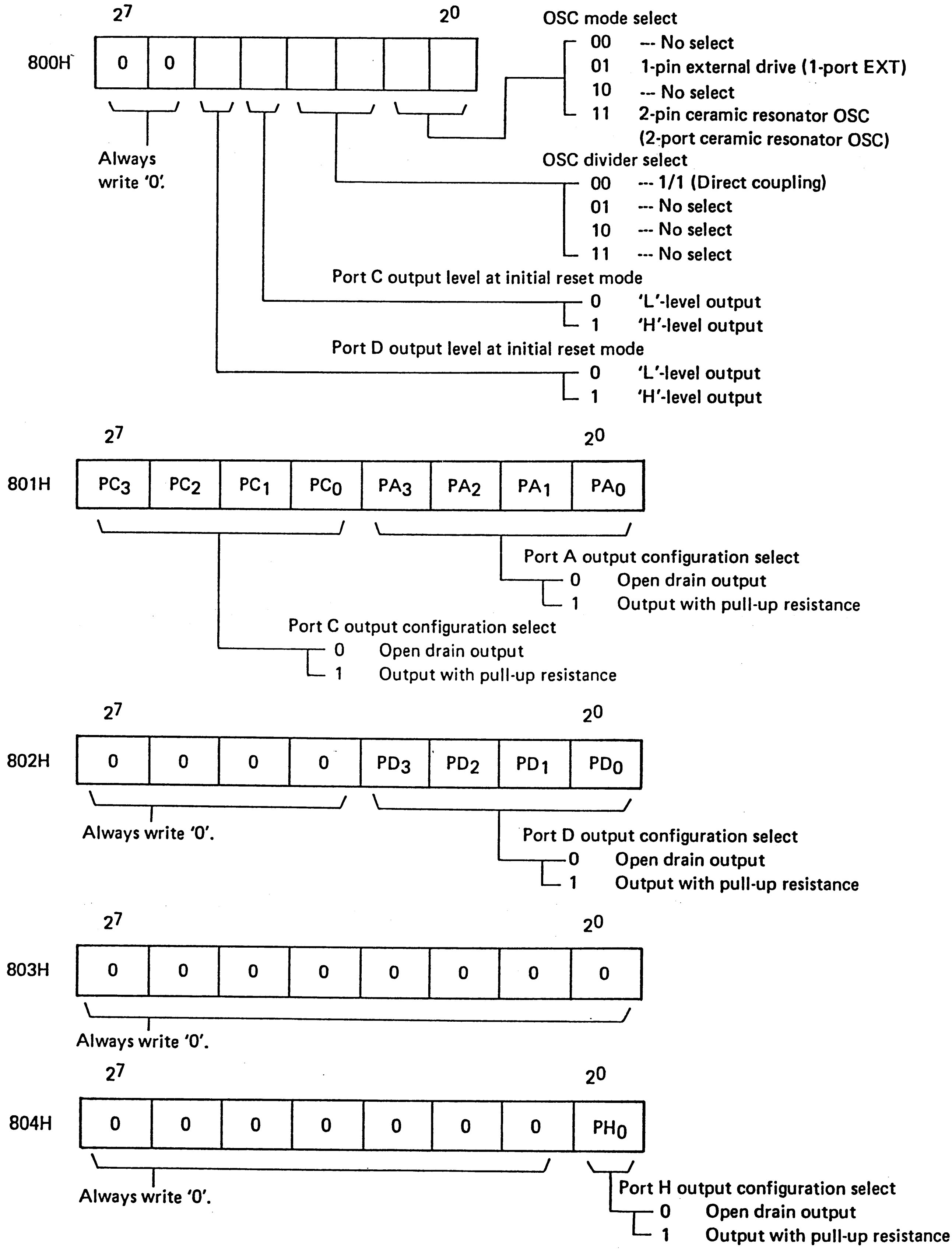
Always write '0' in the area of 0.



Note: When the 2-pin OSC mode is selected, always write '0'.

LC6527F, LC6528F Option Code Specifying Method

Always write '0' in the area of 0.



Note: When the 2-pin OSC mode is selected, always write '0'.

Notes for Standby Function Application

The LC6527N/F/L, 6528N/F/L provide the standby function called HALT mode to minimize the current dissipation when the program is in the wait state.
The standby function is controlled by the HALT instruction, PA pin, $\overline{RES}$ pin.
A peripheral circuit and program must be so designed as to provide precise control of the standby function. In most applications where the standby function is performed, voltage regulation, instantaneous break of power, and external noise are not negligible. When designing an application circuit and program, whether or not to take some measures must be considered according to the extent to which these factors are allowed. This section mainly describes power failure backup for which the standby function is mostly used. A sample application circuit where the standby function is performed precisely is shown below and notes for circuit design and program design are also given below.
When using the standby function, the application circuit shown below must be used and the notes must be also fully observed.
If any other method than shown in this section is applied, it is necessary to fully check the environmental conditions such as power failure and the actual operation of application equipment.

1. HALT mode release conditions
   The HALT mode setting, release conditions are shown in Table 1.

Table 1 HALT mode setting, release conditions

HALT mode setting conditions	HALT mode release conditions
HALT instruction Provided that PA_3 is at high level.	① Reset (Low level is applied to $\overline{RES}$.) ② Low level is applied to PA_3.

Note) HALT mode release condition ② is available only when the RC mode is used for system clock generation; and unavailable when the ceramic resonator mode is used because the OSC circuit may not operate normally.

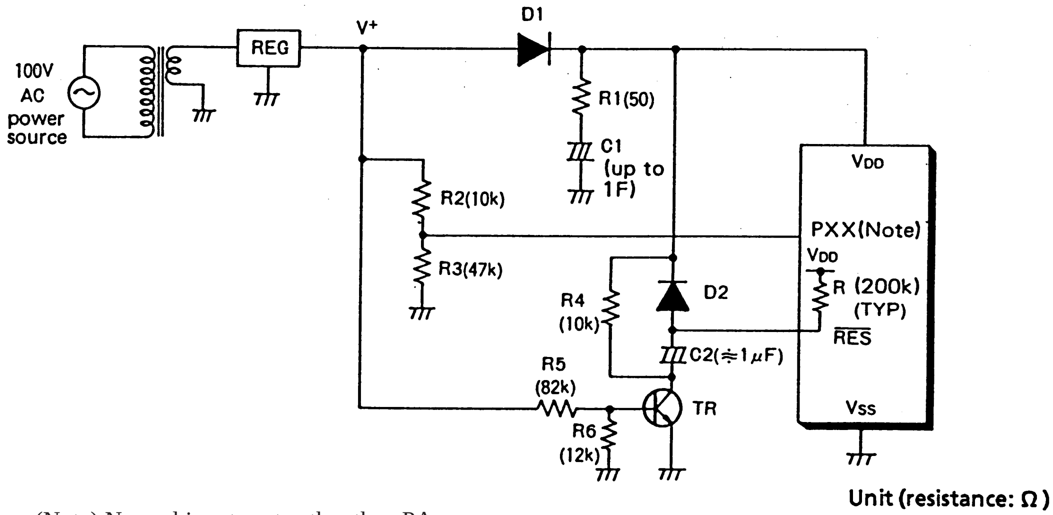
2. Proper cares in using standby function
   When using the standby function, an application circuit and program must be designed with the following in mind.
   (1) The supply voltage at the standby state must not be <u>less</u> than specified.
   (2) Input timing and conditions of each control signal ($\overline{RES}$, PA_3) must be observed at the standby initiate/release state.
   (3) Release operation must not be overlapped at the time of execution of the HALT instruction.

   A sample applicastion where the standby function is used for power failure backup is shown below as a concrete method to observe these notes. A sample application circuit, its operation, and notes for program design are given below.

   Sample application where the standby function is used for power failure backup.
   Power failure backup is an application where power failure of the main power source is detected and the HALT instruction is executed to cause the standby state to be entered. The power dissipation is minimized and a backup capacitor is used to retain the contents of the internal registers for a certain period of time. After power is restored, a reset occurs automatically and the execution of the program starts at address 000H of the program counter (PC). Shown below are sample applications where the program selects or not between power-ON reset and reset after power is restored, notes, measures for instantaneous break of AC power.

2-1. Sample application 1 where the standby function is used for power failure backup
Shown below is a sample application where the program does not select between power-ON reset and reset after power is restored.

2-1-1. Sample application circuit – (1)
Fig. 2-1 shows a sample application where the standby function is used for power failure backup.



(Note) Normal input ports other than PA_3.

Fig. 2-1. Sample Application – (1) where the Standby Function is Used for Power Failure Backup

2-1-2. Operating waveform in sample application circuit – (1)
The operating waveform in the sample application circuit in Fig. 2-1 is shown in Fig. 2-2. The mode is roughly divided as follows:
(a) Power-ON reset
(b) Instantaneous break of main power source
(c) Return from power failure backup

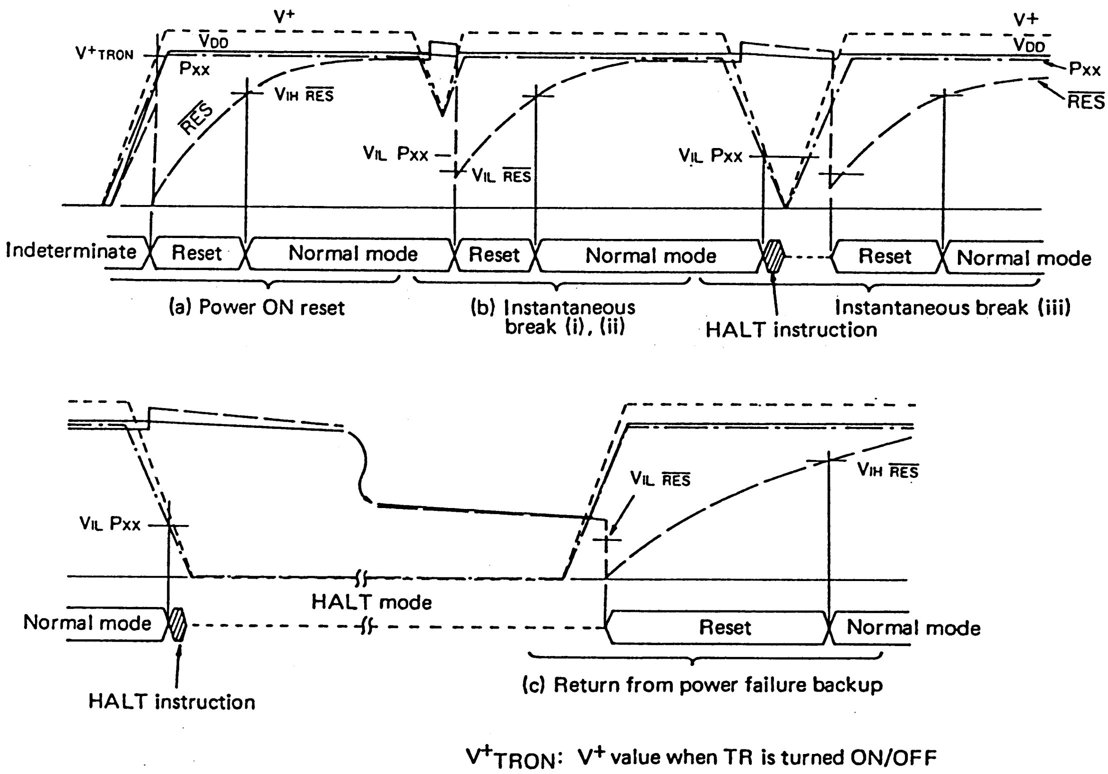


Fig. 2-2 Operating Waveform in Sample Application Circuit – (1)

2-1-3. Operation of sample application circuit – (1)

(a) At the time of power-ON reset

After power rises, a reset occurs automatically and the execution of the program starts at address 000H of the program counter (PC).

– Note –

This sample application circuit provides an indeterminate region where no reset occurs before the operating V_{DD} range is entered.

(b) At the time of instantaneous break

(i) When the P_{XX} input voltage does not meet V_{IL} (the P_{XX} input level does not get lower than input threshold level V_{IL}) and the $\overline{RES}$ input voltage only meets V_{IL}:
A reset occurs in the normal mode, providing the same operation as power-ON reset.

(ii) When both of the P_{XX} input voltage and $\overline{RES}$ input voltage do not meet V_{IL}:
The program continues running in the normal mode.

(iii) When both of the P_{XX} input voltage and $\overline{RES}$ input voltage meet V_{IL}:
When two pollings do not regard the P_{XX} input voltage as "L" level, the HALT mode is not entered and reset occurs.
When two pollings regard the P_{XX} input voltage as "L" level, the HALT mode is entered and after power is restored a reset occurs, releasing the standby mode.

(c) At the time of return from power failure backup

After power is restored, a reset occurs, releasing the standby mode.

2-1-4. Notes for design of sample application circuit – (1)

- V^+ rise time and C2
  Make the time constant (C2, R) of the reset circuit 10 times as long as the V^+ rise time. (R: ON-chip resistor, 200kohms typ.)
  Make the V^+ rise time shorter (up to 20ms).
- R1 and C1
  Make the R1 value as small as possible. Make the C1 value as large as possible according to the backup time calculated. (Fix the R1 value so that the C1 charging current does not exceed the power source capacity.)
- R2 and R3
  Make the "H"-level input voltage applied to the P_{XX} pin equal to V_{DD}.
- R4
  Fix the time constant of C2 and C4 so that C2 can discharge during the period of time from when V^+ gets lower than V^+TRON (TR OFF) at the time of instantaneous break until the P_{XX} input voltage gets lower than V_{IL} (because release by reset is not available after the HALT mode is entered by instantaneous break).
- R5 and R6
  Make V^+ (V_{BE} = 0.6V is obtained by R5 and R6) when the reset circuit works (Tr ON) more than (operating V_{DD} min + V_F of diode D1).
  Observing this note, make V^+ as low as possible to provide a reset early enough after power-ON.
- Backup time
  The normal operastion continues with a relatively high current dissipation from when power failure is detected by the P_{XX} until the HALT instruction is executed. Fix the C1 value so that the standby supply voltage is held during backup time of set + above-mentioned time.

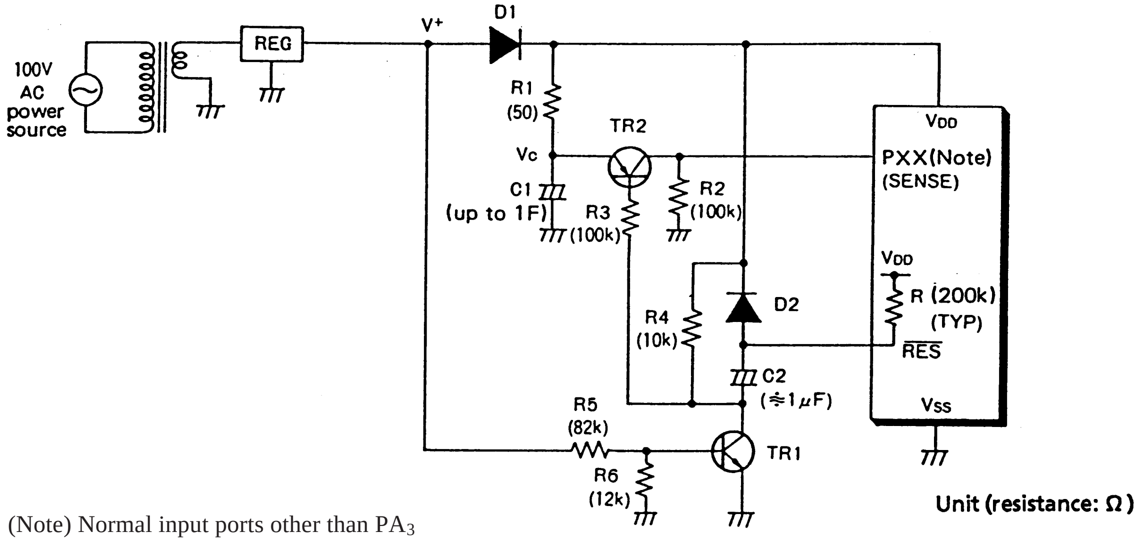
2-1-5. Notes for software design

- Design the program so that port A_3 is brought to "H" level at the standby mode.
- Check a standby request by polling the input port twice.
  (Example)

```
        ¦
        ¦
        ¦
       BP1      AAA     ; 1st polling
       BP1      AAA     ; 2nd polling
       HALT             ; Standby
        ¦
        ¦
        ¦
AAA:
```

2-2. Sample application 2 where the standby function is used for power failure backup
Shown below is a sample application where the program selects between power-ON reset and reset after power is restored.

2-2-1. Sample application circuit – (2) (No instantaneous break in power source)
Fig. 2-3 shows a sample application where the standby function is used for power failure backup.



(Note) Normal input ports other than PA_3

Fig. 2-3 Sample Application – (2) where the Standby Function is Used for Power Failure Backup

2-2-2. Operating waveform in sample application circuit – (2)
The operating waveform in the sample applicatioin circuit in Fig. 2-3 is shown in Fig. 2-4. The mode is roughly divided as follows:
(1) Power-ON reset
(2) Return from power failure backup

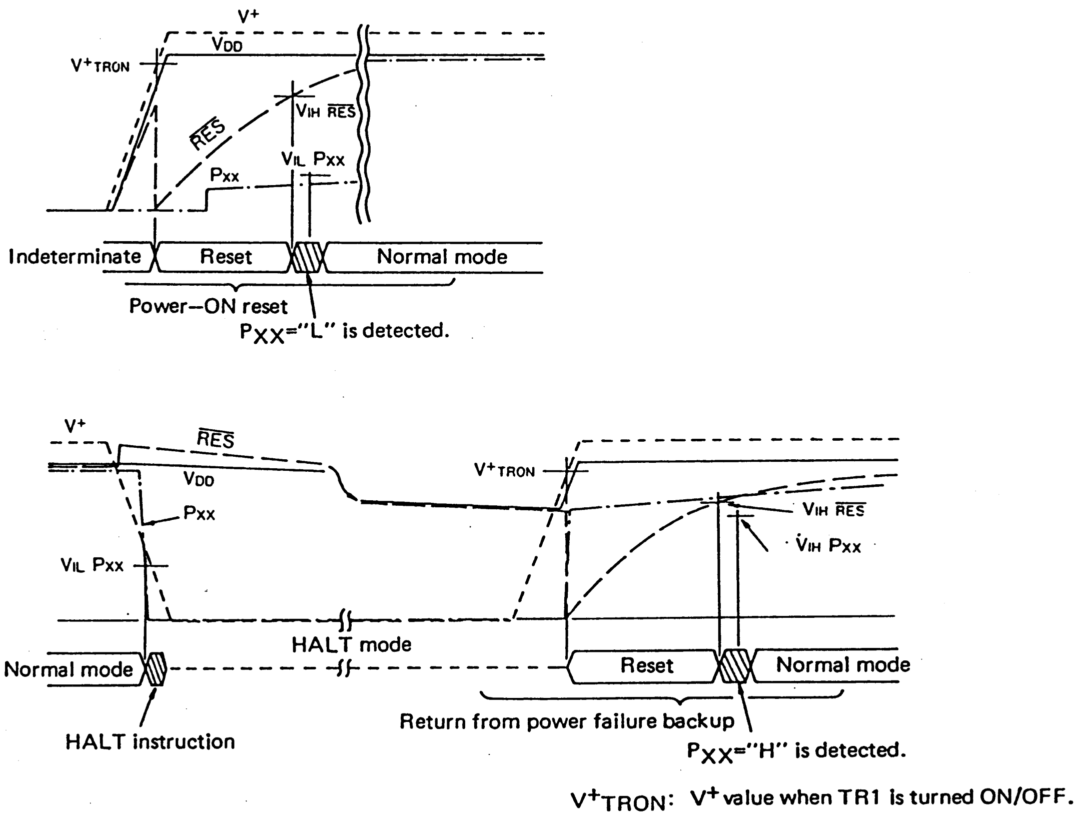


Fig. 2-4 Operating Waveform in Sample Application Circuit – (2)

2-2-3. Operating of sample application circuit – (2)

(a) At the time of power-ON reset

The operation and notes are the same as for sample application circuit – (1), except that after reset release P_{XX}="L" is program-detected to decide program start after initial reset.

(b) Standby initiation

When one polling regrds the P_{XX} input voltage as "L" level, the HALT mode is entered.

(c) At the time of return from power failure backup

After power is restored, a reset occurs, releasing the standby mode.

After standby release P_{XX}="H" is program-detected, deciding program start after power is restored.

– Note –

If power is restored after V_{DD} during power failure backup gets lower than V_{IH} on the P_{XX}, P_{XX}="L" may be program-detected, deciding program start after initial reset.

2-2-4. Notes for design of sample application circuit – (2)

- R2 and R3
  Fix the R2 value so that R2 ≫ R1 is yielded and fix the R3 value so that I_B of TR2 is limited.
- R4
  There is no severe restriction on the R4 value, but fix it so that C2 can discharge quickly.
  Other notes are the same as for sample application circuit – (1).

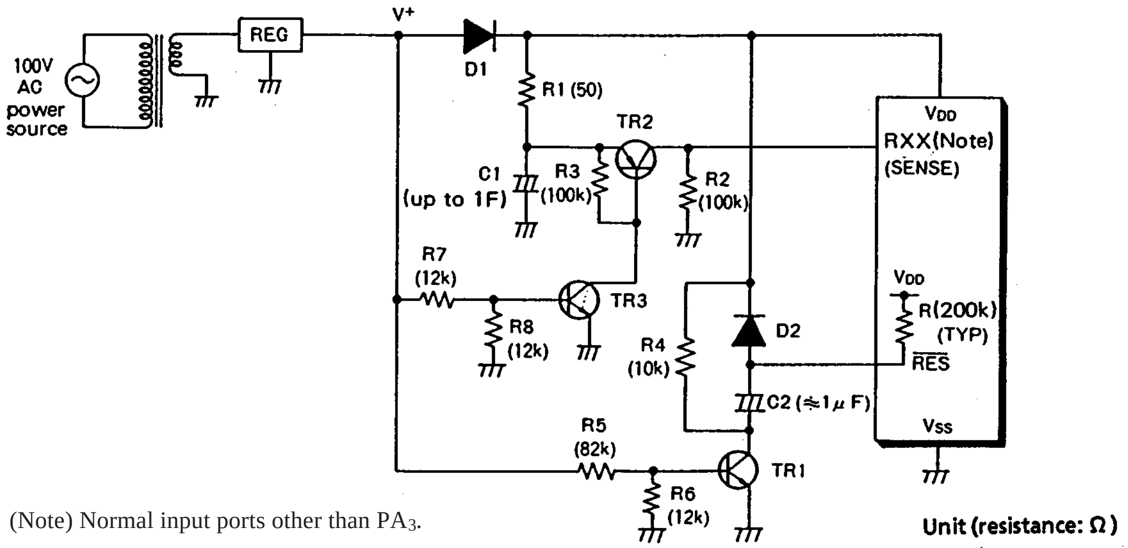
2-2-5. Notes for software design

- Design the program so that port A_3 is brought to "H" level at the standby mode.
- Check a standby request by polling the input port once.
  (Example)

```
              ¦
              ¦
              ¦
             BP1        AAA        ; Polling
             HALT                  ; Standby
              ¦
              ¦
              ¦
AAA:
```

2-3. Sample application 3 where the standby function is used for power failure backup

2-3-1. Sample application circuit – (30) (There is an instantaneous break in power source.)
Fig. 2-5 shows a sample application where the standby function is used for power failure backup.



(Note) Normal input ports other than PA_3.

Fig. 2-5 Sample Application – (3) where the Standby Function is Used for Power Failure Backup

2-3-2. Operating waveform in sample application circuit – (3)
The operating waveform in the sample application circuit in Fig. 2-5 is shown in Fig. 2-6. The mode is roughly divided as follows:

(1) Power-ON reset
(2) Instantaneous break of main power source
(3) Return from power failure backup

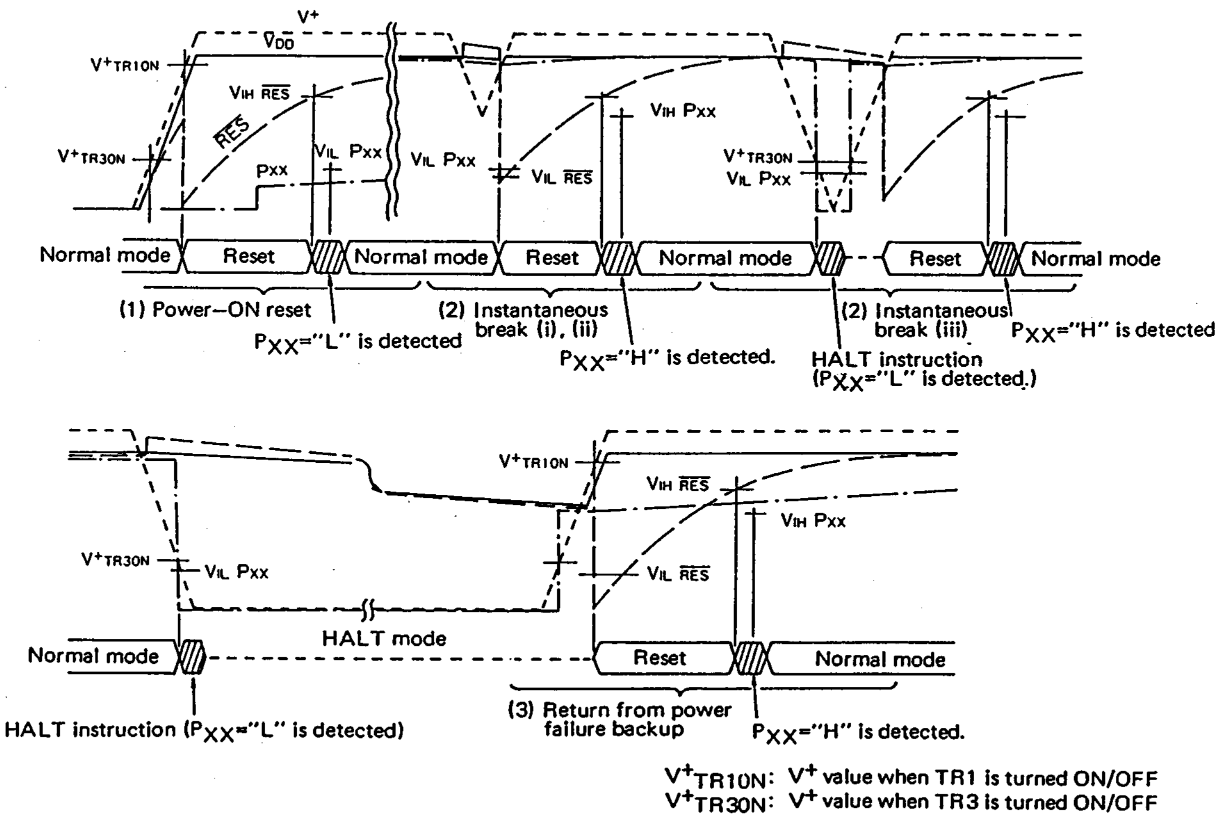


Fig. 2-6 Operating Waveform in Sample Application Circuit – (3)

2-3-3. Operation of sample application circuit – (3)

(a) At the time of power-ON reset
The operation and notes are the same as for sample application circuit – (2)

(b) At the time of instantaneous break

(i) When the P_{XX} input voltage does not meet V_{IL} (the P_{XX} input level does not get lower than input threshold level V_{IL}) and the $\overline{RES}$ input voltage only meets V_{IL}:
A reset occurs in the normal mode. After reset release P_{XX}="H" is program-detected, deciding program start after instantaneous break.

(ii) When both of the P_{XX} input voltage and $\overline{RES}$ input voltage do not meet V_{IL}:
The program continues running in the normal mode.

(iii) When both of the P_{XX} input voltage and $\overline{RES}$ input voltage meet V_{IL}:
When two pollings do not regard the P_{XX} input voltage as "L" level, the HALT mode is not entered and a reset occurs.
When two pollings regard the P_{XX} input voltage as "L" level, the HALT mode is entered and after power is restored a reset occurs, releasing the standby mode. After standby release P_{XX}="H" is program-detected, deciding program start after instantaneous break.

(c) At the time of return from power failure backup
The operation and notes are the same as for sample application circuit – (2)

2-3-4. Notes for design of sample application circuit – (3)

- R3
  Bias resistance of TR2
- R7 and R8
  Fix the R7 and R8 values so that TR3 is turned ON/OFF at approximately 1.5V of V^+.

Other notes are the same as for sample application circuit – (1).

2-3-5. Notes for software design
Same as for sample application circuit – (1).