IS62LV6416LL

64K x 16 HIGH-SPEED ULTRA-LOW POWER CMOS STATIC RAM WITH 3.3V SUPPLY

ADVANCE INFORMATION
APRIL 1997

FEATURES

- High-speed access time: 15, 20, 35, and 45 ns
- CMOS low power operation
  - — 40 mW (typical) operating
  - — 90 µW (typical) standby
- TTL compatible interface levels
- Single 3.3V ± 10% power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- Available in 44-pin SOJ package and 44-pin TSOP

DESCRIPTION

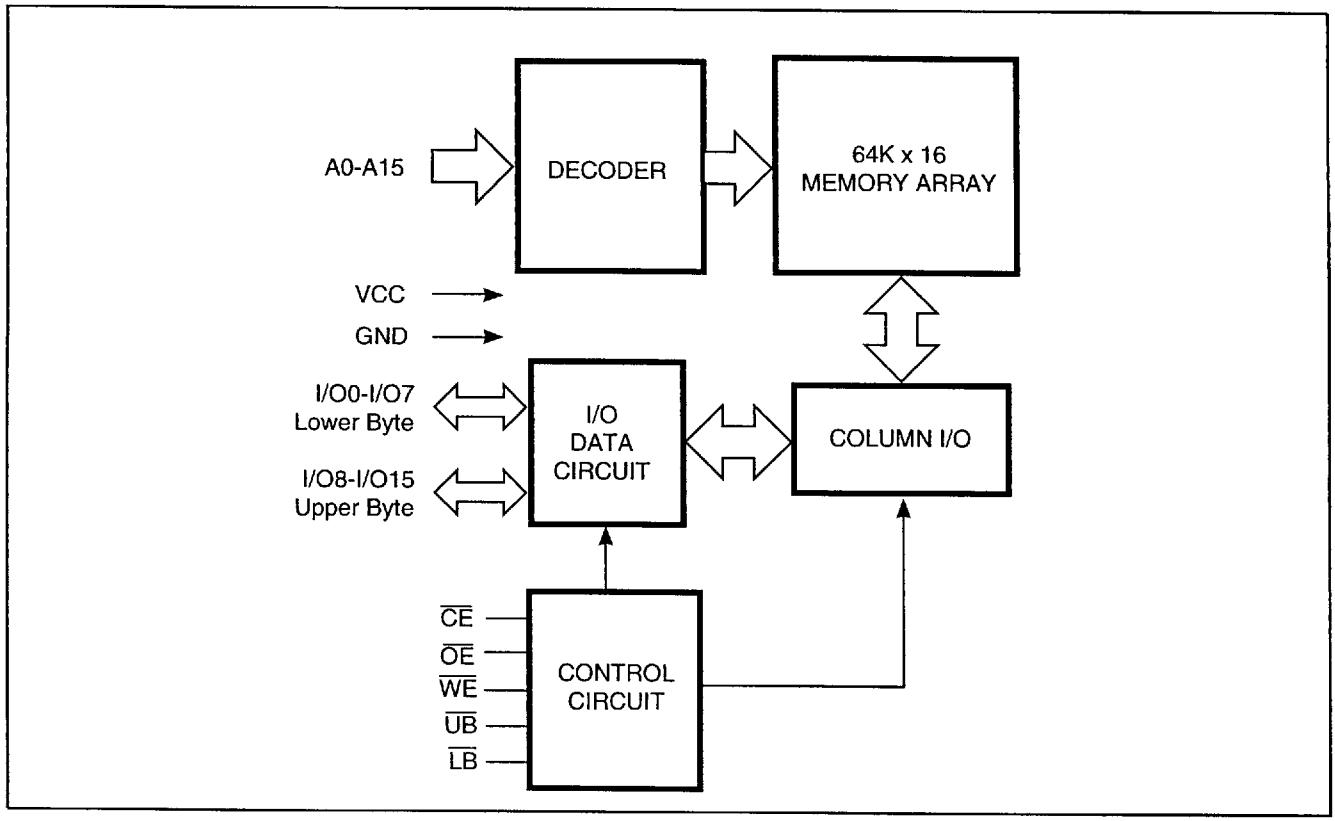
The *ISSI* IS62LV6416LL is a high-speed, ultra-low power, 1,048,576-bit static RAM organized as 65,536 words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 15 ns with low power consumption.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

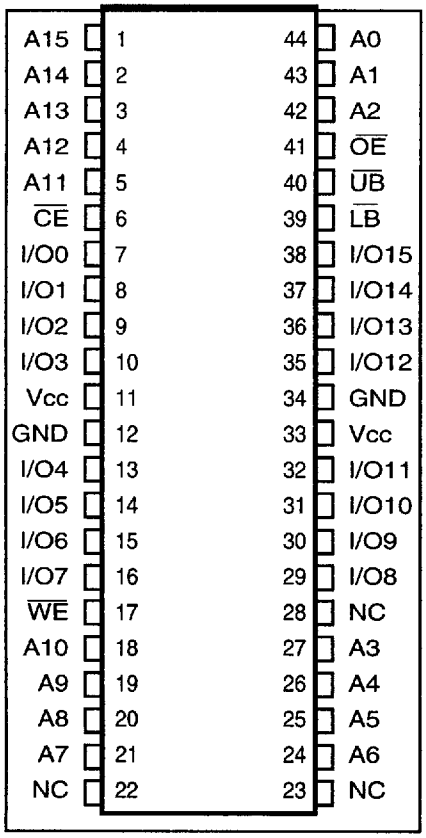
The IS62LV6416LL is packaged in the JEDEC standard 44-pin 400-mil SOJ and 44-pin TSOP.

FUNCTIONAL BLOCK DIAGRAM

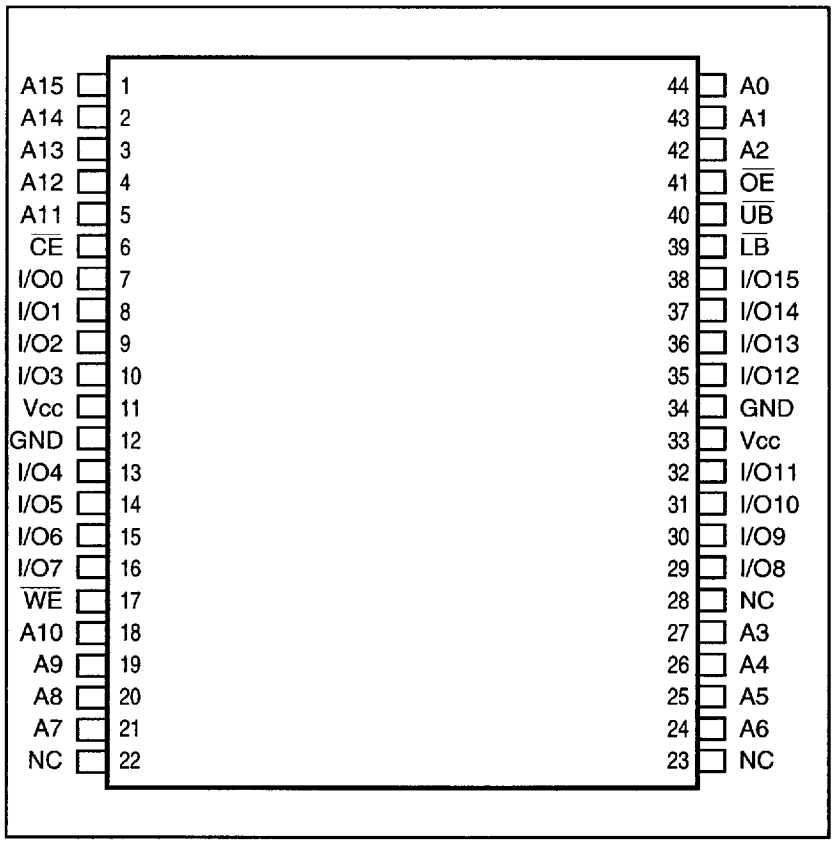


PIN CONFIGURATIONS

44-Pin SOJ



44-Pin TSOP



PIN DESCRIPTIONS

A0-A15	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CE	Chip Enable Input
OE	Output Enable Input
WE	Write Enable Input
LB	Lower-byte Control (I/O0-I/O7)
UB	Upper-byte Control (I/O8-I/O15)
NC	No Connection
Vcc	Power
GND	Ground

TRUTH TABLE

Mode	WE	CE	OE	LB	UB	I/O PIN I/O0-I/O7	I/O PIN I/O8-I/O15	Vcc Current
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	L	H	L	High-Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	X	H	L	High-Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to Vcc+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	–40°C to +85°C	3.3V ± 10%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled	–1	1	µA

Notes:
1. V_{IL} (min.) = –2.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

				-15 ns		-20 ns		-35 ns		-45 ns		
Symbol	Parameter	Test Conditions		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	120	—	110	—	100	—	90	mA
			Ind.	—	140	—	130	—	120	—	110	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE}$ ≥ V_{IH}, f = 0	Com.	—	10	—	10	—	10	—	10	mA
			Ind.	—	20	—	20	—	20	—	20	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com.	—	50	—	50	—	50	—	50	µA
			Ind.	—	80	—	80	—	80	—	80	

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

		-15 ns		-20 ns		-35 ns		-45 ns		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{RC}	Read Cycle Time	15	—	20	—	35	—	45	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	35	—	45	ns
t_{OHA}	Output Hold Time	3	—	3	—	3	—	3	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	15	—	20	—	35	—	45	ns
t_{DOE}	$\overline{OE}$ Access Time	—	7	—	8	—	10	—	20	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	6	—	8	0	10	0	15	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	6	0	8	0	10	0	15	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	3	—	3	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	7	—	8	—	10	—	15	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	6	0	8	0	10	0	15	ns
t_{LZB}	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1a and 1b

AC TEST LOADS

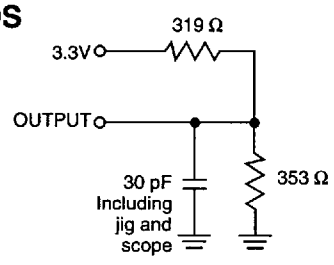


Figure 1a.

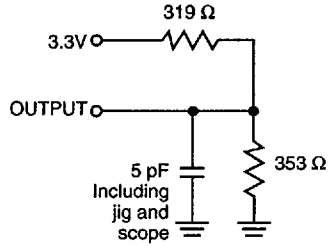
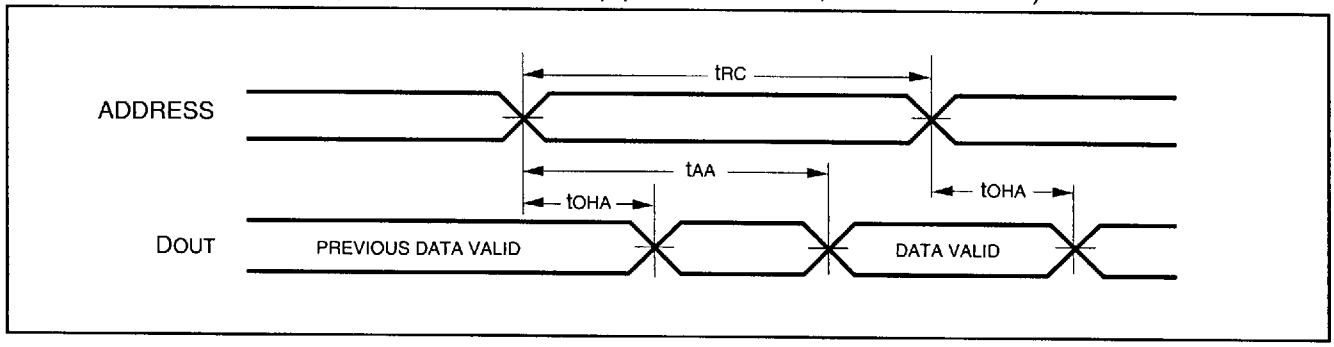


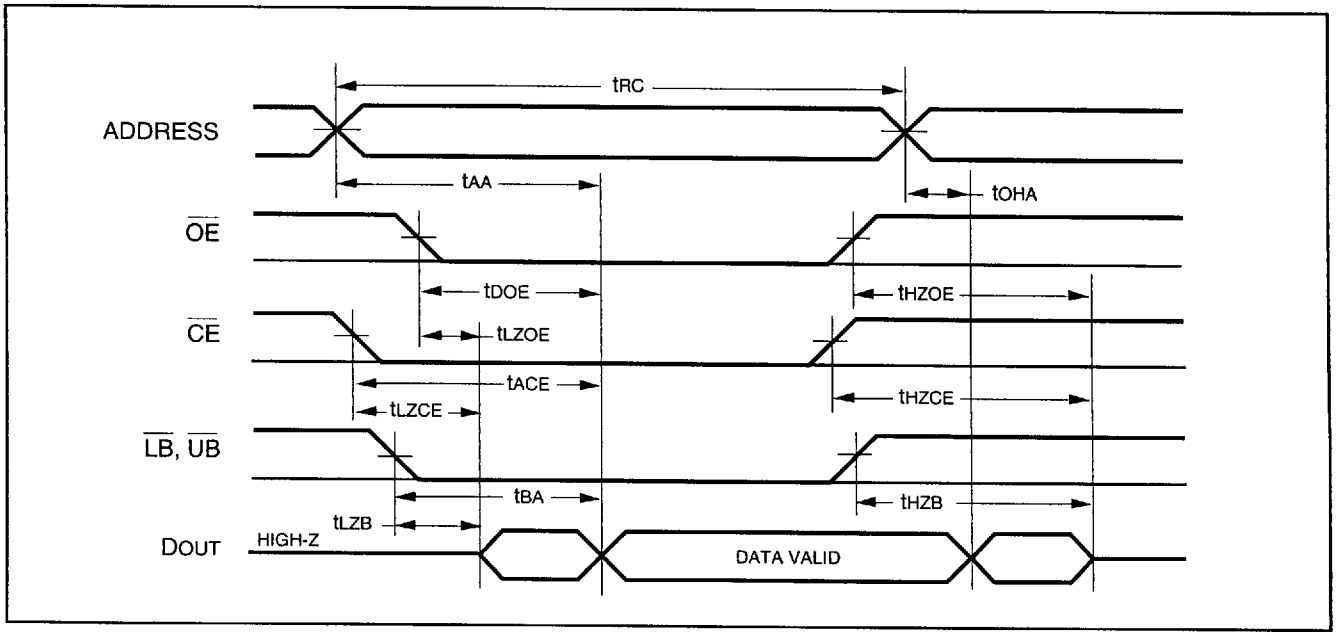
Figure 1b.

AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transition.

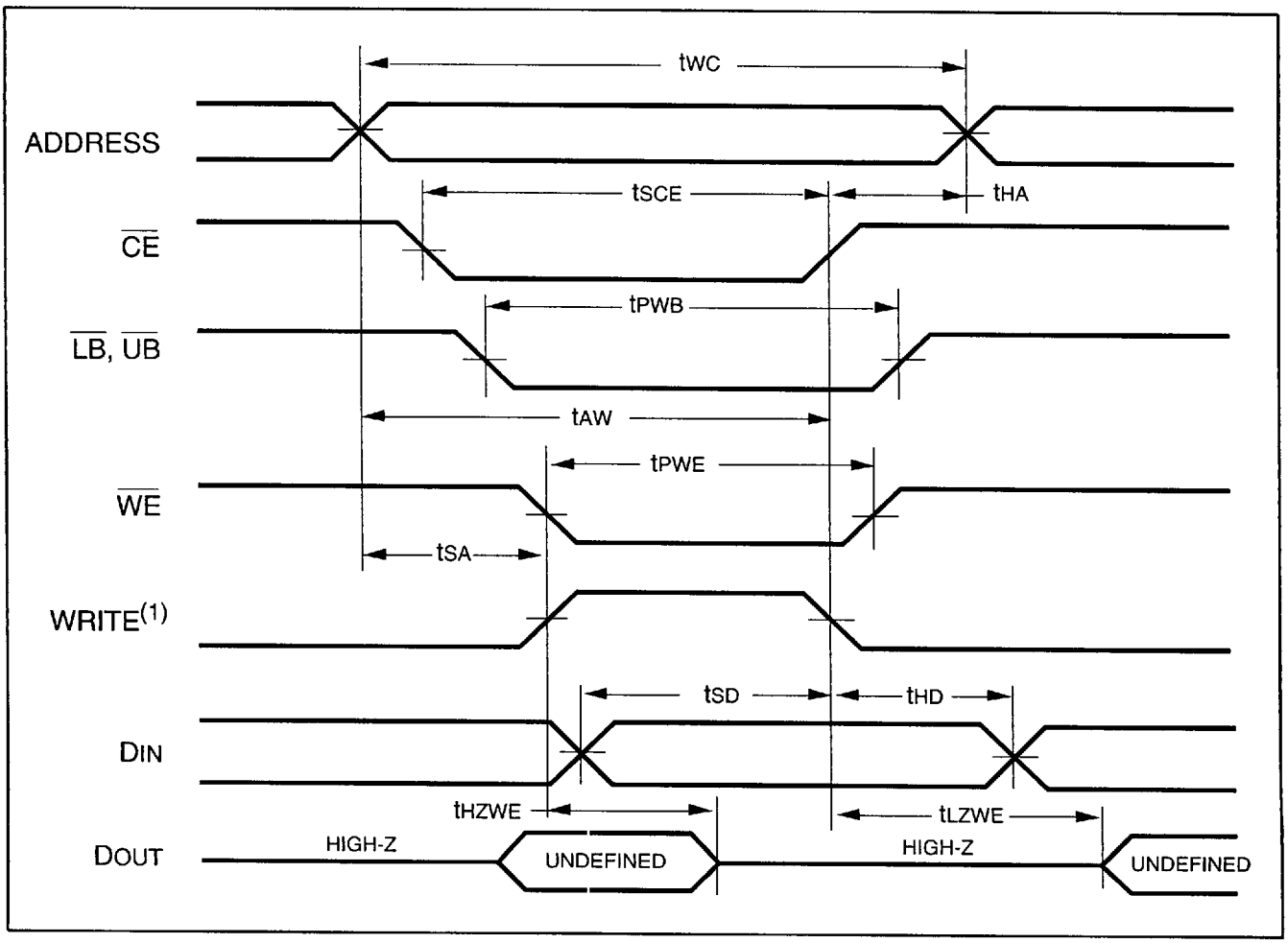
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-15 ns Min.	-15 ns Max.	-20 ns Min.	-20 ns Max.	-35 ns Min.	-35 ns Max.	-45 ns Min.	-45 ns Max.	Unit
t_{WC}	Write Cycle Time	15	—	20	—	35	—	45	—	ns
t_{SCE}	$\overline{CE}$ to Write End	10	—	12	—	25	—	35	—	ns
t_{AW}	Address Setup Time to Write End	10	—	12	—	25	—	35	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	10	—	12	—	25	—	35	—	ns
t_{PWE}	$\overline{WE}$ Pulse Width	10	—	12	—	25	—	35	—	ns
t_{SD}	Data Setup to Write End	7	—	9	—	20	—	25	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	5	—	9	—	10	—	15	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	3	—	3	—	3	—	3	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]



Notes:
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CE}$ and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CE}$) [($\overline{LB}$) = ($\overline{UB}$)] ($\overline{WE}$).

ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
15	IS62LV6416LL-15T	Plastic TSOP
	IS62LV6416LL-15K	400-mil Plastic SOJ
20	IS62LV6416LL-20T	Plastic TSOP
	IS62LV6416LL-20K	400-mil Plastic SOJ
35	IS62LV6416LL-35T	Plastic TSOP
	IS62LV6416LL-35K	400-mil Plastic SOJ
45	IS62LV6416LL-45T	Plastic TSOP
	IS62LV6416LL-45K	400-mil Plastic SOJ

ORDERING INFORMATION
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
15	IS62LV6416LL-15TI	Plastic TSOP
	IS62LV6416LL-15KI	400-mil Plastic SOJ
20	IS62LV6416LL-20TI	Plastic TSOP
	IS62LV6416LL-20KI	400-mil Plastic SOJ
35	IS62LV6416LL-35TI	Plastic TSOP
	IS62LV6416LL-35KI	400-mil Plastic SOJ
45	IS62LV6416LL-45TI	Plastic TSOP
	IS62LV6416LL-45KI	400-mil Plastic SOJ

ISSI

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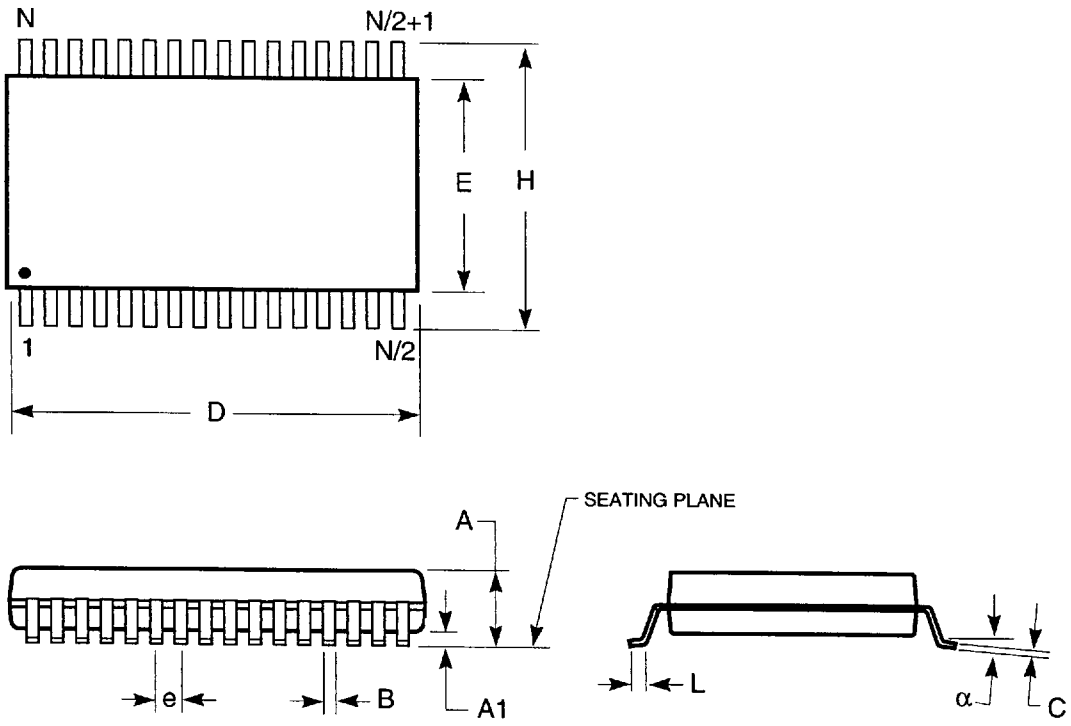
http://www.issiusa.com

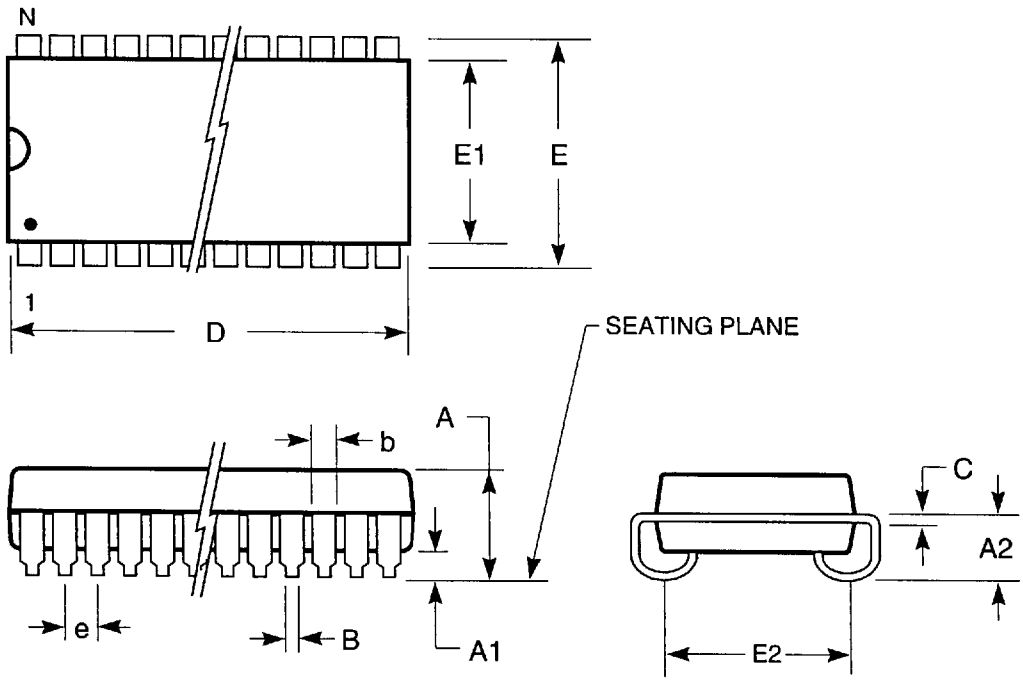
Plastic TSOP
Package Code: T (Type II)



Plastic TSOP (T - Type II)								
	Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.								
No. Leads	32				44			
A	—	1.27	—	0.049	0.991	1.194	0.039	0.047
A1	0.10	0.15	0.004	0.006	0.050	0.150	0.002	0.0059
B	0.30	0.45	0.012	0.020	0.30	0.40	0.012	0.016
C	0.12	0.16	0.004	0.006	0.120	0.210	0.0017	0.0083
D	20.80	21.23	0.811	0.828	18.313	18.517	0.721	0.729
E	10.03	10.29	0.391	0.400	10.058	10.262	0.396	0.404
H	11.56	11.96	0.451	0.466	11.735	11.938	0.462	0.470
e	1.27 BSC		0.050 BSC		0.800 BSC		0.0315 BSC	
L	0.35	0.65	0.014	0.025	0.406	0.597	0.016	0.0235
S	—	0.95	—	0.037	—	0.95	—	0.037
α	0°	5°	0°	5°	0°	5°	0°	5°

Notes:
1. Controlling dimension: millimieters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

400-mil Plastic SOJ
Package Code: K



400-mil Plastic SOIC (J-bend) (K)				
	Inches			
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads	32		44	
A	0.131	0.145	0.128	0.148
A1	0.025	—	0.025	—
A2	0.082	—	0.082	—
B	0.013	0.021	0.015	0.020
b	0.024	0.032	0.026	0.032
C	0.006	0.012	0.007	0.013
D	0.820	0.830	1.120	1.130
E	0.430	0.445	0.435	0.445
E1	0.395	0.405	0.395	0.405
E2	0.354	0.380	0.370 Nom.	
e	0.050 BSC		0.050 BSC	
S	—	0.045	—	0.40

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.