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SSI 32P3040
Pulse Detector with Programmable Filter

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DESCRIPTION

The SSI 32P3040 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of encoded read signals. The circuit will handle a data rate of 32 Mbit/s.

In read mode the SSI 32P3040 provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

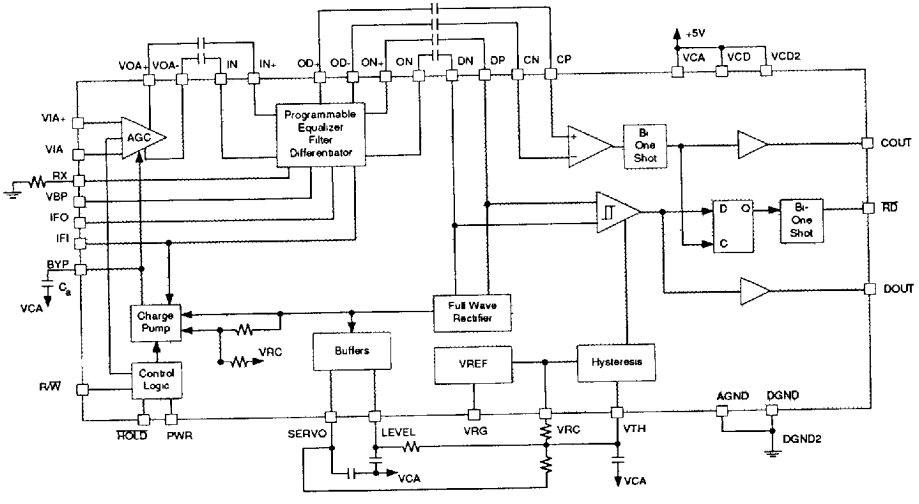
Write to read transient recovery is enhanced by providing AGC input impedance switching and a selectable Fast Recovery mode that provides a higher decay current.

Additionally, the SSI 32P3040 contains an integrated programmable electronic filter with cutoff frequencies between 2.5 and 13 MHz. High frequency boost (for pulse slimming) of up to +9 dB is also provided. The SSI 32P3040 requires only a +5V power supply and is available in 36-lead SOM and 32-lead TQFP packages.

FEATURES

- Compatible with 32 Mbit/s data rate operation
- Fast attack/decay modes for rapid AGC recovery
- Dual rate charge pump for fast transient recovery charge pump currents track programmable channel bandwidth
- Low drift AGC hold, fast AGC recovery, and low AGC input impedance control signals. Circuitry supports programmable gain non-AGC operation
- Temperature compensated, exponential control AGC
- Precision wide bandwidth fullwave rectifier
- Supports programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components
- ±2% Filter group delay variation from 0.3FC to FC
- Servo burst output available
- Differential hysteresis qualifier comparator to ease clock channel timing
- Accurate feed forward or fixed threshold set

BLOCK DIAGRAM



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FEATURES (continued)

- 1 ns max pulse pairing with sine wave input
- 5 mW low power idle mode
- TTL read data output
- +5V only operation
- 36-pin SOM and 32-pin TQFP packages

FUNCTIONAL DESCRIPTION

The SSI 32P3040 Pulse Detector is designed to support a 32 Mbit/s data rate. The signal processing circuits include a wide band variable gain amplifier, a programmable electronic filter, differentiator and pulse slimming equalizer, a precision wide bandwidth fullwave rectifier, and a dual rate charge pump. A fully differential filter, differentiator, equalizer, and fullwave rectifier are provided to minimize external noise pick-up. To optimize recovery for constant density recording, the AGC charge pump current tracks the programmable filter current IFI. The differentiator zero tracks the programmable filter cutoff frequency. Thus in constant density recording applications, an approximately constant differentiated signal amplitude is maintained. The desired filter response and equalization are easily programmed with the SSI 32D4661, Time Base Generator DACs. A dual rate attack charge pump and a Fast Decay mode are included for fast transient recovery. At maximum IFI current, the normal AGC attack current is 0.28 mA. When the signal exceeds 125% of the nominal signal level, the attack current is increased by a factor of 5. The nominal decay current at max IFI is 5.6 µA. The decay current is increased 20 times when in the fast decay mode. In this mode, transients that produce low gain will recover more rapidly with the fast decay current, while transients that produce high gain will put the circuit in the fast attack recovery mode. The decay modes are automatically controlled within the device. When R/$\overline{W}$ is low, the AGC is in its hold mode and its input impedance is switched low. When R/$\overline{W}$ is switched high, the AGC remains in the hold and low input impedance state for 0.7 µs and then switches to the fast decay mode for 0.7 µs. The AGC amplifier input impedance is reduced to allow quick recovery of the AGC amplifier input AC coupling capacitors. When the $\overline{HOLD}$ input is low, the AGC action is stopped and the AGC amplifier gain is set by the voltage at the BYP pin. In most applications, the BYP pin voltage is stored on an external capacitor when $\overline{HOLD}$ goes low. In applications where AGC action is not desired, the BYP voltage can be set by a resistor divider network connected from VCC to VRC. If a programmable gain is desired, the resistor network could be driven by a current DAC. The precision fullwave rectifier produces an accurate Level and Servo output signal. These outputs are referenced to the reference voltage VRC. SERVO and LEVEL are buffered open emitter outputs with 100 ohm series current limiting resistors. These outputs could be further filtered with external capacitors.

LEVEL has an internal 50 µA discharge current source. An optional Servo output capacitor discharge circuit can be included. An external resistor connected to the RX pin sets the electronic filter reference current which is the source from pin IFO. If a programmable frequency response is desired, a portion of the current from IFO, which is proportional to absolute temperature, must be injected into pin IFI. This could be accomplished by a current DAC. Some frequency response programming may be accomplished by connecting IFO to IFI and switching different resistors to pin RX. Frequency boost is accomplished by varying the voltage at VBP. VBP has a nominal 100 mV built-in offset so that the circuit has 0 dB boost for VBP below 100 mV. The voltage at VBP should be proportional to the reference voltage at pin VRG.

A differential comparator with floating hysteresis threshold allows differential signal qualification for noise rejection. An accurate feed forward qualification level is generated by comparing the difference between LEVEL and VRC. VRC is referenced to VCA. Thus with the VTH resistor network connected from VCA to VRC, an accurate fixed threshold can be established. The threshold is clamped to a minimum value of 50 mV. Thus a qualified signal must exceed this minimum level even when the VTH-VRC voltage is zero. A qualified signal zero crossing triggers the output one shot. The one shot period is set internally. Low level differential outputs are provided for high speed operation and to minimize noise generation.

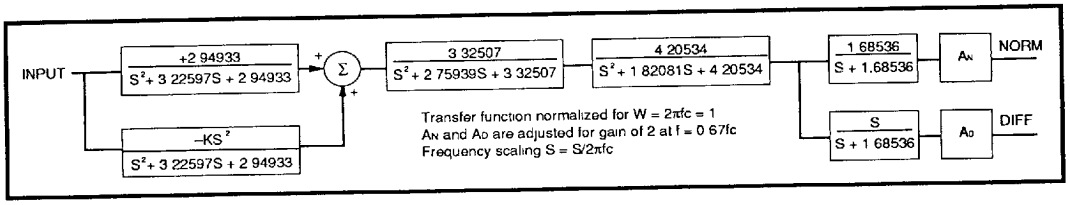

FIGURE 1: Bessel Filter Transfer Function

$$K = 2.94933\,(10^{\frac{BOOST\ (dB)}{20}} - 1)$$

TABLE 1: Typical Change in f - 3 dB Point with Boost

Boost (dB)	Gain@fc (dB)	Gain@peak (dB)	fPeak/fc	f-3dB/fc	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.20	0.36
2	-1	0.00	no peak	1.47	0.76
3	0	0.15	0.62	1.74	1.22
4	1	1.00	1.08	1.96	1.73
5	2	2.12	1.24	2.13	2.30
6	3	3.35	1.24	2.28	2.94
7	4	4.56	1.39	2.42	3.65
8	5	5.82	1.39	2.54	4.46
9	6	7.04	1.39	2.66	5.36
10	7	8.24	1.39	2.77	6.38
11	8	9.41	1.39	2.88	7.52
12	9	10.55	1.39	2.98	8.79
13	10	11.70	1.55	3.08	10.22

Notes: 1. fc is the original programmed cutoff frequency with no boost.
2. f - 3 dB is the new -3 dB value with boost implemented.
3. $f$peak is the frequency where the magnitude peaks with boost implemented.

e.g., fc = 13 MHz when boost = 0 dB
if boost is programmed to 5 dB, then f - 3 dB = 27.69 MHz
$f$peak = 16.12 MHz

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
VIA+, VIA-	I	AGC Amplifier input pins.
IN+, IN-	I	Equalizer/filter input pins.
DP, DN	I	Data inputs to data comparators and fullwave rectifier.
CP, CN	I	Differentiated data inputs to the clock comparator.
VTH	I	Threshold level setting input for the data comparators.
R/$\overline{W}$	I	TTL compatible input when high puts the charge pump in the normal mode.
PWR	I	TTL compatible input when high puts the circuit in its normal operating mode.
$\overline{HOLD}$	I	TTL compatible input when low disables the AGC action by turning off the charge pump.
OUTPUT PINS		
VOA+, VOA-	O	AGC amplifier output pins.
ON+, ON-	O	Equalizer/filter normal output pins.
OD+, OD-	O	Equalizer/filter differentiated output pins.
DOUT	O	Test point for monitoring the data F/F D-input. Usage requires an external 2.4 kΩ resistor from DOUT to GND. (Not available in 32-pin TQFP package.)
COUT	O	Test points for monitoring the data F/F clock inputs. Usage requires an external 2.4 kΩ resistor from DOUT to GND. (Not available in 32-pin TQFP package.)
$\overline{RD}$	O	TTL compatible read data output pins.
LEVEL	O	Open NPN emitter output that provides a fullwave rectified signal for the VTH input. The signal is referenced to VRC.
SERVO	O	Open NPN emitter output that provides a fullwave rectified servo signal. The signal is referenced to VRC.
ANALOG PINS		
VRC	-	Reference voltage pin for SERVO and LEVEL. VRC is referenced to VCA.
VRG	-	Reference voltage pin for the programmable filter. VRG is referenced to ground.
VBP	-	The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND.
RX	-	Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO.
IFO		Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin.

PIN DESCRIPTION (continued)

ANALOG PINS (continued)

NAME	TYPE	DESCRIPTION
IFI		Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency.
BYP		The AGC integrating capacitor C_A is connected between BYP and VCA.
VCA, VCD,VCD2		Analog and Digital +5 volts.
AGND, DGND, DGND2		Analog and Digital grounds.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

ABSOLUTE MAXIMUM RATINGS (Operation above maximum ratings may damage the device.)

PARAMETER	RATING
Storage Temperature	-65 to +150°C
Junction Operating Temperature,Tj	+130°C
Supply Voltage, VCA, VCD	-0.7 to 7V
Voltage Applied to Inputs	-0.5 to VCA, VCD +0.5V

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATING
Supply Voltage	VCA = VCD = VCC	4.5V<VCC<5.5V
Ambient Temperature, Ta		0°C<Ta<70°C

POWER SUPPLY

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ISS	Supply Voltage Current	Active mode		75	90	mA
		Low-Power mode		1	1.5	mA
PD	Power Dissipation	Active mode		400	500	mW
		Low-Power mode		5	8	mW

ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

LOGIC SIGNALS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIL	TTL Input Low Voltage		-0.3		0.8	V
VIH	TTL Input High Voltage		2.0		VCC +0.3	V
IIL	TTL Input Low Current	VIL = 0.4V	-0.4			mA
IIH	TTL Input High Current	VIH = 2.7V			0.1	mA
VOH	TTL Output High Voltage	IOH = -400µA	2.4			V
VOL	TTL Output Low Voltage	IOL = 3 mA			0.5	V
TRDRF	Output Rise and Fall Time	CL = 15 pF			7	ns
TH	Hold Input Switching Times				0.3	µs
TWR	Write to Read Recovery Time	R/$\overline{W}$ pin low to high	0.5		1.4	µs

AGC AMPLIFIER

The input signals are AC coupled to VIA+ and VIA-, VOA+ and VOA- are AC coupled to IN+ and IN-, ON+ and ON- are AC coupled to DP and DN, Ca 1000 pF, Fin = 4 MHz. Unless otherwise specified, the output is measured differentially at VOA+ and VOA-, Fin = 4 MHz and filter boost at Fc = 0dB.

VIR	Input Range	Filter boost at FC = 0 dB	24		240	mVppd
		Filter boost at FC = 9 dB	20		120	mVppd
VDPN	DP-DN voltage	VIA± = 0.1 Vpp	0.85		1.05	Vppd
VDPNV	DP-DN Voltage Variation	24 mV < VIA± < 240 mV			8.0	%
AV	Gain Range		1.9		22	V/V
AVPV	Gain Sensitivity			38		dB/V
VOADR	VOA+, VOA- Dynamic Range	THD = 1% max	0.75			Vpp
ZIN	Input Impedance	R/$\overline{W}$= high	3.0		7.5	kΩ
ZCMIN	Common Mode	R/$\overline{W}$ = high		1.5		kΩ
	Input Impedance	R/$\overline{W}$ = low		200		Ω
VOS	Output Offset Voltage Variation	Over gain range	-200		+200	mV
VINO	Input Noise Voltage	gain = max, filter not connected to VOA±, Rs = 0Ω, Bw = 15 MHz		5	10	nV/√Hz
BW	Bandwidth	No AGC action	55	75		MHz
CMRR	Common-mode Rejection Ratio	gain = max, Vin = 0 VDC + 100 mVpp @ 5 MHz	40	65		dB
PSRR	Power Supply Rejection Ratio	gain = max, 100 mVpp @ 5 MHz on VCA, VCD, VCD2	45	67		dB
TGD	Gain Decay Time	VIA± = 240 mV to 120 mV VOA± >0.9 Final Value BYP ≤, 1000 pF, IFI = max		34	44	µs

ANALOG PINS (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TGA	Gain Attack Time	VIA± = 120 mV to 240 mV VOA± <1.1 Final Value BYP ≤, 1000 pF, IFI = max		1.5	2	µs

AGC CONTROL
The input signals are AC coupled to DP and DN. Ca = 1000 pF, LEVEL load = 50 µA, SERVO load = 100 µA.

VDI	DP-DN Signal Input Range				1.4	Vpp
ALO	Level (Servo) Output Gain	DP-DN = 0.25 to 0.5 VDC LG = (V_{LEVEL} - V_{RC})/2(DP-DN)	0.73		0.81	V/V
BWL	Level (Servo) Output Bandwidth	1 dB	15			MHz
VLO	Level Offset Voltage	Output-VRC, IL = 50 µA			30	mV
VSO	Servo Offset Voltage	Output - VRC, IL = 100 µA			30	mV
ZLS	Level (Servo) Output Impedance	IL = 100 µA		200	300	Ω
ID	Discharge Current			0.008 x IFI		mA
IDF	Fast Discharge Current	0.7 to 1.4 µs after R/$\overline{W}$ goes high		20 x ID		mA
ICH	Charge Pump Attack Current			50 x ID		mA
ICHF	Charge Pump Fast Attack Current	DP-DN = 1.35 Vpp		5 x ICH		mA
IBYP	Pin Leakage Current	$\overline{HOLD}$ = low, V_{BYP} = VCC -1.5V	-0.1		0.1	µA
VRC	Reference Voltage		VCC-2.52		VCC-2.15	V
IVRC	Output Drive		-0.75		0.75	mA
VRG	Reference		2.15		2.5	V
IVRG	Source Current		1			mA
VAGC	Pin Voltage			VRC+1.0		V

EQUALIZER/FILTER The input signals are AC coupled to IN+ and IN-.

f_c	Filter Cutoff Frequency	f_c = 19.14(IFI/IFO)(1/Rx)	2.5		13.5	MHz
V_{RX}	PTAT Reference Current Set Output Voltage	TA = 25°C I_{RX} = 0 - 0.7 mA Rx > 1.21 kΩ		850		mV
IFOR	PTAT Reference Current Output Current Range	TA = 25°C 1.21 kΩ < Rx < 7.73 kΩ IFO = V_{RX}/Rx	0.11		0.7	mA

EQUALIZER/FILTER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IFIR	PTAT Programming Current Range	TA = 25°C, VRX = 850 mV	0.11		0.7	mA
VBPR	Input Voltage Range		0		VRG	V
IBP	Input Bias Current				3	µA
FCA	Filter FC Accuracy	FC = 5 to 13.5 MHz	-12		+12	%
AO	[(ON±)]/[(IN±)] Normal Gain	F = 0.67 FC	1.4		2.2	V/V
AD	[(OD±)]/[(IN±)] Diff Gain	F = 0.67 FC	1.0AO		1.3AO	V/V
FB	Frequency Boost at FC	FB = 20 log [1.884(VBP-0.1) /VRG+1] VBP -0.1>0	0		9.5	dB
FBA	Frequency Boost Accuracy	FB = max	-1		+1	dB
TGD	Group Delay Variation	0.3 FC to FC = 13.5 MHz FB = 0 to max	-2		+2	%
VOO	Output Offset Voltage	Variation over entire frequency range	-200		+200	mV
VOF	Filter Output Dynamic Range	THD = 1.5% max	1.0			Vpp
		THD = 3.0% max F = 0.67 FC	1.25			Vpp
RINF	Filter Input Resistance		4.0	6.0	8.0	kΩ
CINF	Filter Input Capacitance				7	pF
RO	Filter Output Resistance	IO = 0.5 mA		70	85	Ω
IFOD	Filter Output Drive Current		-1		+1	mA
VNN	Eout Output Noise Voltage ON±	BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = 0		2.2	3.0	mVRMS
		BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = VRG		3.0	4.5	mVRMS
VND	Eout Output Noise Voltage OD±	BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = 0		5.4	6.4	mVRMS
		BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = VRG		9.6	10.6	mVRMS

DATA COMPARATOR
The input signals are AC coupled to DP and DN.

RINDC Differential Input Resistnace		7		14	kΩ
CINDC Differential Input Capacitance				5	pF
ATH Threshold Voltage Gain, Kth	0.3 < VTH-VRC < 0.75	0.42		0.49	V/V
VIAMIN Minimum Threshold Voltage	VTH-VRC ≤ 0.11V		.05		V
TPDDC Propagation Delay	To DOUT		10		ns
ITH VTH Input Bias Current				2	µA
DOUTSS DOUT Signal Swing	2.4 kΩ from DOUT to GND		0.5		V

CLOCKING
The input signals are AC coupled to CP and CN.

RINCL Differential Input Resistance		7		14	kΩ
CINCL Differential Input Capacitance				5	pF
TDS D F/F Set Up Time	DP-DN threshold to CP-CN zero cross	0			ns
TPP Pulse Pairing	Vs = 1Vpp, F = 2.5 MHz			1	ns
TPDCL Propagation Delay to RD	Vs = 20 mVpp sq wave		14	20	ns
RDPW Output Pulse Width	Measured at 1.4V level	10		27	ns
COUTS Signal Swing	2.4 kΩ from COUT to GND		0.5		V

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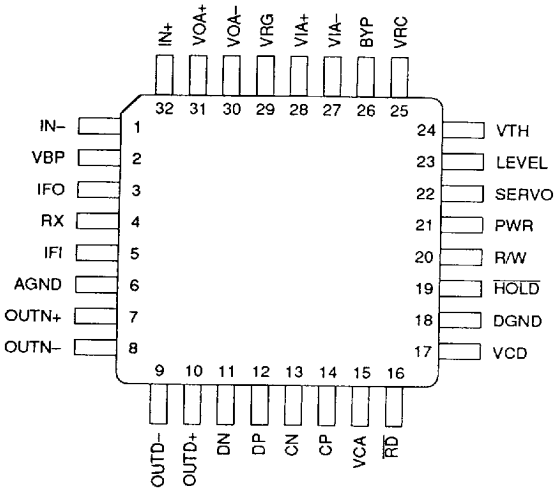
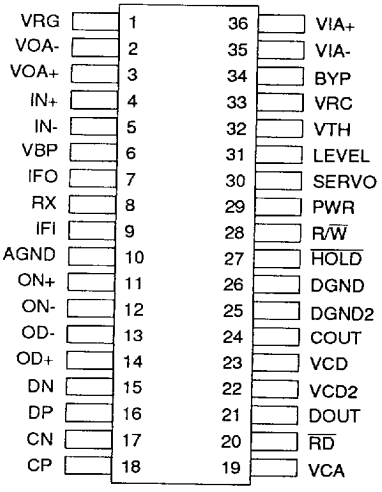
PACKAGE PIN DESIGNATIONS
(Top View)



32-Lead TQFP

THERMAL CHARACTERISTICS: θja

32-Lead TQFP	124° C/W
36-Lead SOM	75° C/W



36-Lead SOM

CAUTION. Use handling procedures necessary for a static sensitive component

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32P3040		
32-Lead Thin Quad Flatpack	32P3040-CGT	32P3040-CGT
36-Lead Small Outline	32P3040-CM	32P3040-CM

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