MC100LVEP34

2.5V / 3.3V ECL ÷2, ÷4, ÷8 Clock Generation Chip

The MC100LVEP34 is a low skew ÷2, ÷4, ÷8 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single–ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock; therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon startup, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as multiple LVEP34s in a system. Single–ended CLK input operation is limited to a $V_{CC} \geq 3.0$ V in PECL mode, or $V_{EE} \leq -3.0$ V in NECL mode.

- 35 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- The 100 Series Contains Temperature Compensation.
- PECL Mode Operating Range: V_{CC} = 2.375 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = –2.375 V to –3.8 V
- Open Input Default State
- LVDS Input Compatible

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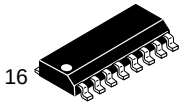
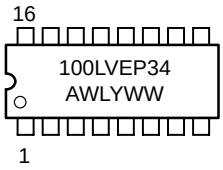
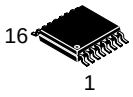
MARKING DIAGRAMS*

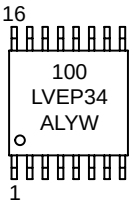


SO–16
D SUFFIX
CASE 751B





TSSOP–16
DT SUFFIX
CASE 948F

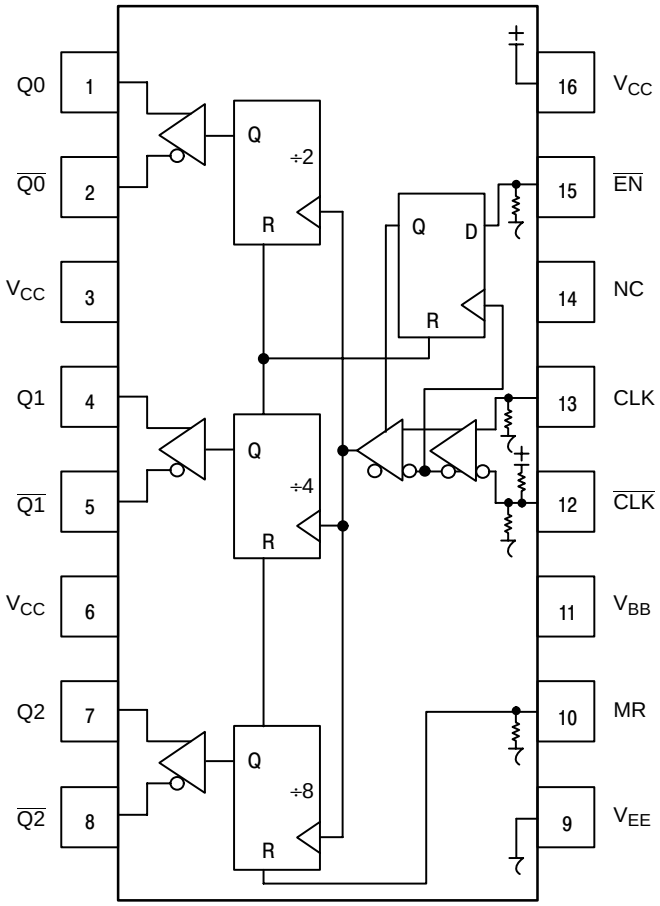


A = Assembly Location
L, WL = Wafer Lot
Y = Year
W, WW = Work Week

*For additional information, refer to Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEP34D	SO–16	48 Units/Rail
MC100LVEP34DR2	SO–16	2500 Units/Reel
MC100LVEP34DT	TSSOP–16	96 Units/Rail
MC100LVEP34DTR2	TSSOP–16	2500 Units/Reel



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 16–Lead Pinout (Top View) **and Logic Diagram**

PIN DESCRIPTION

PIN	FUNCTION
CLK*, $\overline{CLK}$**	ECL Diff Clock Inputs
$\overline{EN}$*	ECL Sync Enable
MR*	ECL Master Reset
Q0, $\overline{Q0}$	ECL Diff ÷2 Outputs
Q1, $\overline{Q1}$	ECL Diff ÷4 Outputs
Q2, $\overline{Q2}$	ECL Diff ÷8 Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

* Pins will default LOW when left open.
** Pins will default to $V_{CC}/2$ when left open.

FUNCTION TABLE

CLK	$\overline{EN}$	MR	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold $Q_{0–3}$
X	X	H	Reset $Q_{0–3}$

Z = Low-to-High Transition
ZZ = High-to-Low Transition

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		37.5 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 200 V > 2 kxV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating Oxygen Index		UL 94 V–0 A @ 0.125 in 28 to 34
Transistor Count		210 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	16 SOIC 16 SOIC	100 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	16 SOIC	33 to 36	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	16 TSSOP 16 TSSOP	138 108	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	16 TSSOP	33 to 36	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

100EP DC CHARACTERISTICS, PECL V_{CC} = 2.5 V, V_{EE} = 0 V (Note 3)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current	40	50	60	40	50	60	42	52	62	mA
V_{OH}	Output HIGH Voltage (Note 4)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{OL}	Output LOW Voltage (Note 4)	555	680	925	555	680	925	555	680	925	mV
V_{IH}	Input HIGH Voltage (Single Ended) (Note 5)	1335		1620	1335		1620	1275		1620	mV
V_{IL}	Input LOW Voltage (Single Ended) (Note 5)	555		875	555		875	555		875	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 5, Note 6)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

3. Input and output parameters vary 1:1 with V_{CC}.
4. All loading with 50 ohms to V_{CC}–2.0 volts.
5. Do not use V_{BB} at V_{CC} < 3.0 V. Single ended input CLK pin operation is limited to $V_{CC} \geq$ 3.0 V in PECL mode.
6. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 7)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	40	50	60	40	50	60	42	52	62	mA
V_{OH}	Output HIGH Voltage (Note 8)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 8)	1355	1570	1725	1355	1570	1725	1355	1570	1725	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1355		1675	1355		1675	1355		1675	mV
V_{BB}	Output Voltage Reference (Note 9)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 10)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

7. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to –0.5 V.
8. All loading with 50 ohms to V_{CC}–2.0 volts.
9. Single ended input CLK pin operation is limited to $V_{CC} \geq$ 3.0 V in PECL mode.
10. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100EP DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = –3.8 V to –2.375 V (Note 11)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	40	50	60	40	50	60	42	52	62	mA
V_{OH}	Output HIGH Voltage (Note 12)	–1145	–1020	–895	–1145	–1020	–895	–1145	–1020	–895	mV
V_{OL}	Output LOW Voltage (Note 12)	–1945	–1700	–1575	–1945	–1700	–1575	–1945	–1700	–1575	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1225		–880	–1225		–880	–1225		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1945		–1625	–1945		–1625	–1945		–1625	mV
V_{BB}	Output Voltage Reference (Note 13)	–1525	–1425	–1325	–1525	–1425	–1325	–1525	–1425	–1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 14)	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

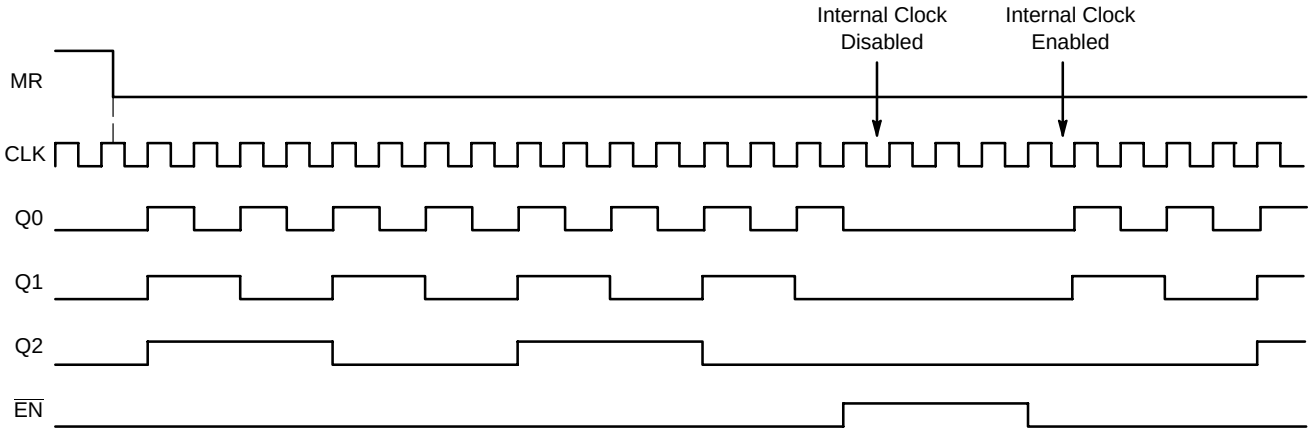
11. Input and output parameters vary 1:1 with V_{CC}.
12. All loading with 50 ohms to V_{CC}–2.0 volts.
13. Single ended input CLK pin operation is limited to $V_{EE} \leq$ –3.0 V in NECL mode.
14. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC CHARACTERISTICS V_{CC}= 0 V; V_{EE}= –3.8 V to –2.375 V or V_{CC}= 2.375 V to 3.8 V; V_{EE}= 0 V (Note 15)

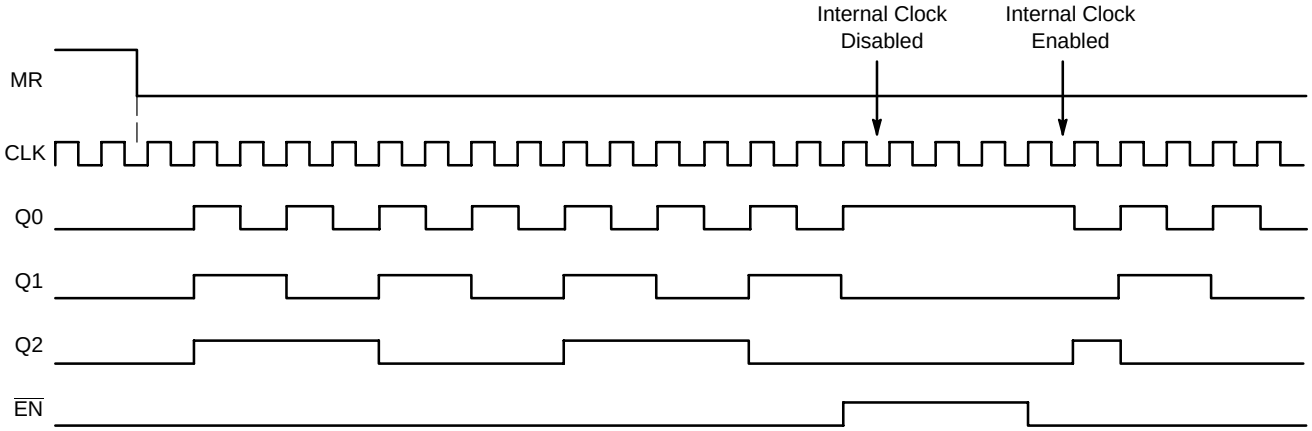
		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (See Figure 4. F_{max}/JITTER)	2.8			2.8			2.8			GHz
t_{PLH} t_{PHL}	Propagation CLK to Q0, Q1, Q2 Delay to Output MR to Q	550 500	650 600	750 700	600 550	700 650	800 750	650 600	750 700	850 800	ps
t_{JITTER}	Cycle–to–Cycle Jitter (See Figure 4. F_{max}/JITTER)		< 1			< 1			< 1		ps
t_S	Setup Time $\overline{EN}$	150	50		150	50		150	50		ps
t_H	Hold Time $\overline{EN}$	200	100		200	100		200	100		ps
t_{RR}	Set/Reset Recovery	300	200		300	200		300	200		ps
V_{PP}	Input Swing (Note 16)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	90	170	200	100	180	250	120	200	280	ps

15. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to V_{CC}–2.0 V.
16. $V_{PP(}$min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

There are two distinct functional relationships between the Master Reset and Clock:



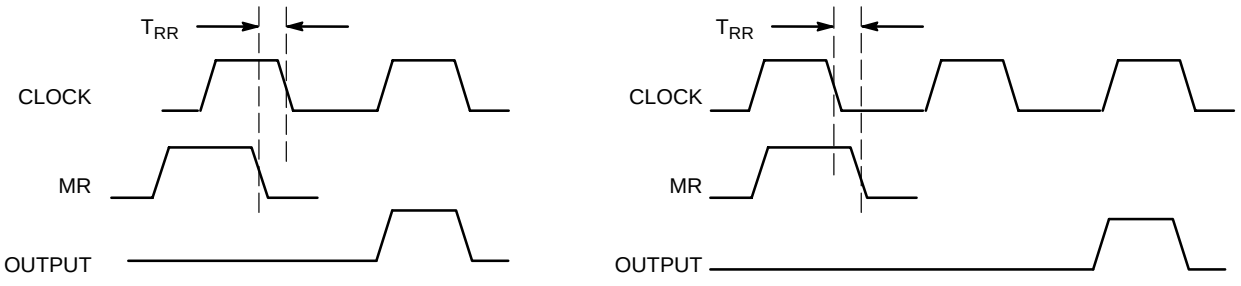
CASE 1: If the MR is de–asserted (L–H), while the Clock is still high, the outputs will follow the first ensuing clock rising edge.



CASE 2: If the MR is de–asserted (L–H), after the Clock has transitioned low, the outputs will follow the second ensuing clock rising edge.

Figure 2. Timing Diagrams

The $\overline{EN}$ signal will freeze the internal clocks to the flip–flops on the first falling edge of CLK after its assertion. The internal dividers will maintain their state during the internal clock freeze and will return to clocking once the internal clocks are unfrozen. The outputs will transition to their next states in the same manner, time and relationship as they would have had the $\overline{EN}$ signal not been asserted.



CASE 1 **CASE 2**

Figure 3. Reset Recovery Time

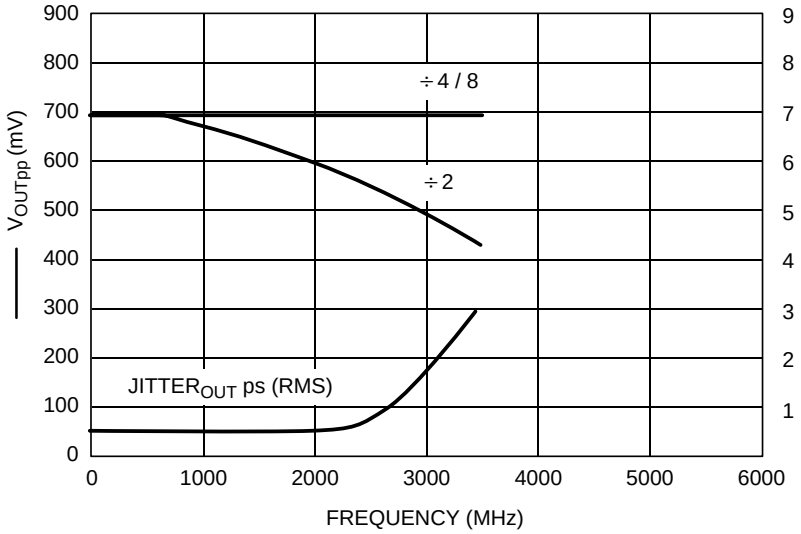


Figure 4. F_{max}/Jitter

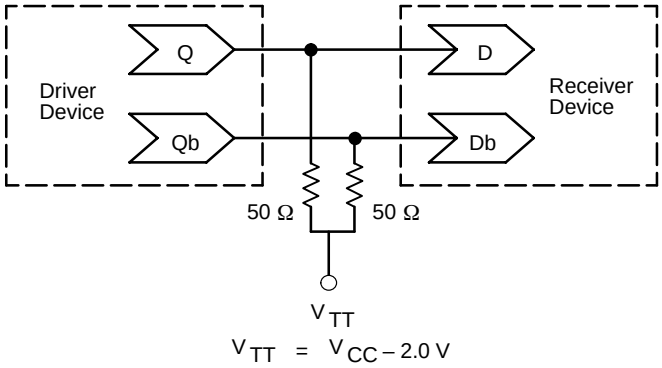


Figure 5. Typical Termination for Output Driver and Device Evaluation
(Refer to Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

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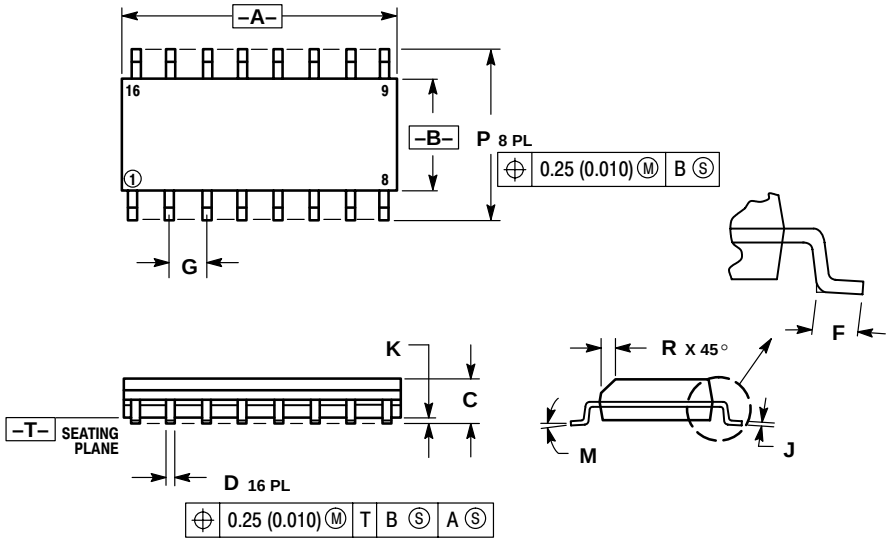
PACKAGE DIMENSIONS

SO–16
D SUFFIX
CASE 751B–05
ISSUE J

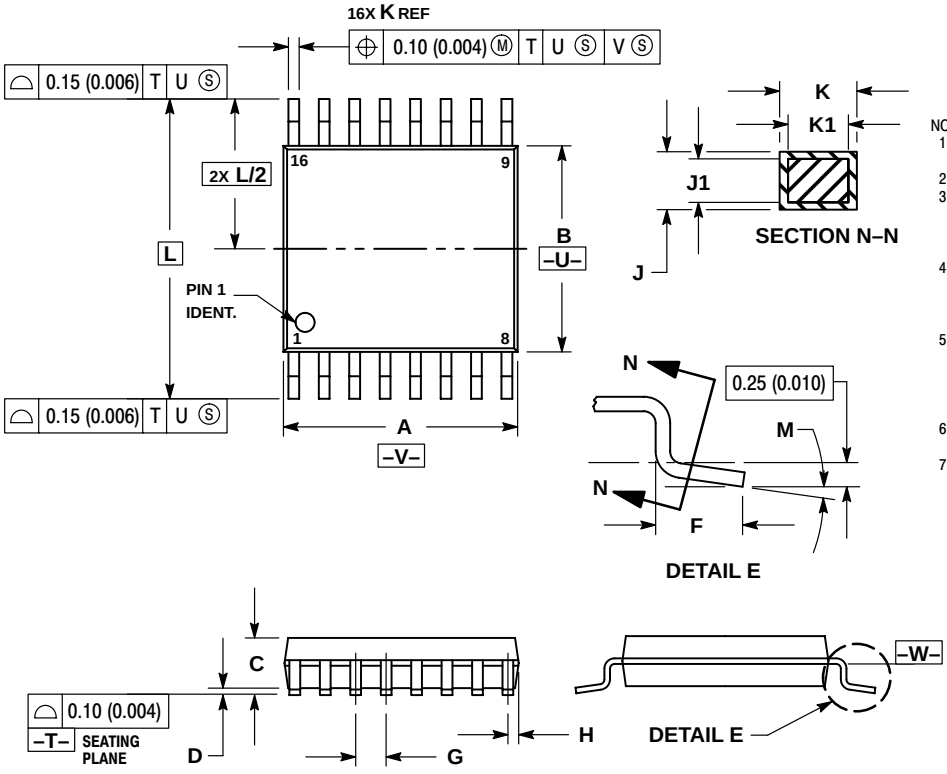


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

TSSOP–16
DT SUFFIX
CASE 948F–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

Notes

Notes

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