CS-8147

10V/5V Low Dropout Dual Regulator with $\overline{\text{ENABLE}}$

Description

The CS-8147 is a 10V/5V dual output linear regulator. The 10V ±.5% output sources 500mA and the 5V ±3% output sources 70mA. The secondary output is inherently stable and does not require an external capacitor.

The on board $\overline{\text{ENABLE}}$ function controls the regulator's two outputs. When $\overline{\text{ENABLE}}$ is high, the regulator is placed in SLEEP mode. Both outputs are disabled and the regulator draws only 70µA of quiescent current.

The regulator is protected against overvoltage conditions. Both outputs are protected against short circuit and thermal runaway conditions.

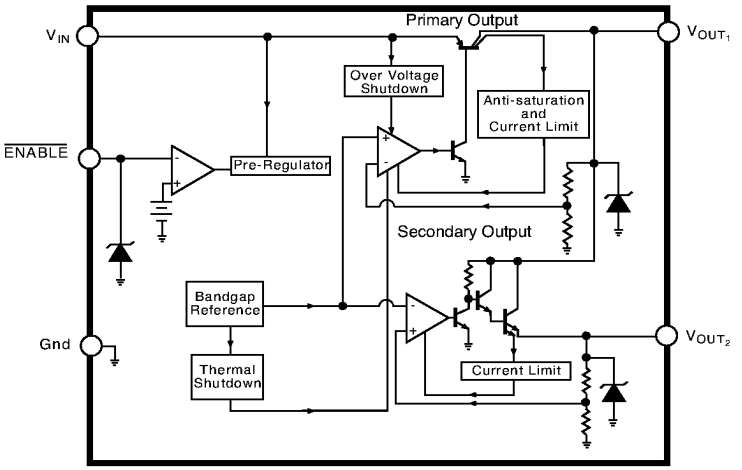
The CS-8147 is packaged in a 5 lead TO-220 with copper tab. The copper tab can be connected to a heat sink if necessary.

Absolute Maximum Ratings

Input Voltage (V_{IN})
- Operating Range ..... -0.5V to 26V
- Overvoltage Protection 60V
- $\overline{\text{ENABLE}}$ Input ..... -0.3 to 10V

Internal Power Dissipation ..... Internally Limited
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature Range ..... -40°C +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature Soldering
- Wave Solder(through hole styles only) ..... 10 sec. max, 260°C peak

Block Diagram

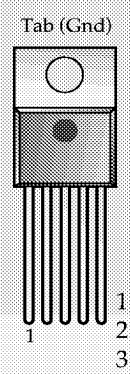


Features

- **Two Regulated Outputs**
  - **10V ± 5%; 500 mA**
  - **5V ± 3%; 70 mA**
- **70µA SLEEP Mode Current**
- **Inherently Stable Secondary Output (No Output Cap Required)**
- **Fault Protection**
  - **Overvoltage Shutdown**
  - **Reverse Battery**
  - **60V Load Dump**
  - **-50V Reverse Transient**
  - **Short Circuit**
  - **Thermal Shutdown**
- **CMOS Compatible $\overline{\text{ENABLE}}$ Input with Low ($I_{OUT(max)}$) Input Current.**

Package Options

TO-220 5 Lead



1 $\overline{\text{ENABLE}}$
2 V_{IN}
3 Gnd
4 V_{OUT_1} (10V)
5 V_{OUT_2} (5V)

Cherry Semiconductor

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Electrical Characteristics for V_O: V_{IN} = 14V, I_{OUT} = 5mA,-40°C < T_J < 150°C, -40°C≤ T_A ≤125°C, $\overline{ENABLE}$ = LOW unless otherwise specified

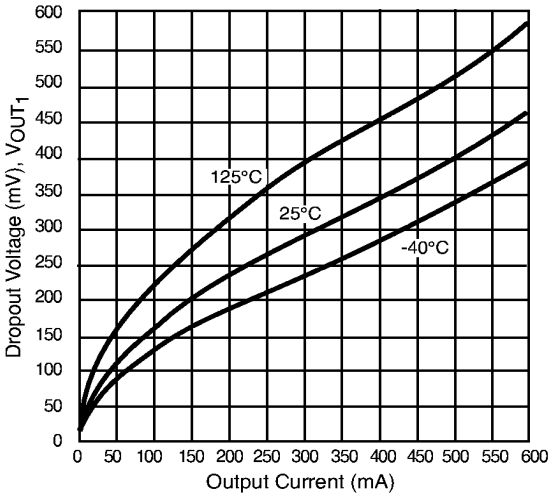
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Primary Output (V_{OUT_1})					
Output Voltage	13V≤V_{IN}≤26V, I_{OUT_1}≤500mA,	9.50	10.00	10.50	V
Dropout Voltage	I_{OUT_1}1=500mA		0.5	0.7	V
Line Regulation	11V≤V_{IN}≤18V, I_{OUT_1}=250mA		15	90	mV
Load Regulation	5mA≤ I_{OUT_1}≤500mA		15	75	mV
Quiescent Current	I_{OUT_1}≤1mA,No Load on V_{OUT_2},V_{IN}=18V I_{OUT_1}=500mA,No Load on V_{OUT_2},V_{IN}=11V		3 60	7 120	mA mA
Quiescent Current	ENABLE=HIGH V_{OUT_1},V_{OUT_2}=OFF		70	200	μA
Current Limit		0.55	0.80		A
Maximum Line Transient	V_{OUT_1}≤13V	60			V
Reverse Polarity Input Voltage, DC	V_{OUT_1}≥-0.6V, 10Ω Load	-18	-30		V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, t=100ms, V_{OUT}≥-6V, 10Ω Load	-50	-80		V
Long Term Stability			50		mV/khr
Over Voltage Shutdown	V_{OUT_1}+V_{OUT2}	32	36	40	V
■ Secondary Output (V_{OUT_2})					
Output Voltage	6V≤V_{IN}≤26V, 1mA≤I_{OUT_2}≤70mA	4.85	5.00	5.15	V
Dropout Voltage	I_{OUT_2}≤70mA		1.5	2.5	V
Line Regulation	11≤V_{IN}≤18V, I_{OUT}=70μA		4	50	mV
Load Regulation	1mA≤I_{OUT_2}≤70mA, V_{IN}-14V		10	50	mV
Current Limit			150		mA
■ $\overline{ENABLE}$ Function ($\overline{ENABLE}$)					
Input $\overline{ENABLE}$ Threshold	V_{OUT_1} On V_{OUT_1} Off	 2.50	1.40 1.40	0.80	V V
Input $\overline{ENABLE}$ Current	Input Voltage Range 0 to 5V	-10		10	μA

Package Pin Description

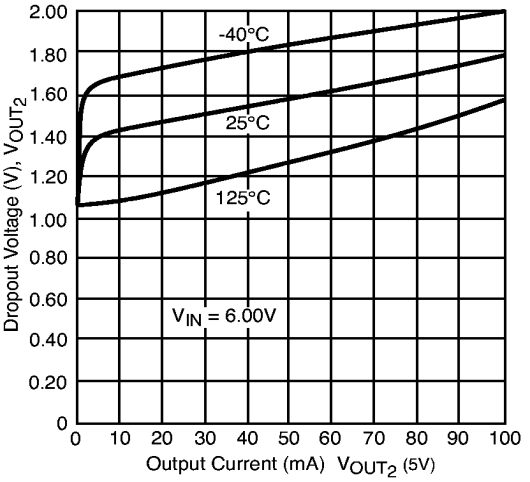
PACKAGE PIN #	PIN SYMBOL	FUNCTION
TO-220		
1	$\overline{ENABLE}$	CMOS compatible input pin; switches V_{OUT_1} and V_{OUT_2} on and off. When $\overline{ENABLE}$ is low, V_{OUT_1} and V_{OUT_2} are active.
2	V_{IN}	Supply voltage, usually direct from battery.
3	Gnd	Ground connection.
4	V_{OUT_1}	Regulated output 10V, 500mA (typ)
5	V_{OUT_2}	Secondary output 5V, 70mA (typ).

Typical Performance Characteristics

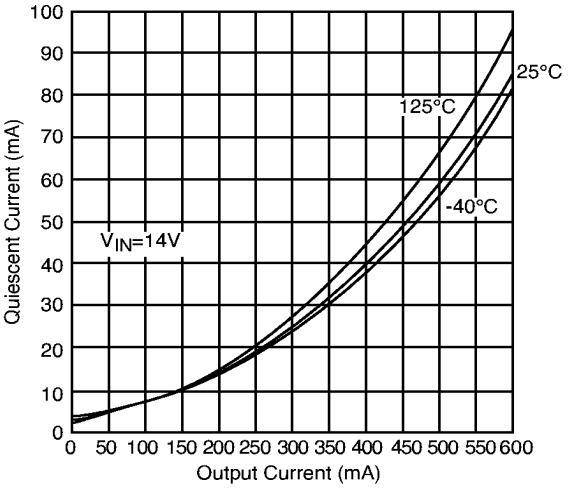
Dropout Voltage vs. Output Current (V_{OUT_1})



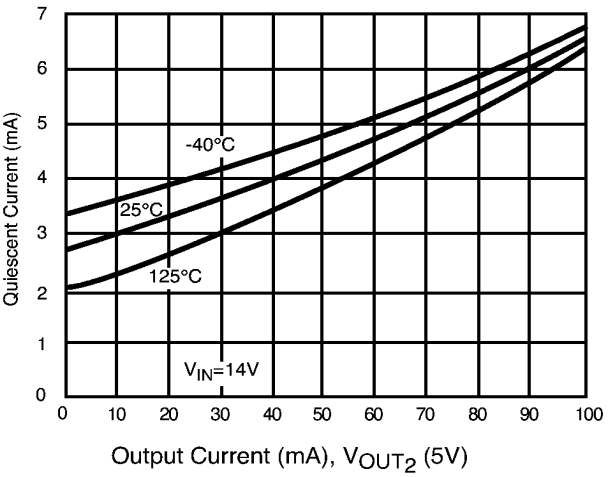
Dropout Voltage vs. Output Current (V_{OUT_2})



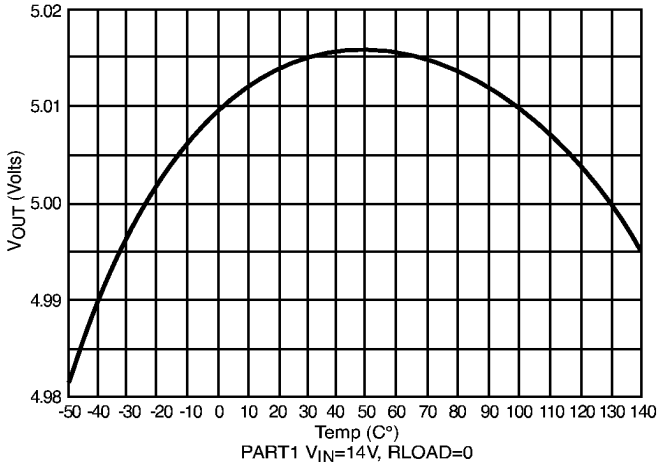
Quiescent Current vs. Output Current (V_{OUT_1})



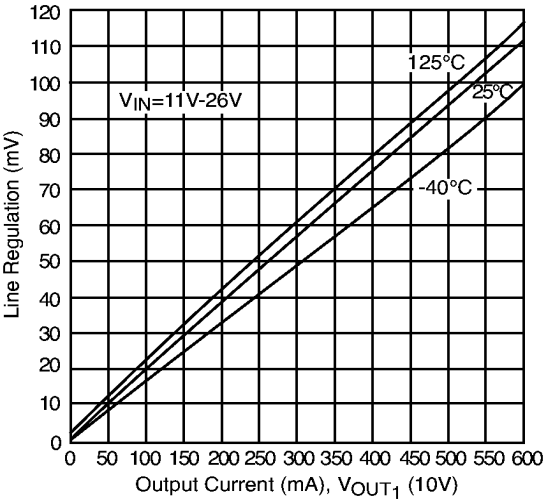
Quiescent Current vs. Output Current (V_{OUT_2})



V_{OUT_2} vs. Temperature

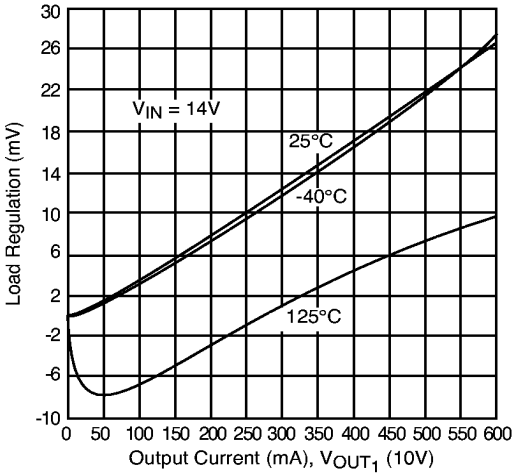


Line Regulation vs. Output Current (V_{OUT_1})

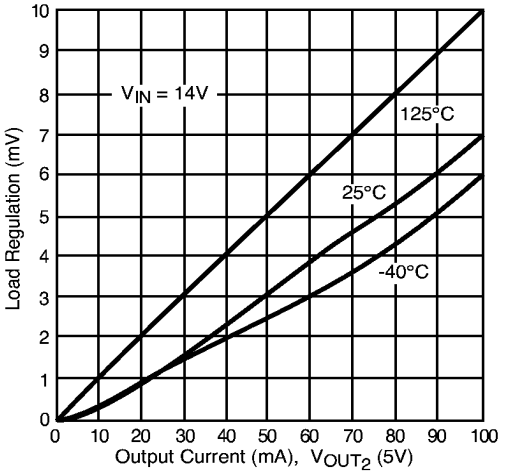


Typical Performance Characteristics

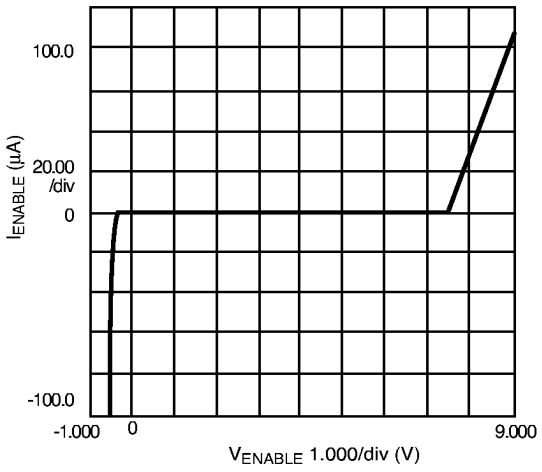
Load Regulation vs. Output Current (V_{OUT_1})



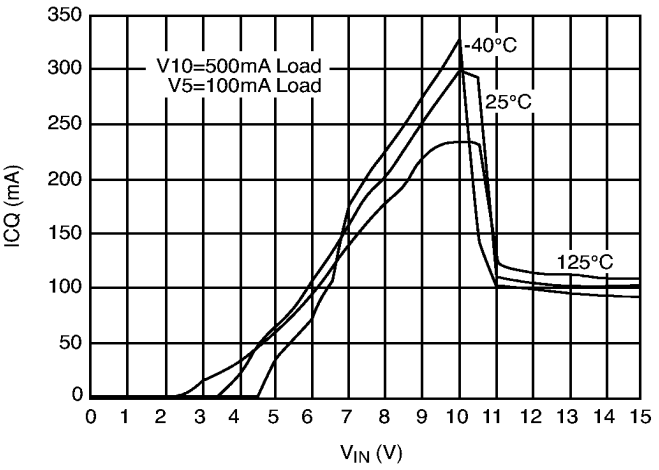
Load Regulation vs. Output Current (V_{OUT_2})



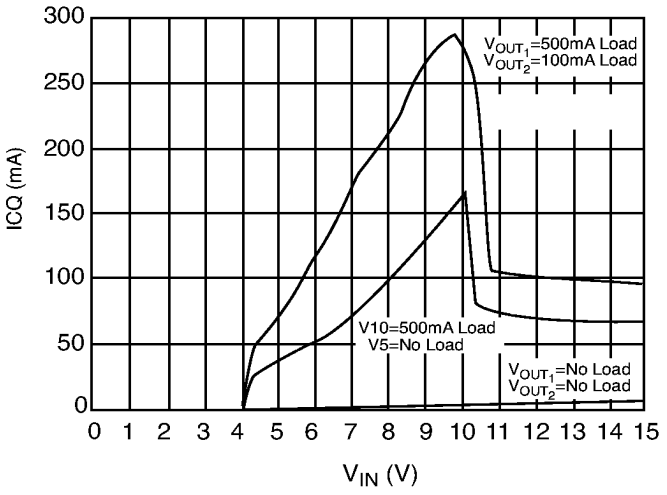
ENABLE Input Current vs. Input Voltage



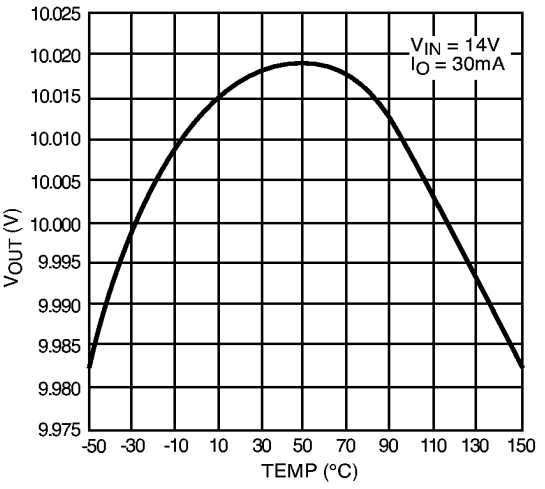
Quiescent Current (I_{GND}) vs. V_{IN} over Temperature



Quiescent Current (I_{GND}) vs. V_{IN} over R_{LOAD}



ENABLE Input Current vs. Input Voltage



Definition of Terms

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Current Limit: Peak current that can be delivered to the output.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

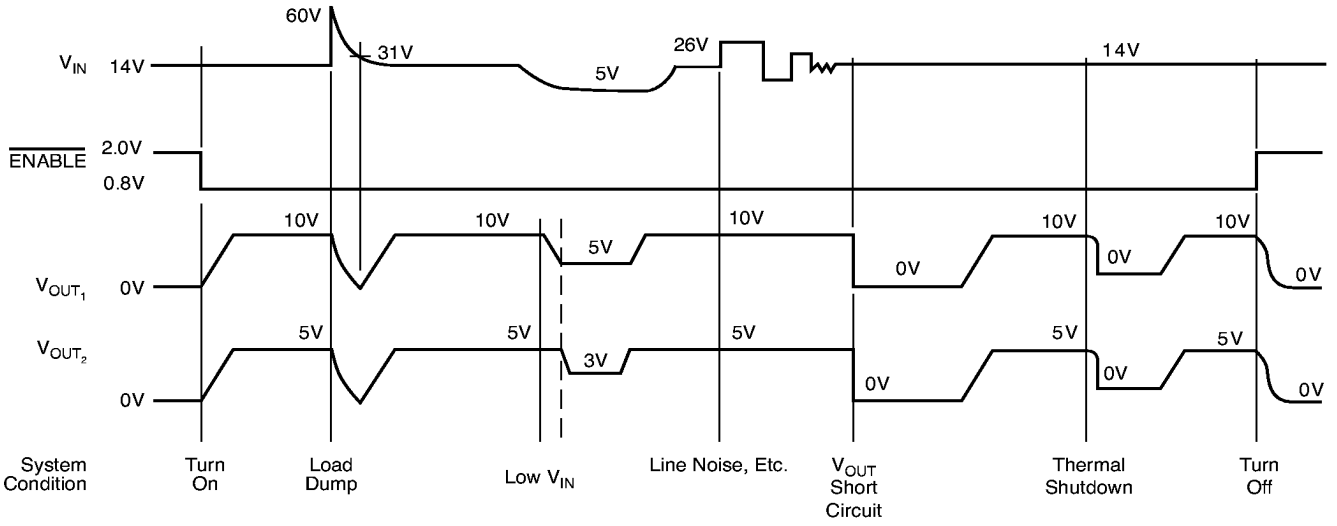
Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

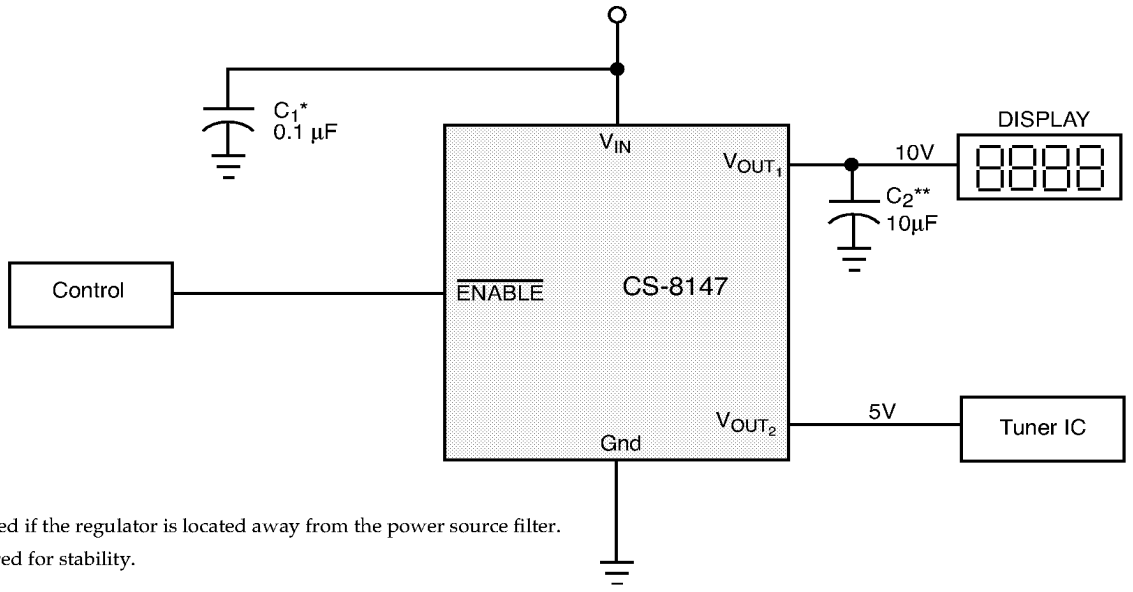
Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_{OUT}: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Typical Circuit Waveform



Test & Applications Circuit



* C_1 is required if the regulator is located away from the power source filter.

**C_2 is required for stability.

Since both outputs are controlled by the same $\overline{\text{ENABLE}}$, the CS-8147 is ideal for applications where a sleep mode is required. Using the CS-8147, a section of circuitry such as a display and nonessential 5V circuits can be shut down under microprocessor control to conserve energy.

The test applications circuit diagram shows an automotive radio application where the display is powered by 10V from V_{OUT1} and the Tuner IC is powered by 5V from V_{OUT_2}. Neither output is required unless both the ignition and the Radio On/OFF switch are on.

Stability Considerations

The secondary output V_{OUT_2} is inherently stable and does not require a compensation capacitor. However an output capacitor connected between V_{OUT_1} and ground is required for stability in most applications.

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (-25°C to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provide this information.

The value for the output capacitor C2 shown in the test and applications circuit should work for most applications, however it is not necessarily the cheapest or best solution.

To determine acceptable value for C2 for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs on the oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. (Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible)

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. (A smaller capacitor will usually cost less and occupy less board space.) If the capacitor oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real work environment. Vary the ESR to reduce ringing.

Step 7: Remove the unit from the environmental chamber and heat the IC with a heat gun. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found for each output, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ±20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitors should be less than 50% of the maximum allowable ESR found in step 3 above.

Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 1) is

$$P_{D(max)} = \{V_{IN(max)} - V_{OUT1(min)}\}I_{OUT_1(max)} + \{V_{IN(max)} - V_{OUT_2(min)}\}I_{OUT_2(max)} + V_{IN(max)}IQ \quad (1)$$

Where

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT_1(min)}$ is the minimum output voltage from V_{OUT_1},

$V_{OUT_2(min)}$ is the minimum output voltage from V_{OUT_2},

$I_{OUT_1(max)}$ is the maximum output current, for the application

$I_{OUT_2(max)}$ is the maximum output current, for the application

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R\Theta_{JA}$ can be calculated:

$$R\Theta_{JA} = \frac{150°C - T_A}{P_D} \quad (2)$$

The value of $R\Theta_{JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R\Theta_{JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

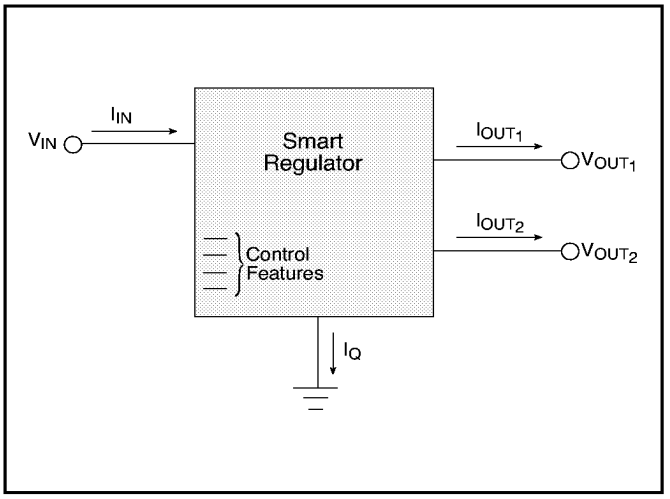


Figure 1: Dual output regulator with key performance parameters labeled.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R\Theta_{JA}$.

$$R\Theta_{JA} = R\Theta_{JC} + R\Theta_{CS} + R\Theta_{SA} \quad (3)$$

where

$R\Theta_{JC}$ = the junction–to–case thermal resistance,
$R\Theta_{CS}$ = the case–to–heatsink thermal resistance, and
$R\Theta_{SA}$ = the heatsink–to–ambient thermal resistance.

$R\Theta_{JC}$ appears in the package section of the data sheet. Like $R\Theta_{JA}$, it too is a function of package type. $R\Theta_{CS}$ and $R\Theta_{SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

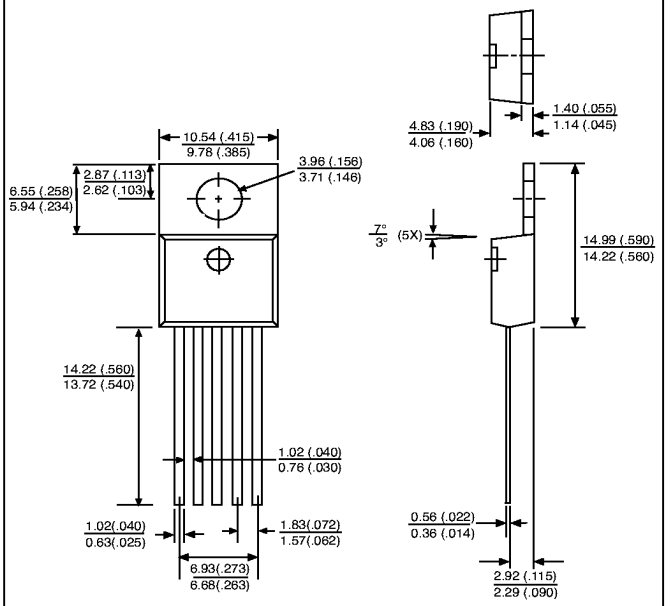
Package Specification

PACKAGE DIMENSIONS IN MM(INCHES)

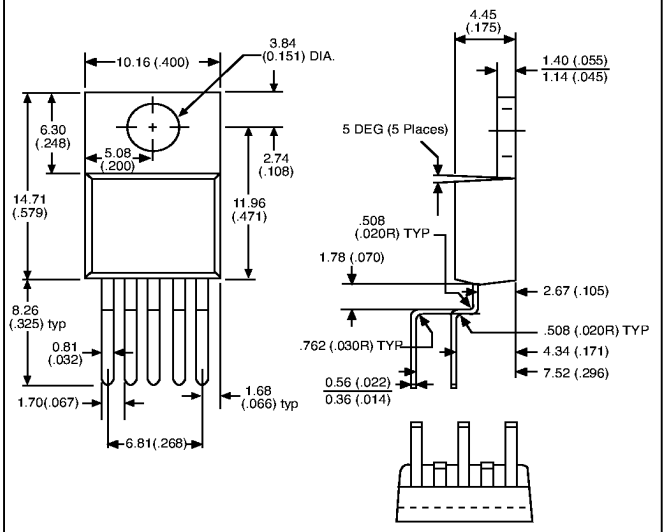
PACKAGE THERMAL DATA

Thermal Data		TO-220	
$R\Theta_{JC}$	typ	2.4	°C/W
$R\Theta_{JA}$	typ	50	°C/W

5 Lead TO-220 (Straight)



5 Lead TO-220 (Vertical)



Ordering Information

Part Number	Description
CS-8147T5	5 Lead TO-220 Straight
CS-8147TV5	5 Lead TO-220 Vertical
CS-8147TH5	5 Lead TO-220 Horizontal

Preliminary

This product is in the preproduction stages of the design process. The data sheet contains preliminary data. CSC reserves the right to make changes to the specifications without notice. Please contact CSC for the latest available information.