CS-8129

5V, 750mA Low Dropout Linear Regulator with Lower $\overline{\text{RESET}}$ Threshold

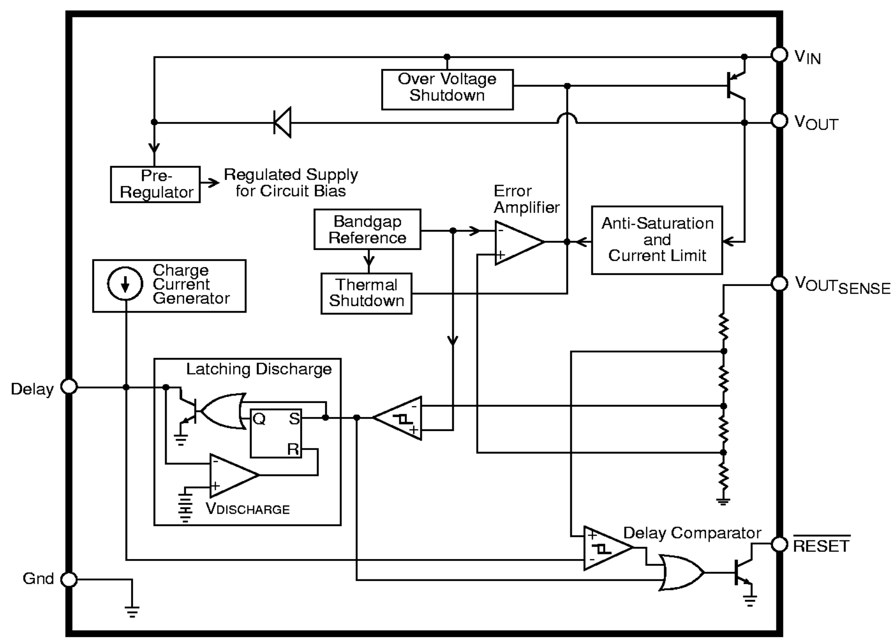
Description

The CS-8129 is a precision 5V linear regulator capable of sourcing 500mA. The $\overline{\text{RESET}}$ threshold voltage has been lowered to 4.2V so that the regulator can be used with 4V microprocessors. The lower $\overline{\text{RESET}}$ threshold also permits operation under low battery conditions (5.5V plus a diode). The $\overline{\text{RESET}}$'s delay time is externally programmed using a discrete RC network. During power up, or when the output goes out of regulation, $\overline{\text{RESET}}$ remains in the low state for the duration of the delay. This function is independent of the input voltage and will function correctly as long as the output voltage remains at or above 1V. Hysteresis is included in the Delay and the $\overline{\text{RESET}}$ comparators to improve noise immunity. A latching discharge circuit is used to discharge the delay capacitor when it is triggered by a brief fault condition.

The regulator is protected against a variety of fault conditions: i.e. reverse battery, overvoltage, short circuit and thermal runaway conditions. The regulator is protected against voltage transients ranging from -50V to +40V. Short circuit current is limited to 1.2A (typ).

The CS-8129 is packaged in a 5 lead TO–220 and a 16 lead surface mount package.

Block Diagram

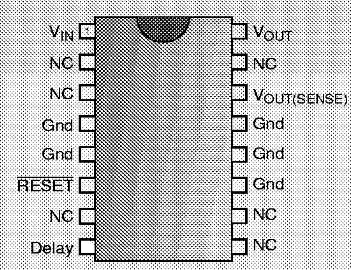


Features

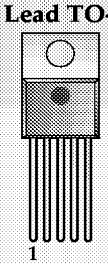
- **5V +/- 3% Regulated Output**
- **Low Dropout Voltage (0.6V @ 0.5A)**
- **500mA Output Current Capability**
- **Reduced $\overline{\text{RESET}}$ Threshold for use with 4V Microprocessors**
- **Externally Programmed $\overline{\text{RESET}}$ Delay**
- **Fault Protection**
  - **Reverse Battery**
  - **60V, 50V Peak Transient Voltage**
  - **Short Circuit**
  - **Thermal Shutdown**

Package Options

16 Lead SOIC Wide



5 Lead TO-220



1 V_{IN}
2 $\overline{\text{RESET}}$
3 Gnd
4 Delay
5 V_{OUT}

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Absolute Maximum Ratings

Input Operating Range .... -0.5 to 26V
Power Dissipation .... Internally Limited
PeakTransient Voltage (46V Load Dump) .... -50V, 60V
Output Current .... Internally Limited
ESD Susceptibility (Human Body Model) 4kV
Operating Temperature .... -40°C to 125°C
Junction Temperature .... -55°C to 150°C
Storage Temperature .... -55°C to 150°C
Lead Temperature Soldering
    Wave Solder (through hole styles only) .... 10 sec. max, 260°C peak
    Reflow (SMD styles only) .... 60 sec. max above 183°C, 230°C peak

Electrical Characteristics: $-40°C \le T_A \le +125°C$, $-40°C \le T_J \le +150°C$, $6V \le V_{IN} \le 26V$, $5mA \le I_{OUT} \le 500mA$, $R_{\overline{RESET}} = 4.7k\Omega$ to V_{OUT} unless otherwise noted*

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ **Output Stage (V_{OUT})**					
Output Voltage		4.85	5.00	5.15	V
Dropout Voltage	$I_{OUT} = 500mA$		0.35	0.60	V
Supply Current	$I_{OUT} \le 10mA$ $I_{OUT} \le 100mA$ $I_{OUT} \le 500mA$		2 6 55	7 12 100	mA
Line Regulation	$6V \le V_{IN} \le 26V$, $I_{OUT} = 50mA$		5	50	mV
Load Regulation	$50mA \le I_{OUT} \le 500mA$, $V_{IN} = 14V$		10	50	mV
Ripple Rejection	f = 120Hz, V_{IN} = 7 to 17V, $I_{OUT} = 250mA$	54	75		dB
Current Limit		0.75	1.20		A
Overvoltage Shutdown		32		40	V
Reverse Polarity Input Voltage DC	$V_{OUT} \ge -0.6V$, 10Ω Load	-15	-30		V
■ **$\overline{RESET}$ and Delay Functions**					
Delay Charge Current	$V_{DELAY} = 2V$	5	10	15	µA
$\overline{RESET}$ Threshold	V_{OUT} Increasing, $V_{RT(ON)}$ V_{OUT} Decreasing, $V_{RT(OFF)}$	4.05 4.00	4.35 4.20	4.50 4.45	V V
$\overline{RESET}$ Hysteresis	$V_{RH}=V_{RT(ON)} - V_{RT(OFF)}$	50	150	250	mV
Delay Threshold	Charge, $V_{DC(HI)}$ Discharge, $V_{DC(LO)}$	3.25 2.85	3.50 3.10	3.75 3.35	V V
Delay Hysteresis		200	400	800	mV
$\overline{RESET}$ Output Voltage Low	$1V < V_{OUT} < V_{RT(L)}$, 3kΩ to V_{OUT}		0.1	0.4	V
$\overline{RESET}$ Output Leakage Current	$V_{OUT} > V_{RT(H)}$		0	10	µA
Delay Capacitor Discharge Voltage	Discharge Latched "ON", $V_{OUT} > V_{RT}$		0.2	0.5	V
Delay Time	$C_{DELAY} = 0.1\mu F$ (Note 1)	16	32	48	ms

* To observe safe operating junction temperatures, low duty cycle pulse testing is used in tests where applicable.

$$\text{Delay Time} = \frac{C_{Delay} \times V_{Delay\ Threshold\ Charge}}{I_{Charge}} = C_{Delay} \times 3.5 \times 10^5 \text{ (typ)}$$

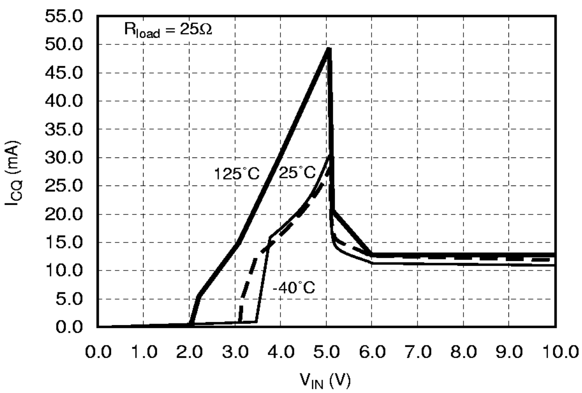
Note 1: assuming ideal capacitor

Package Lead Description

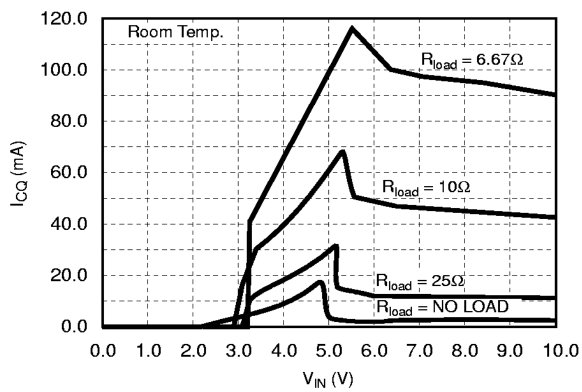
PACKAGE LEAD #		LEAD SYMBOL	FUNCTION
16L SOIC Wide	**5L TO-220**		
1	1	V_{IN}	Unregulated supply voltage to IC.
16	5	V_{OUT}	Regulated 5V output.
4, 5, 11, 12, 13	3	Gnd	Ground connection.
8	4	Delay	Timing capacitor for $\overline{RESET}$ function.
6	2	$\overline{RESET}$	CMOS/TTL compatible output lead. $\overline{RESET}$ goes low whenever V_{OUT} drops below 6% of it's regulated value.
14	N/A	$V_{OUT(SENSE)}$	Remote sensing of output voltage.

Typical Performance Characteristics

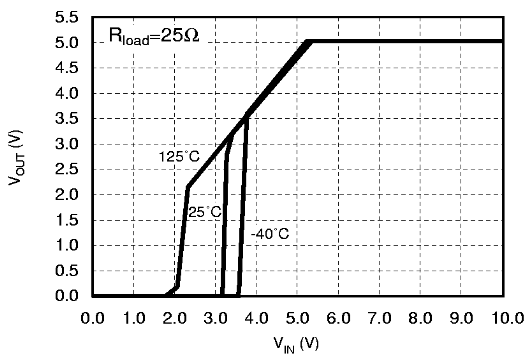
Quiescent Current vs Input Voltage over Temperature



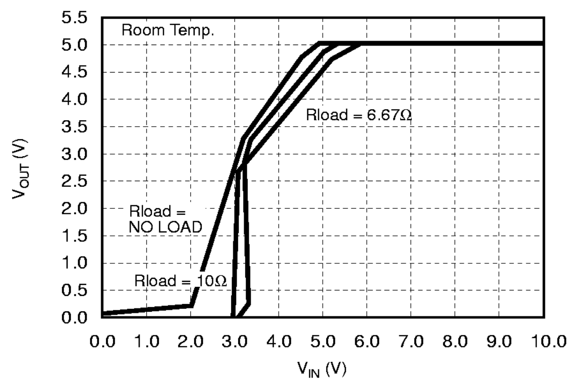
Quiescent Current vs Input Voltage over Load Resistance



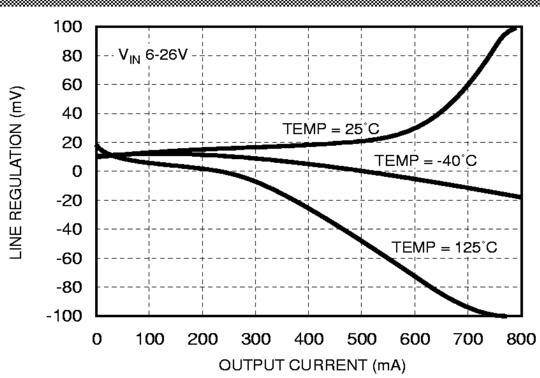
Output Voltage vs Input Voltage over Temperature



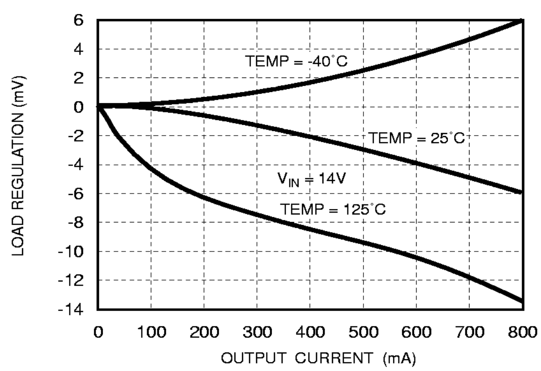
V_{OUT} vs. V_{IN} over R_{LOAD}



Line Regulation vs. Output Current

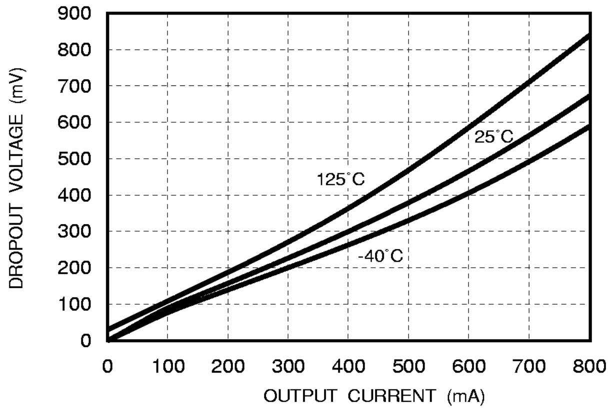


Load Regulation vs. Output Current

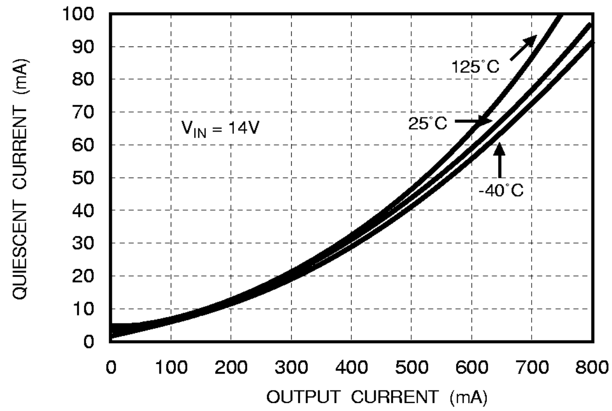


Typical Performance Characteristics Continued

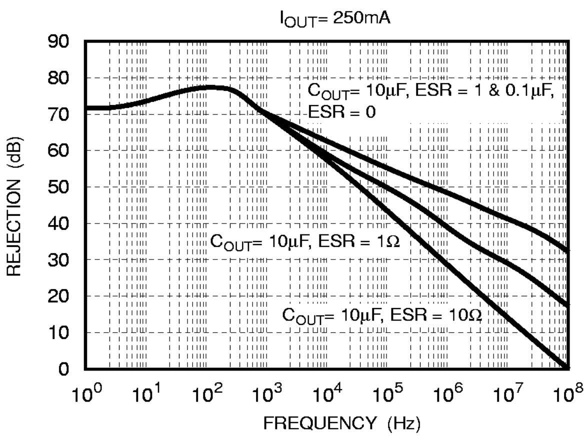
Dropout Voltage vs. Output Current



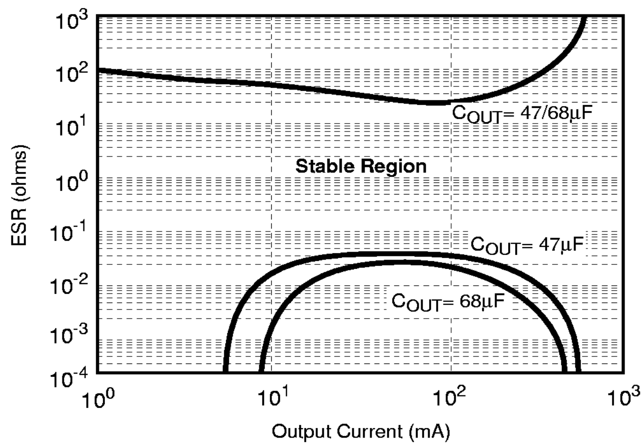
Quiescent Current vs. Output Current



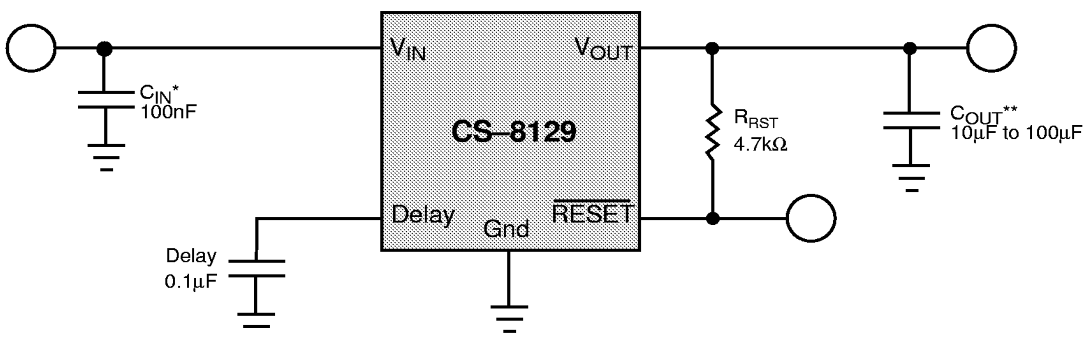
Ripple Rejection



Output Capacitor ESR



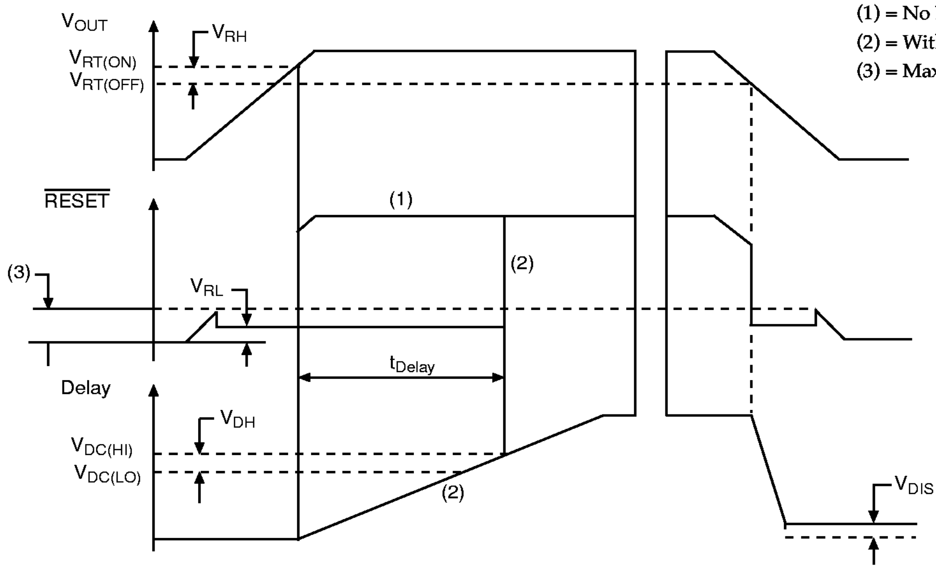
Test & Application Circuit



*C_{IN} required if regulator is far from the power source filter.

**C_{OUT} required for stability.

RESET Circuit Waveform



RESET Circuit Functional Description

The CS-8129 RESET function has hysteresis on both the reset and delay comparators, a latching Delay capacitor discharge circuit, and operates down to 1V.

The RESET circuit output is an open collector type with ON and OFF parameters as specified. The RESET output NPN transistor is controlled by the two circuits described (see Block Diagram).

Low Voltage Inhibit Circuit

This circuit monitors output voltage, and when output voltage is below the specified minimum causes the RESET output transistor to be in the ON (saturation) state. When the output voltage is above the specified level, this circuit permits the RESET output transistor to go into the OFF state if allowed by the RESET Delay circuit.

Reset Delay Circuit

This circuit provides a programmable (by external capacitor) delay on the RESET output lead. The Delay lead provides source current to the external delay capacitor only when the "Low Voltage Inhibit" circuit indicates that output voltage is above $V_{RT(ON)}$. Otherwise, the Delay lead sinks current to ground (used to discharge the delay capacitor). The discharge current is latched ON when the output voltage is below $V_{RT(OFF)}$. The Delay capacitor is fully discharged anytime the output voltage falls out of regulation, even for a short period of time. This feature ensures a controlled RESET pulse is generated following detection of an error condition. The circuit allows the RESET output transistor to go to the OFF (open) state only when the voltage on the Delay lead is higher than $V_{DC(HI)}$.

The Delay time for the RESET function is calculated from the formula:

$$\text{Delay time} = \frac{C_{Delay} \times V_{Delay\ Threshold}}{I_{Charge}}$$

$$\text{Delay time} = C_{Delay(\mu F)} \times 3.2 \times 10^5$$

If C_{Delay}=0.1μF, Delay time (ms)=32ms ± 50%: i.e. 16ms to 48ms. The tolerance of the capacitor must be taken into account to calculate the total variation in the delay time.

Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (-25°C to -40°C), both the value and ESR of the least expensive will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor C_{OUT} shown in the test and applications circuit should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for C_{OUT} for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Remove the unit from the environmental chamber and heat the IC with a heat gun. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of +/- 20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 1) is:

$$P_{D(max)} = \{V_{IN(max)} - V_{OUT(min)}\} I_{OUT(max)} + V_{IN(max)} I_Q \qquad (1)$$

where

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150°C - T_A}{P_D} \qquad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

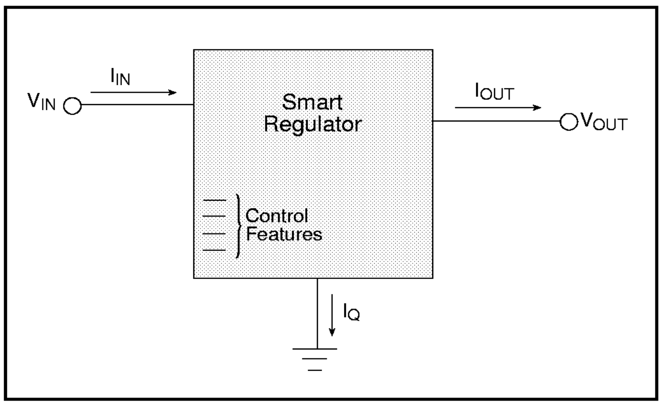


Figure 1: Single output regulator with key performance parameters labeled.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$.

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

where

$R_{\Theta JC}$ = the junction–to–case thermal resistance,
$R_{\Theta CS}$ = the case–to–heatsink thermal resistance, and
$R_{\Theta SA}$ = the heatsink–to–ambient thermal resistance.

$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it too is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

Package Specification

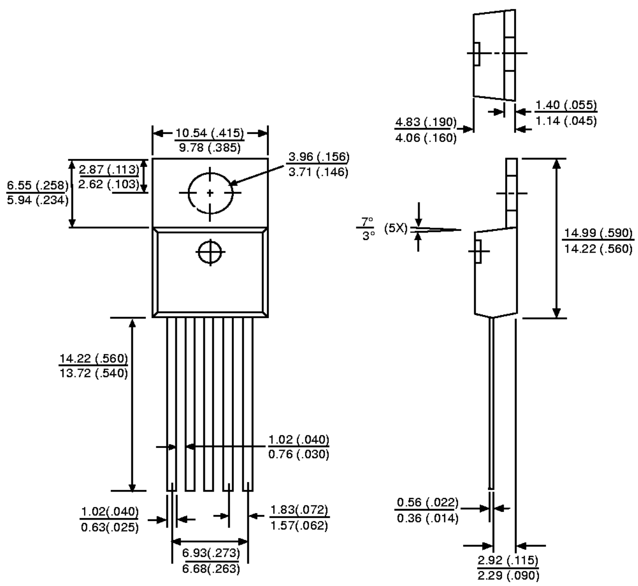
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16 L SOIC Wide	10.46	10.21	.412	.402

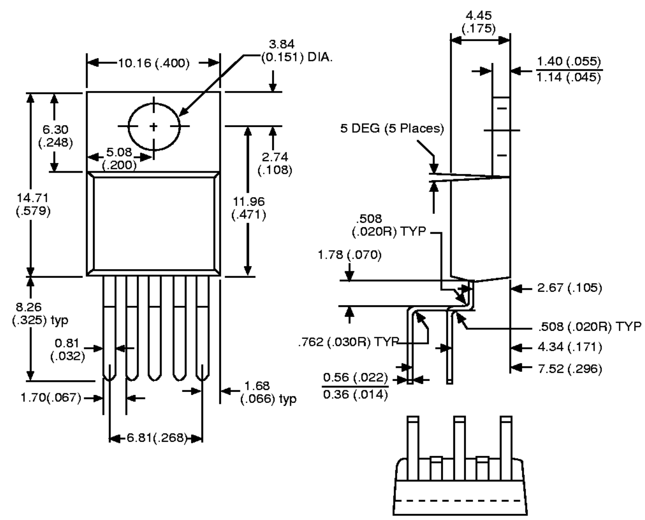
PACKAGE THERMAL DATA

Thermal Data		16 Lead SOIC Wide	5 Lead TO-220	
$R_{\Theta JC}$	typ	23	2.1	°C/W
$R_{\Theta JA}$	typ	105	50	°C/W

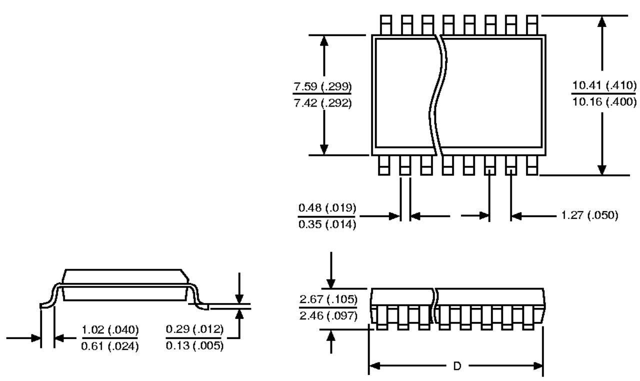
TO-220 (Straight)



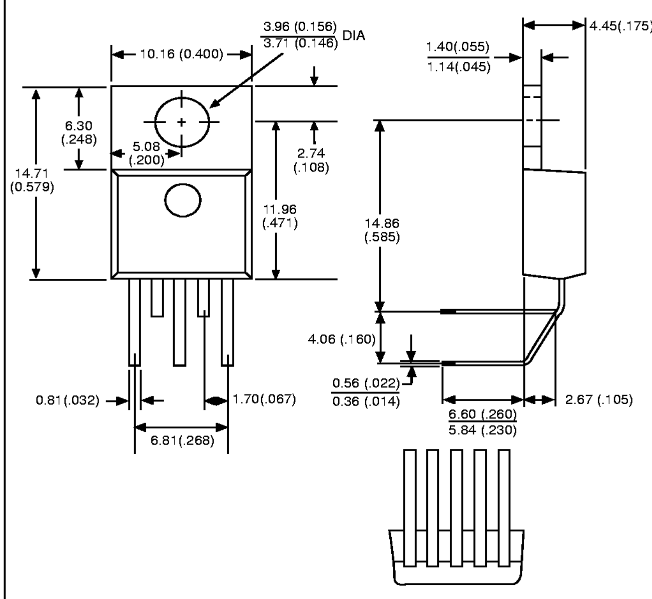
5 Lead TO-220 (Vertical)



SO Wide



5 Lead TO-220 (Horizontal)



Ordering Information

Part Number	Description
CS-8129DW16	16 Lead SOIC Wide
CS-8129T5	5 Lead TO-220 Straight
CS-8129TH5	5 Lead TO-220 Horizontal
CS-8129TV5	5 Lead TO-220 Vertical
CS-8129DWR16	16 Lead SOIC Wide Tape & Reel

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