

Advance Information

Description

The μPD4216410 and the μPD4217410 are fast-page dynamic RAMs with write per-bit organized as 4,194,304 words by 4 bits and designed to operate from a single +5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{\text{CAS}}$ independent of $\overline{\text{RAS}}$. After a valid read or read-modify-write cycle, data is held on the outputs by holding $\overline{\text{CAS}}$ low. The data output is returned to high impedance by returning $\overline{\text{CAS}}$ high. Fast-page read and write cycles can be executed by cycling $\overline{\text{CAS}}$.

Refreshing may be accomplished by a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by $\overline{\text{RAS}}$ -only refresh cycles or by normal read or write cycles.

Two versions of the 4,194,304 by 4-bit fast-page dynamic RAM with write-per-bit are available. The μPD4216410 version uses 4096 address combinations of $A_0 - A_{11}$ to refresh the memory during a 64-ms refresh period. The μPD4217410 version uses 2048 address combinations of $A_0 - A_{10}$ to refresh the memory during a 32-ms refresh period.

To access the memory during read, write, and read-modify-write cycles, the μPD4216410 uses row address combinations of $A_0 - A_{11}$ and column address combinations of $A_0 - A_9$. The μPD4217410 uses row and column address combinations of $A_0 - A_{10}$.

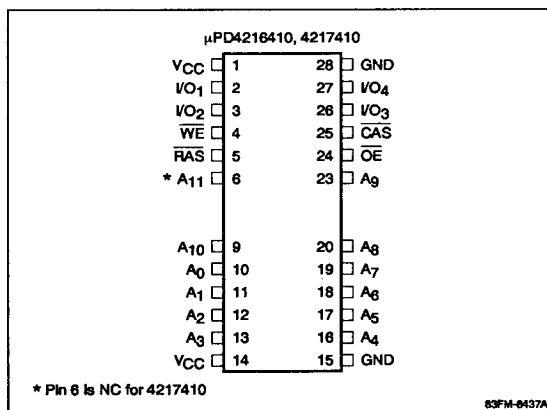
Features

- 4,194,304 by 4-bit organization
- Single +5-volt power supply
- Fast-page option with write-per-bit
- Low power dissipation
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles

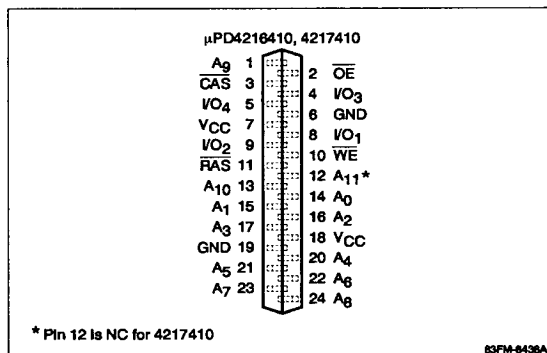
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 4096 refresh cycles every 64 ms (4216410); 2048 refresh cycles every 32 ms (4217410)
- 28/24-pin plastic SOJ (400 mil), 24-pin plastic ZIP (475 mil), and 28/24-pin plastic TSOP packaging

Pin Configurations

28/24-Pin Plastic SOJ



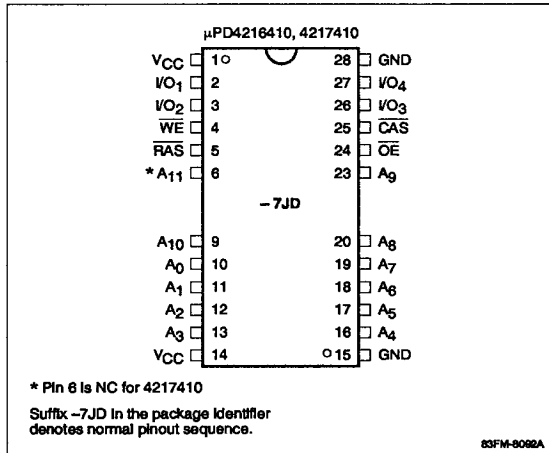
24-Pin Plastic ZIP



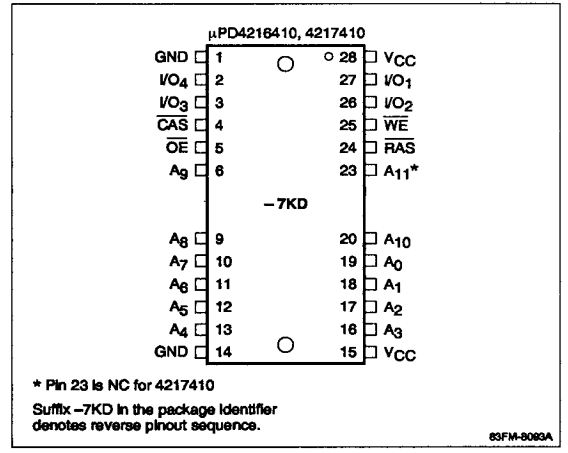
Contact your NEC sales representative for complete data sheet and product availability.

Pin Configurations (cont)

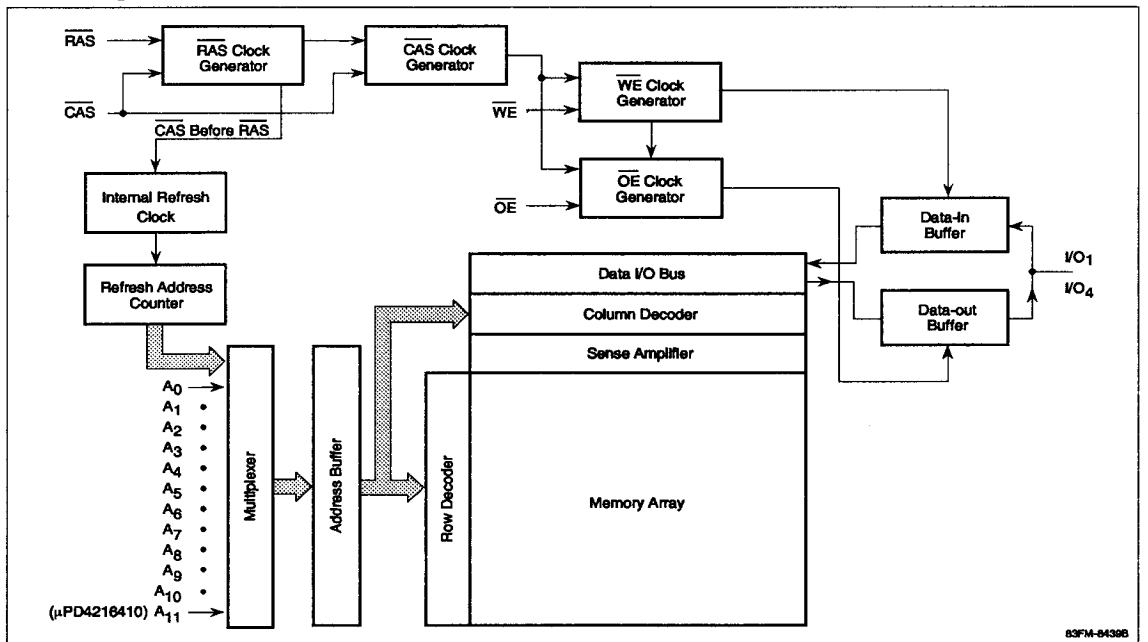
28/24-Pin Plastic TSOP (Normal Pinouts)



28/24-Pin Plastic TSOP (Reverse Pinouts)



Block Diagram



Ordering Information, μPD4216410 (4096 refresh cycles)

Part Number	RAS Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD4216410LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	45 ns	
LE-80	80 ns	150 ns	50 ns	
LE-10	100 ns	180 ns	60 ns	
μPD4216410V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
V-70	70 ns	130 ns	45 ns	
V-80	80 ns	150 ns	50 ns	
V-10	100 ns	180 ns	60 ns	
μPD4216410G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	45 ns	
G5-80	80 ns	150 ns	50 ns	
μPD4216410G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	45 ns	
G5M-80	80 ns	150 ns	50 ns	

Ordering Information, μPD4217410 (2048 refresh cycles)

Part Number	RAS Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD4217410LE-60	60 ns	110 ns	40 ns	28/24-pin plastic SOJ (400 mil)
LE-70	70 ns	130 ns	45 ns	
LE-80	80 ns	150 ns	50 ns	
LE-10	100 ns	180 ns	60 ns	
μPD4217410V-60	60 ns	110 ns	40 ns	24-pin plastic ZIP
V-70	70 ns	130 ns	45 ns	
V-80	80 ns	150 ns	50 ns	
V-10	100 ns	180 ns	60 ns	
μPD4217410G5-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (normal pinouts)
G5-70	70 ns	130 ns	45 ns	
G5-80	80 ns	150 ns	50 ns	
μPD4217410G5M-60	60 ns	110 ns	40 ns	28/24-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns	130 ns	45 ns	
G5M-80	80 ns	150 ns	50 ns	