NEC

MOS INTEGRATED CIRCUIT

μPD16835A

MONOLITHIC QUAD H BRIDGE DRIVER CIRCUIT

DESCRIPTION

The μPD16835A is a monolithic quad H bridge driver IC that employs a CMOS control circuit and a MOS FET output circuit. Because it uses MOS FETs in its output stage, this driver IC consumes less power than conventional driver ICs that use bipolar transistors.

Because the μPD16835A controls a motor by inputting serial data, its package has been shrunk and the number of pins reduced. As a result, the performance of the application set can be improved and the size of the set has been reduced.

The μPD16835A employs a current-controlled 64-step micro step driving method that drives stepper motor with low vibration.

The μPD16835A is housed in a 38-pin plastic shrink SOP to contribute to the miniaturization of the application set.

The μPD16835A can simultaneously drive two stepper motors and is ideal for the mechanisms of camcorders.

FEATURES

- Four H bridge circuits employing power MOS FETs
- Current-controlled 64-step micro step driving
- Motor control by serial data (8 bytes x 8 bits) (original oscillation: 4-MHz input)
  Data is input with the LSB first.
  EVR reference setting voltage: 100 to 250 mV (@V_{REF} = 250 mV) ... 4-bit data input (10-mV step)
  Chopping frequency: 32 to 124 kHz ... 5-bit data input (4-kHz step)
  Original oscillation division or internal oscillation selectable
  Number of pulses in 1 V_D: 0 to 252 pulses ... 6 bits + 2-bit data input (4 pulses/step)
  Step cycle: 0.25 to 8191.75 μs ... 15-bit data input (0.25- μs step)
- 3-V power supply. Minimum operating voltage: 2.7 V (MIN.)
- Low current consumption I_{DD}: 3.0 mA (MAX.), $I_{DD\ (RESET)}$: 100 μA (MAX.), $I_{MO(RESET)}$: 1.0 μA (MAX.)
- 38-pin plastic shrink SOP (7.62 mm (300))

ORDERING INFORMATION

Part number	Package
μPD16835AGS-BGG	38-pin plastic shrink SOP (7.62 mm (300))

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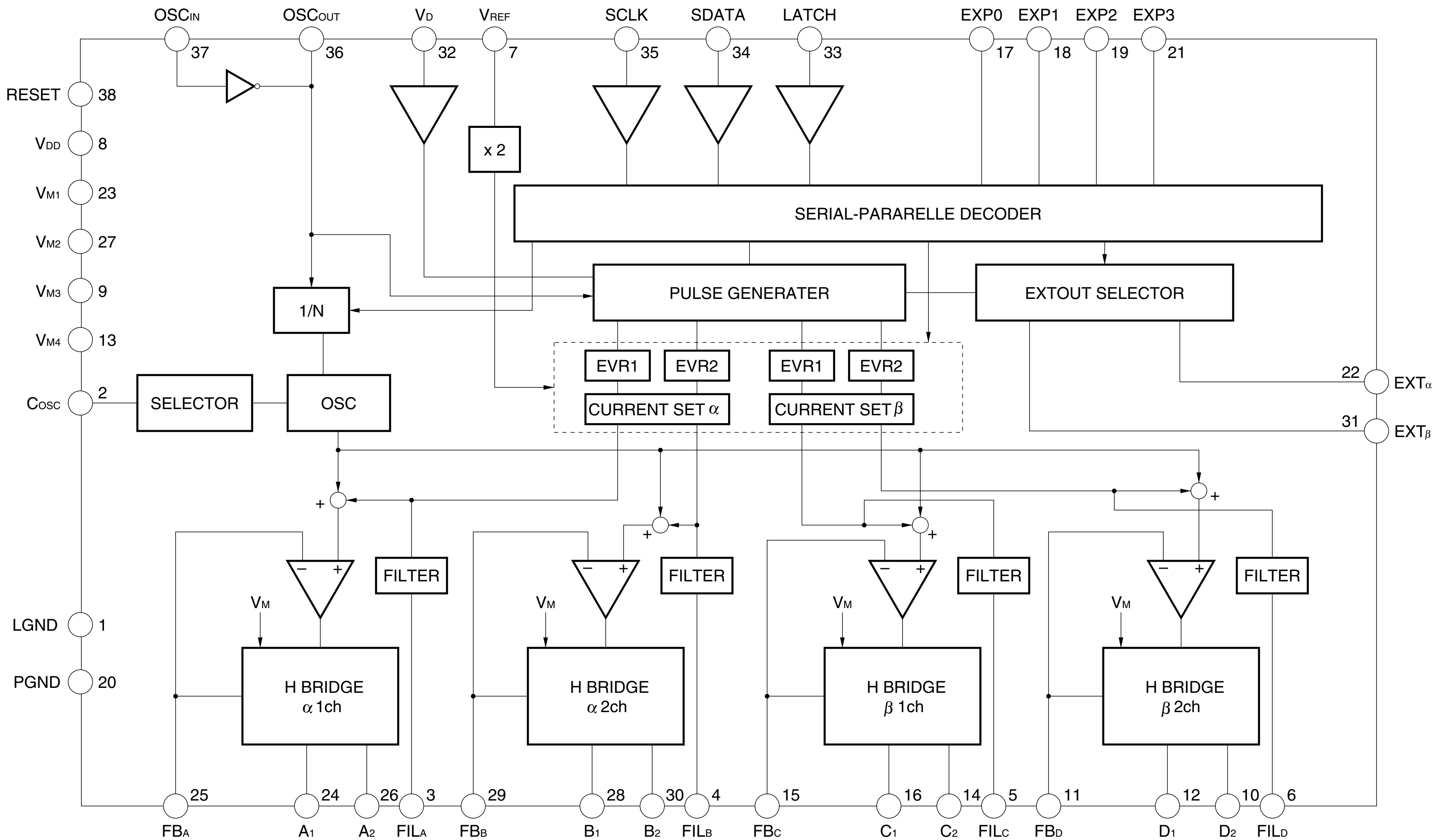
BLOCK DIAGRAM



PIN CONFIGURATION

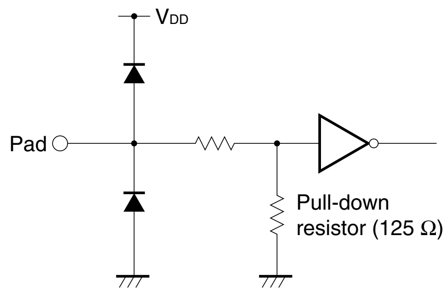
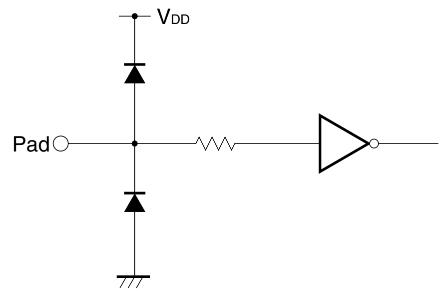
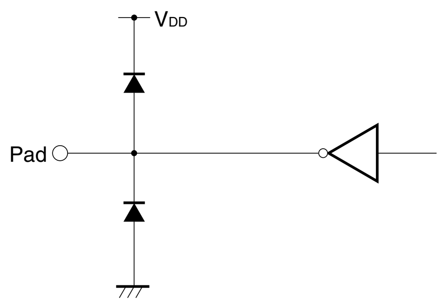
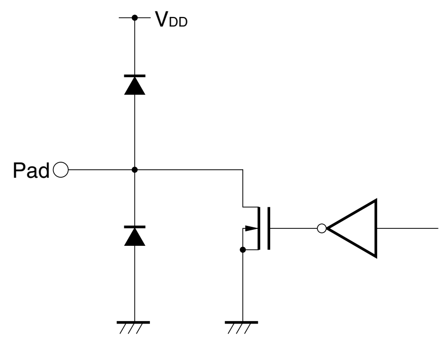
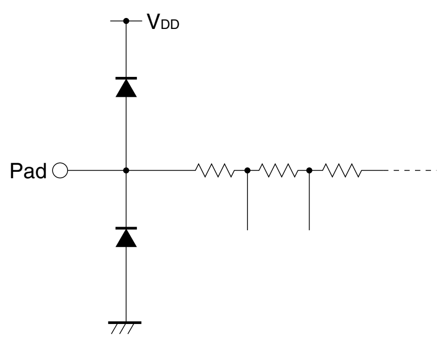
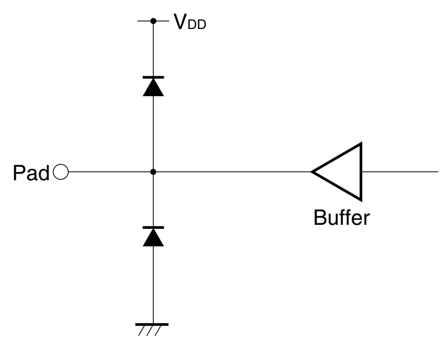
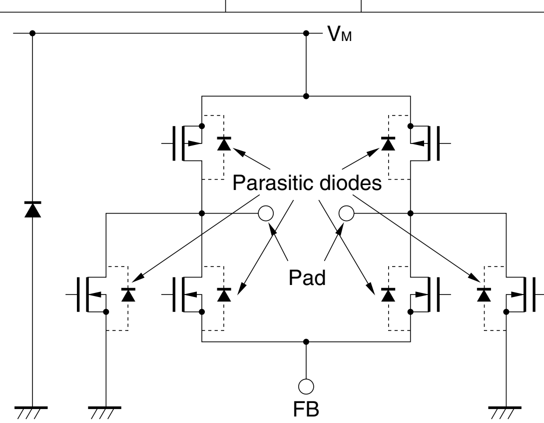
38-pin plastic shrink SOP (7.62 mm (300))

1	LGND	RESET	38
2	C_{OSC}	OSC_{OUT}	37
3	FIL_A	OSC_{IN}	36
4	FIL_B	SCLK	35
5	FIL_C	SDATA	34
6	FIL_D	LATCH	33
7	V_{REF}	V_D	32
8	V_{DD}	EXT_β	31
9	V_{M3}	B_2	30
10	D_2	FB_B	29
11	FB_D	B_1	28
12	D_1	V_{M2}	27
13	V_{M4}	A_2	26
14	C_2	FB_A	25
15	FB_C	A_1	24
16	C_1	V_{M1}	23
17	EXP0	EXT_α	22
18	EXP1	EXP3	21
19	EXP2	PGND	20

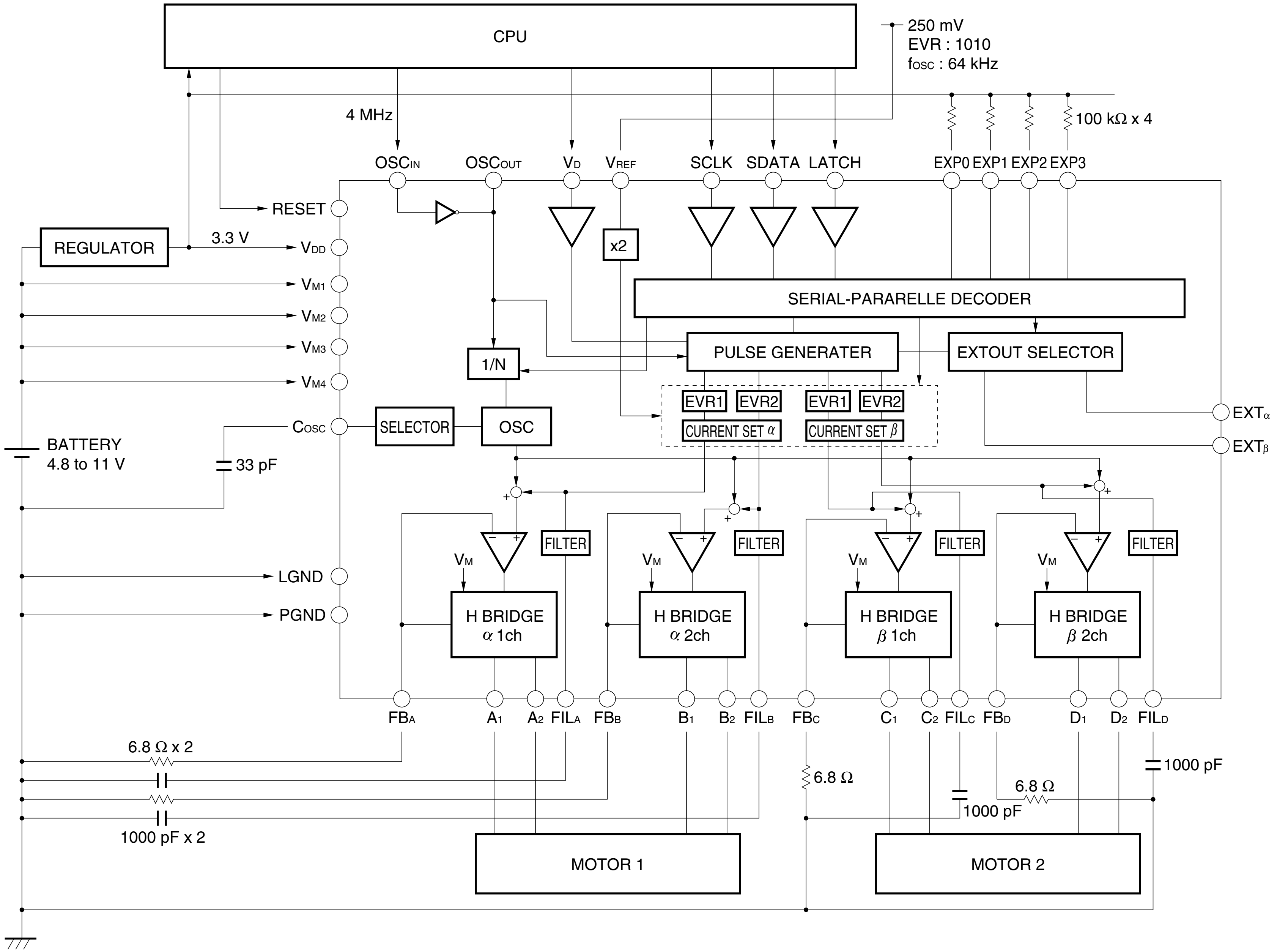
1. PIN FUNCTIONS

Pin No.	Symbol	Function
1	LGND	Control circuit GND pin
2	C_{OSC}	Chopping capacitor connection pin
3	FIL_A	α 1-ch filter capacitor connection pin (1000 pF TYP.)
4	FIL_B	α 2-ch filter capacitor connection pin (1000 pF TYP.)
5	FIL_C	β 1-ch filter capacitor connection pin (1000 pF TYP.)
6	FIL_D	β 2-ch filter capacitor connection pin (1000 pF TYP.)
7	V_{REF}	Reference voltage input pin (250 mV TYP.)
8	V_{DD}	Control circuit supply voltage input pin
9	V_{M3}	Output circuit supply voltage input pin
10	D_2	β 2-ch output pin
11	FB_D	β 2-ch sense resistor connection pin
12	D_1	β 2-ch output pin
13	V_{M4}	Output circuit supply voltage connection pin
14	C_2	β 1-ch output pin
15	FB_C	β 1-ch sense resistor connection pin
16	C_1	β 1-ch output pin
17	EXP0	Output monitor pin (open drain)
18	EXP1	Output monitor pin (open drain)
19	EXP2	Output monitor pin (open drain)
20	PGND	Power circuit GND pin
21	EXP3	Output monitor pin (open drain)
22	EXT_α	Logic circuit monitor pin
23	V_{M1}	Output circuit supply voltage input pin
24	A_1	α 1-ch output pin
25	FB_A	α 1-ch sense resistor connection pin
26	A_2	α 1-ch output pin
27	V_{M2}	Output circuit supply voltage input pin
28	B_1	α 2-ch output pin
29	FB_B	α 2-ch sense resistor connection pin
30	B_2	α 2-ch output pin
31	EXT_β	Logic circuit monitor pin
32	V_D	Video sync signal input pin
33	LATCH	Latch signal input pin
34	SDATA	Serial data input pin
35	SCLK	Serial clock input pin
36	OSC_{IN}	Original oscillation input pin (4 MHz TYP.)
37	OSC_{OUT}	Original oscillation output pin
38	RESET	Reset signal output pin

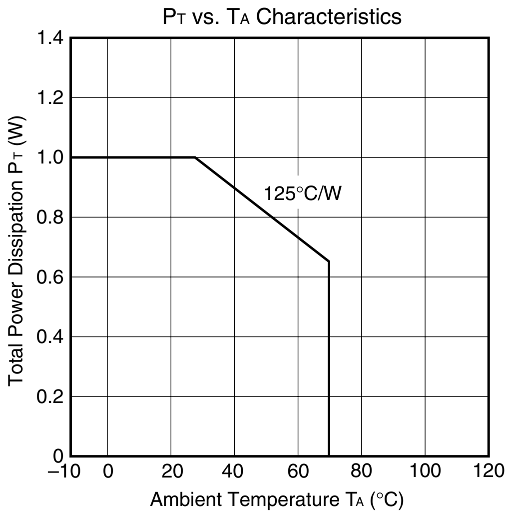
2. I/O PIN EQUIVALENT CIRCUIT

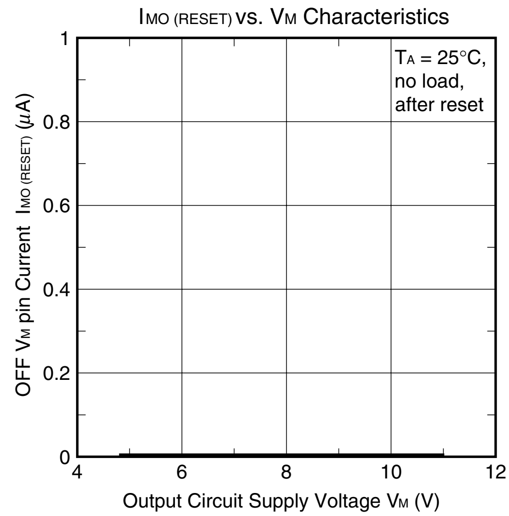
Pin Name	Equivalent Circuit	Pin Name	Equivalent Circuit
V_{DD} LATCH SDATA SCLK		OSC_{IN} RESET	
OSC_{OUT} EXT_α EXT_β		EXP0 EXP1 EXP2 EXP3	
V_{REF}		FIL_A FIL_B FIL_C FIL_D	
A_1, A_2 B_1, B_2 C_1, C_2 D_1, D_2			

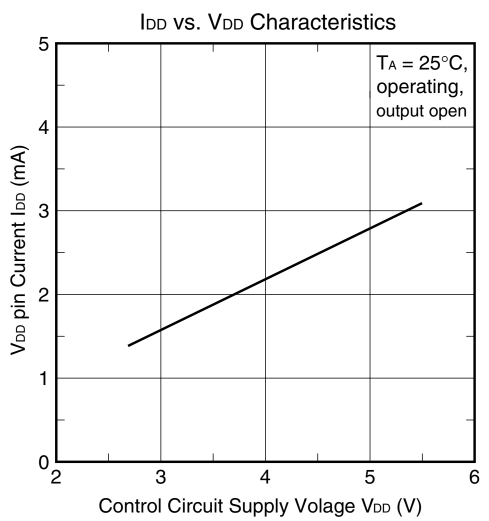
3. EXAMPLE OF STANDARD CONNECTION

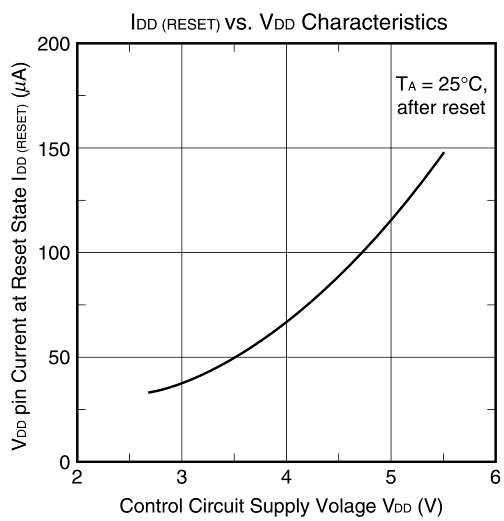


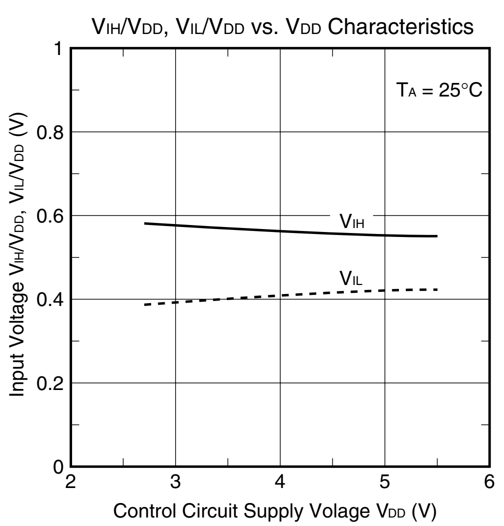
4. STANDARD CHARACTERISTICS CURVES

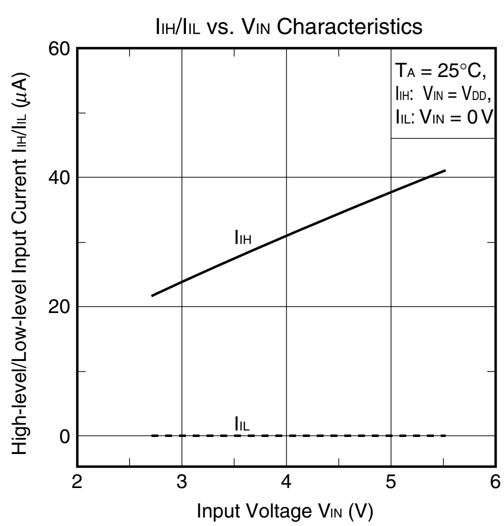




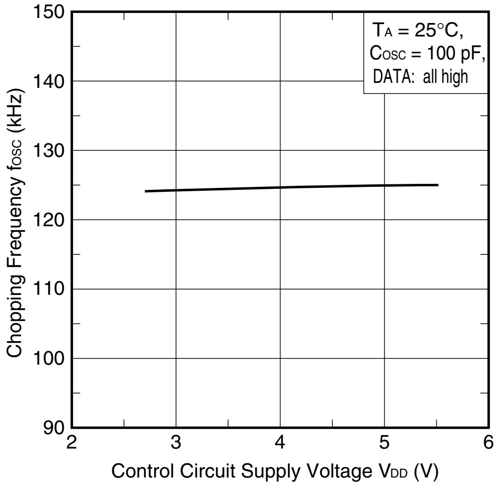




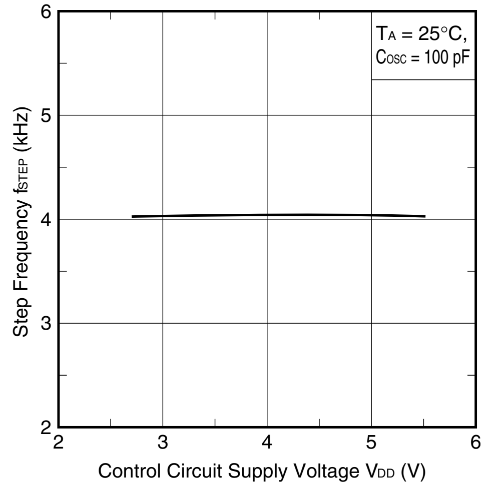




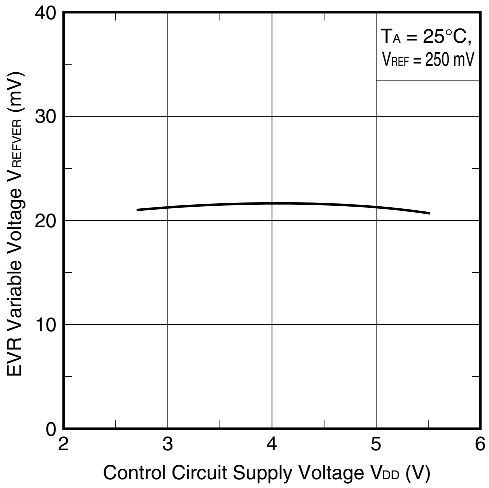
f_{OSC} vs. V_{DD} Characteristics



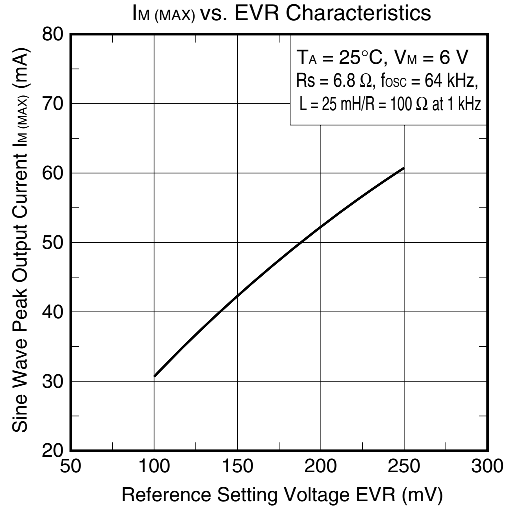
f_{STEP} vs. V_{DD} Characteristics



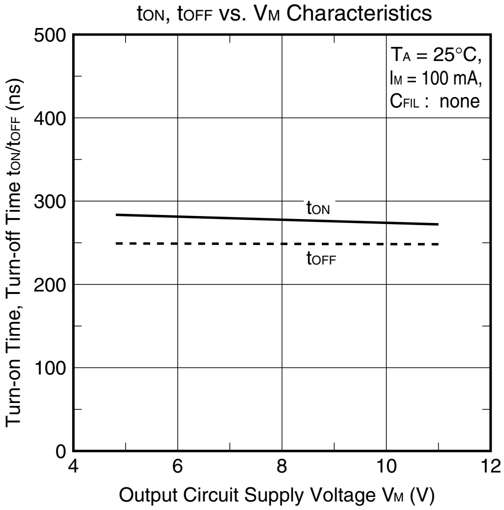
V_{REFVER} vs. V_{DD} Characteristics



$I_{M (MAX)}$ vs. EVR Characteristics



t_{ON}, t_{OFF} vs. V_M Characteristics



5. INTERFACE (I/F) CIRCUIT DATA CONFIGURATION (f_{CLK} = 4-MHz EXTERNAL CLOCK INPUT)

Input data consists of serial data (8 bytes x 8 bits).

Input serial data with the LSB first, from the 1st byte to 8th byte.

(1) Initial data

<1st byte>

Bit	Data	Function	Setting
D7	1	HEADER DATA2	DATA selection
D6	1	HEADER DATA1	
D5	1	HEADER DATA0	
D4	0	–	–
D3	1 or 0	EXP3	Hi-Z or L
D2	1 or 0	EXP2	Hi-Z or L
D1	1 or 0	EXP1	Hi-Z or L
D0	1 or 0	EXP0	Hi-Z or L

Remark Hi-Z : High impedance,
L : Low level (current sink)

<2nd byte>

Bit	Data	Function	Setting
D7	8-bit data input Note	First Point Wait	Start point wait 256 μs to 65.28 ms Setting (1 to 255) Δt = 256 μs
D6			
D5			
D4			
D3			
D2			
D1			
D0			

Note Input other than “0”.

<3rd byte>

Bit	Data	Function	Setting
D7	8-bit data input Note	First Point Magnetize Wait	Start point drive wait 256 μs to 65.28 ms Setting (1 to 255) Δt = 256 μs
D6			
D5			
D4			
D3			
D2			
D1			
D0			

Note Input other than “0”.

(2) Standard data

<1st byte>

Bit	Data	Function	Setting
D7	0	HEADER DATA2	DATA selection
D6	0	HEADER DATA1	
D5	0	HEADER DATA0	
D4	0	–	–
D3	1 or 0	EXP3	Hi-Z or L
D2	1 or 0	EXP2	Hi-Z or L
D1	1 or 0	EXP1	Hi-Z or L
D0	1 or 0	EXP0	Hi-Z or L

Remark Hi-Z : High impedance,
L : Low level (current sink)

<2nd byte>

Bit	Data	Function	Setting
D7	1 or 0	α ROTATION	α ch CCW/CW
D6	1 or 0	α ENABLE	α ch ON/OFF
D5	6-bit data input	α Pulse Number	α ch Number of pulses in 1 V_D Setting (0 to 63) Δn = 4 pulses Note
D4			
D3			
D2			
D1			
D0			

Note The number of pulses can be varied in 4-pulse steps.

<3rd byte>

Bit	Data	Function	Setting
D7	15-bit data Low-order 8-bit data input	α Pulse Width	α ch pulse cycle 0.25 to 8191.75 μs Setting (1 to 32767) Δt = 0.25 μs
D6			
D5			
D4			
D3			
D2			
D1			
D0			

<4th byte>

Bit	Data	Function	Setting
D7	1 or 0	OSCSEL	Internal/external
D6	0	-	-
D5	0	-	-
D4	5-bit data input	Chopping Frequency	Chopping frequency : 32 to 124 kHz Setting (8 to 31)[Note] Δf = 4 kHz
D3			
D2			
D1			
D0			

Note The frequency is 0 kHz if 0 to 7 is input.

<4th byte>

Bit	Data	Function	Setting
D7	1 or 0	Current Set α	set2/set1
D6	15-bit data High-order 8-bit data input	α Pulse Width	α ch pulse cycle : 0.25 to 8191.75 μs Setting (1 to 32767) Δt = 0.25 μs
D5			
D4			
D3			
D2			
D1			
D0			

<5th byte>

Bit	Data	EXT_{α}	EXT_{β}
D7	0	-	-
D6	**Note 5**	ENABLE α [Note1]	ENABLE β [Note1]
D5	**Note 5**	ROTATION α [Note2]	ROTATION β [Note2]
D4	**Note 5**	Pulse Out α	Pulse Out β
D3	**Note 5**	FF7 α	FF7 β
D2	**Note 5**	FF3 α	FF3 β
D1	**Note 5**	Checksum [Note3]	FF2 β
D0	**Note 5**	Chopping [Note4]	FF1 β

Notes 1. H level : Conducts, L level : Stops

2. H level : Reverse (CCW), L level : Forward (CW)

3. H level : Normal data input, L level : Abnormal data input

4. Not output in internal oscillation mode.

5. Select one of D0 to D6 and input “1”. If two or more of D0 to D6 are selected, they are positively ORed for output.

<5th byte>

Bit	Data	Function	Setting
D7	1 or 0	β ROTATION	β ch CCW/CW
D6	1 or 0	β ENABLE	β ch ON/OFF
D5	6-bit data input	β Pulse Number	β ch Number of pulses in 1 V_D Setting (1 to 63) Δn = 4 pulses [Note]
D4			
D3			
D2			
D1			
D0			

Note The number of pulses can be varied in 4-pulse steps.

<6th byte>

Bit	Data	Function	Setting
D7	4-bit data input	α ch Current Set2	α ch Output current setting 2 EVR : 100 to 250 mV Setting (0 to 15) [Note]
D6			
D5			
D4			
D3	4-bit data input	α ch Current Set1	α ch Output current setting 1 EVR : 100 to 250 mV Setting (0 to 15) [Note]
D2			
D1			
D0			

Note A voltage of about double EVR is output to the FIL pin.

<6th byte>

Bit	Data	Function	Setting
D7	15-bit data Low-order 8-bit data input	β Pulse Width	β ch pulse cycle: 0.25 to 8191.75 μs Setting (1 to 32767) Δt = 0.25 μs
D6			
D5			
D4			
D3			
D2			
D1			
D0			

<7th byte>

Bit	Data	Function	Setting
D7	4-bit data input	β ch Current Set2	β ch Output current setting 2 EVR: 100 to 250 mV Setting (0 to 15)Note
D6			
D5			
D4			
D3	4-bit data input	β ch Current Set1	β ch Output current setting 1 EVR: 100 to 250 mV Setting (0 to 15)Note
D2			
D1			
D0			

Note A voltage of about double EVR is output to the FIL pin.

<7th byte>

Bit	Data	Function	Setting
D7	1 or 0	Current Set β	set2/set1
D6	15-bit data High-order 7-bit data input	β Pulse Width	β ch pulse cycle: 0.25 to 8191.75 μs Setting (1 to 32767) Δt = 0.25 μs
D5			
D4			
D3			
D2			
D1			
D0			

<8th byte>

Bit	Data	Function	Setting
D7	1 or 0	Checksum	Checksum Note
D6	1 or 0		
D5	1 or 0		
D4	1 or 0		
D3	1 or 0		
D2	1 or 0		
D1	1 or 0		
D0	1 or 0		

Note Data is input so that the sum of the 1st through the 8th bytes is 00H.

<8th byte>

Bit	Data	Function	Setting
D7	1 or 0	Checksum	Checksum Note
D6	1 or 0		
D5	1 or 0		
D4	1 or 0		
D3	1 or 0		
D2	1 or 0		
D1	1 or 0		
D0	1 or 0		

Note Data is input so that the sum of the 1st through the 8th bytes is 00H.

Data Configuration

Data can be input in either of two ways. Initial data can be input when the power is first applied, or standard data can be input during normal operation. Input serial data with the LSB first, i.e., starting from the D0 bit (LSB) of the 1st byte. Therefore, the D7 bit of the 8th byte is the most significant bit (MSB).

When inputting initial data, set a start point wait time that specifies the delay from power application to pulse output, and the start point drive wait time. At the same time, also set a chopping frequency and a reference voltage (EVR) that determines the output current of each channel. Because the μPD16835A has an EXT pin for monitoring the internal operations, the parameter to be monitored can be selected by initial data.

When inputting standard data, input the rotation direction of each channel, the number of pulses, and the data for the pulse cycle.

Initial data or standard data is selected by using bits D5 to D7 of the 1st byte (see Table 5-1).

Table 5-1. Data Selection Mode (1st byte)

D7	D6	D5	Data type
1	1	1	Initial data
0	0	0	Standard data

Remark If the high-order three bits are high, the initial data is selected; if they are low, the standard data is selected.
Data other than (0, 0, 0) and (1, 1, 1) must not be input.

Input the serial data during start point wait time.

Details of Data Configuration

How to input initial data and standard data is described below.

(1) Initial data input

<1st byte>

The 1st byte specifies the type of data (initial data or standard data) and determines the presence or absence of the EXP pin output. Bits D5 to D7 of this byte specify the type of data as shown in Table 5-1, while bits D0 to D3 select the EXP output (open drain).

Table 5-2. 1st Byte Data Configuration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	1	1	1	0	0 or 1	0 or 1	0 or 1	0 or 1

The EXP pin goes low (current sink) when the input data is “0”, and high (high impedance state) when the input data is “1”. Pull this pin up to V_{DD} for use. Input “0” to bit D4.

<2nd byte>

The 2nd byte specifies the delay between data being read and data being output. This delay is called the start up wait time, and the motor can be driven from that point at which the start up wait time is “0”. This time is counted at the rising edge of V_D. The start up wait time can be set to 65.28 ms (when a 4-MHz clock is input), and can be fine-tuned by means of 8-bit division (256-μs step: with 4-MHz clock). The start up wait time is set to 65.28 ms when all the bits of the 2nd byte are set to “1”.

Caution Always input data other than “0” to this byte because the start up wait time is necessary for latching data. If “0” is input to this byte, data cannot be updated. Transfer standard data during the start up wait time.

<3rd byte>

The 3rd byte specifies the delay between the start point wait time being cleared and the output pulse being generated. This time is called the start up drive wait time, and the output pulse is generated from the point at which the start up drive wait time reaches “0”. The start up drive wait time is counted at the falling edge of the start up wait time. The start up drive wait time can be set to 65.28 ms (with 4-MHz clock) and can be fine-tuned by means of 8-bit division (256-μs step: with 4-MHz clock). The start up drive wait time is set to 65.28 ms when all the bits of the 3rd byte are “1”.

Caution Always input data other than “0” to this byte because the start up drive wait time is necessary for latching data. If “0” is input to this byte, data cannot be updated.

<4th byte>

The 4th byte selects a chopping frequency by using 5-bit data. It also selects whether the chopping frequency is created by dividing the original oscillation (external clock) or whether the internal oscillator is used. The chopping frequency is selected by bits D0 to D4. Bit D7 specifies the method used to create the chopping frequency. When this bit is “0”, the original oscillation (external clock input to OSC_{IN}) is used; when it is “1”, the internal oscillator is used. Bits D5 and D6 are fixed to “0”.

The chopping signal is output after the initial data has been input and the first standard data has been latched (see **Timing Chart**).

Table 5-3. 4th Byte Data Configuration (Initial data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0	0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

The chopping frequency is set to 0 kHz and to a value in the range of 32 to 124 kHz (in 4-kHz steps), as follows.

Although the chopping frequency is set by 5 bits of data, it is internally configured using 7-bit data (with the low-order 2 bits fixed to 0).

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0	0	0	0	0	0	0

fosc = 0 kHz

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0	0	0	0	1	1	1

fosc = 0 kHz

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0	0	0	1	0	0	0

fosc = 32 kHz

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0	0	0	1	0	0	1

fosc = 36 kHz

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0	0	1	1	1	1	1

fosc = 124 kHz

<5th byte>

The 5th byte selects a parameter to be output to the EXT pin (logic operation monitor pin). Input data to bits D0 to D6 of this byte. Bit D7 is fixed to “0”.

There are two EXT pins. EXT_{α} indicates the operating status of α ch, and EXT_{β} indicates that of β ch. The relationship between each bit and each EXT pin is as shown in Table 5-4.

Table 5-4. 5th Byte Data Configuration (Initial data)

Bit	Data	EXT_{α}	EXT_{β}
D7	0	Not used	Not used
D6	0 or 1	ENABLE α	ENABLE β
D5	0 or 1	ROTATION α	ROTATION β
D4	0 or 1	PULSEOUT α	PULSEOUT β
D3	0 or 1	FF7 α	FF7 β
D2	0 or 1	FF3 α	FF3 β
D1	0 or 1	CHECKSUM	FF2 β
D0	0 or 1	CHOPPING	FF1 β

The checksum bit is cleared to “0” in the event of an error. Normally, it is “1”.

If two or more signals that output signals to EXT_{α} and EXT_{β} are selected, they are positively ORed for output.

Caution The CHOPPING signal is not output in internal oscillation mode.

Remark The meanings of the symbols listed in Table 5-4 are as follows:

ENABLE : Output setting (H : Conducts, L : Stops)

ROTATION : Rotation direction (H : Reverse (CCW), L : Forward (CW))

PULSEOUT : Output pulse signal

FF7 : Presence/absence of pulse in LATCH cycle (Outputs H level if output pulse information exists in standard data.)

FF3 : Pulse gate (output while pulse exists)

FF2 : Outputs H level during start up wait time + start up drive wait time

FF1 : Outputs H level during start up wait time

CHECKSUM : Checksum output (H : when normal data is transmitted,
L : when abnormal data is transmitted)

CHOPPING : Chopping wave output (in original oscillation mode only)

<6th byte>

The 6th byte sets the peak output current value of α ch. The output current is determined by the EVR reference voltage.

The 250-mV (TYP.) voltage input from an external source to the V_{REF} pin is internally doubled and input to a 4-bit D/A converter. By dividing this voltage by 4-bit data, an EVR reference voltage can be set inside the IC within the range of 200 to 500 mV, in units of 20 mV.

The μPD16835A can set two values of the EVR reference voltage in advance. This is done by using bits D0 to D3 or D4 to D7. Which of the two EVR reference voltage values is to be used is specified by the CURRENT SET bit in the standard data.

If all the bits of the 6th byte are “0”, the EVR reference voltage of 200 mV is selected; if they are “1”, the EVR reference voltage of 500 mV is selected.

Table 5-5. 6th Byte Data Configuration (Initial data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

Remark Bits D4 to D7 : Reference voltage 2 (EVR $\alpha 2$)
Bits D0 to D3 : Reference voltage 1 (EVR $\alpha 1$)

<7th byte>

The 7th byte specifies the peak output current value of β ch. The output current is determined by the EVR reference voltage.

The 250-mV (TYP.) voltage input from an external source to the V_{REF} pin is internally doubled and input to a 4-bit D/A converter. By dividing this voltage by 4-bit data, an EVR reference voltage can be set inside the IC within a range of 200 to 500 mV, in units of 20 mV.

The μPD16835A can set two values of the EVR reference voltage in advance. This is done using bits D0 to D3 or D4 to D7. Which of the two EVR reference voltage values is to be used is specified by the CURRENT SET bit in the standard data.

If all the bits of the 7th byte are “0”, the EVR reference voltage of 200 mV is selected; if they are “1”, the EVR reference voltage of 500 mV is selected.

Table 5-6. 7th Byte Data Configuration (Initial data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

Remark Bits D4 to D7 : Reference voltage 2 (EVR $\beta 2$)
Bits D0 to D3 : Reference voltage 1 (EVR $\beta 1$)

<8th byte>

The 8th byte is checksum data. Normally, the sum of the 8-byte data is 00H.

If the sum is not 00H because data transmission is abnormal, the stepping operation is inhibited and the checksum output pin (EXT pin) is kept “L”.

(2) Standard data input

<1st byte>

The 1st byte specifies the type of data and whether the EXP pin output is used, such as when the initial data is input.

Table 5-7. 1st Byte Data Configuration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	1	1	1	0	0 or 1	0 or 1	0 or 1	0 or 1

The EXP pin goes low (current sink) when the input data is “0”, and high (high impedance state) when the input data is “1”. Input “0” to bit D4.

<2nd byte>

The 2nd byte specifies the rotation direction of the α channel, enables output of the α channel, and the number of pulses (252 pulses MAX.) during the $1V_D$ period (in 1 cycle of FF2) of the α channel.

Bit D7 is used to specify the rotation direction. The rotation is in the forward direction (CW mode) when this bit is “0”; it is in the reverse direction (CCW mode) when the bit is “1”.

Bit D6 is used to enable the output of the α channel. The α channel enters the high impedance state when this bit is “0”; it is in conduction mode when the bit is “1”.

The number of pulses is set by bits D0 to D5. It is set by 6 bits in terms of software. However, the actual circuit uses an 8-bit counter with the low-order two bits fixed to “0”. Therefore, the number of pulses that is actually generated during start up wait time + start up drive wait (FF2) cycle is the number of pulses input x 4. The number of pulses can be set to a value in the range of 0 to 252, in units of 4 pulses.

Table 5-8. 2nd Byte Data Configuration (Standard data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
	Rotation direction	ENABLE	Number of pulses					

<3rd and 4th bytes>

The 3rd and 4th bytes select the pulse cycle of the α channel and which of the two reference voltages, created in the initial mode, is to be used (CURRENT SETα).

The pulse cycle is specified using 15 bits : bits D0 (least significant bit) to D7 of the 3rd byte, and bits D0 to D6 (most significant bit) of the 4th byte. The pulse cycle can be set to a value in the range of 0.25 to 8191.75 μs in units of 0.25 μs (with a 4-MHz clock).

CURRENT SETα is specified by bit D7 of the 4th byte. When this bit is “0”, reference voltage 1 ($EVR_{\alpha 1}$) is selected; when it is “1”, reference voltage 2 ($EVR_{\alpha 2}$) is selected. For further information, refer to the description of the 6th byte of the initial data.

Table 5-9. 4th Byte Data Configuration (Standard data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
	CURRENT SETα	Most significant bit						

Table 5-10. 3rd Byte Data Configuration (Standard data)

D7	D6	D5	D4	D3	D2	D1	D0
0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
							Least significant bit

(Reference) 6th Byte Data Configuration for Initial Data

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

Remark Bits D4 to D7 : Reference voltage 2 ($EVR_{\alpha 2}$)
Bits D0 to D3 : Reference voltage 1 ($EVR_{\alpha 1}$)

<5th byte>

The 5th byte specifies the rotation direction of the β channel, enables output of the β channel, and the number of pulses (252 pulses MAX.) during the $1V_D$ period (in one cycle of FF2) of the β channel.

Bit D7 is used to specify the rotation direction. The rotation is in the forward direction (CW mode) when this bit is “0”; it is in the reverse direction (CCW mode) when the bit is “1”.

Bit D6 is used to enable the output of the β channel. The β channel goes into a high impedance state when this bit is “0”; it is in the conduction mode when the bit is “1”.

The number of pulses is set by bits D0 to D5. It is set by six bits in terms of software. However, the actual circuit uses an 8-bit decoder with the low-order two bits fixed to “0”. Therefore, the number of pulses that is actually generated during start up wait time + start up drive wait (FF2) cycle is the number of pulses input x 4. The number of pulses can be set in a range of 0 to 252 and in units of 4 pulses.

Table 5-11. 5th Byte Data Configuration (Standard data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

Rotation direction (D7) ENABLE (D6) Number of pulses (D5 to D0)

<6th and 7th bytes>

The 6th and 7th bytes select the pulse cycle of the β channel and which of the two reference voltages, created in the initial mode, is to be used (CURRENT SETβ).

The pulse cycle is specified using 15 bits : bits D0 (least significant bit) to D7 of the 6th byte, and bits D0 to D6 (most significant bit) of the 7th byte. The pulse cycle can be set to a value in the range of 0.25 to 8191.75 μs in units of 0.25 μs (with a 4-MHz clock).

CURRENT SETβ is specified by bit D7 of the 7th byte. When this bit is "0", reference voltage 1 (EVR$_{\beta 1}$) is selected; when it is "1", reference voltage 2 (EVR$_{\beta 2}$) is selected. For further information, refer to the description of the 7th byte of the initial data.

Table 5-12. 7th Byte Data Configuration (Standard data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

CURRENT SETβ (D7) Most significant bit (D6)

Table 5-13. 6th Byte Data Configuration (Standard data)

D7	D6	D5	D4	D3	D2	D1	D0
0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

Least significant bit (D0)

(Reference) 7th Byte Data Configuration for Initial Data

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

Remark Bits D4 to D7 : Reference voltage 2 (EVR $_{\beta 2}$)
Bits D0 to D3 : Reference voltage 1 (EVR $_{\beta 1}$)

<8th byte>

The 8th byte is checksum data. Normally, the sum of the 8-byte data is 00H.

If the sum is not 00H because data transmission is abnormal, the stepping operation is inhibited and the checksum output pin (EXT pin) is held at "L".

(Data Update Timing)

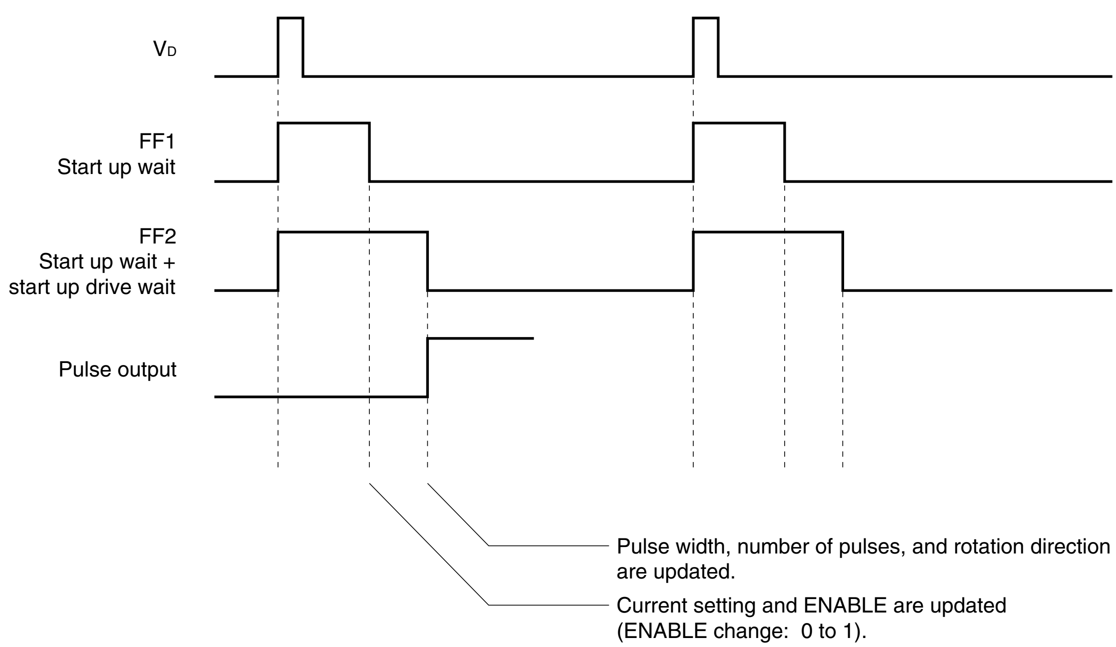
The standard data (pulse width, number of pulses, rotation direction, current setting, and ENABLE) of this product are set and updated at the following latch timing.

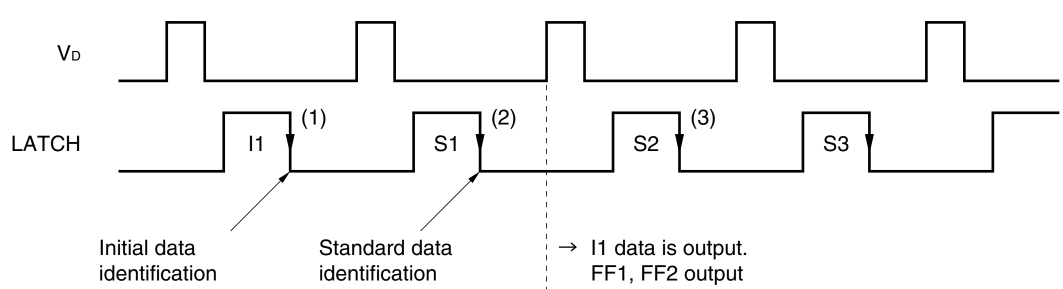
Table 5-14. Data Update Timing

ENABLE change	1 → 1	0 → 1	1 → 0	0 → 0
Pulse width	FF2↓	FF2↓	FF2↓	–
Number of pulses	FF2↓	FF2↓	FF2↓	–
Rotation direction	FF2↓	FF2↓	FF2↓	–
Current setting	FF2↓	FF1↓	FF2↓	–
ENABLE	FF2↓	FF1↓	FF2↓	–

The timing at which data is to be updated differs, as shown in Table 5-14, depending on the enabled status.

For example, suppose the enable signal is currently "0" (output high impedance) and "1" (output conduction) is input by the next data. In this case, the pulse width, number of pulses, and rotation direction signals are updated at FF2(upon the completion of start up wait), and the current setting and ENABLE signals are updated at FF1 (upon completion of start up drive wait).





	(1)	(2)	(3)
Pulse width	Internal data retained. Output reset	Not output	Updated to S2 data at FF2
Rotation direction	Internal output retained	Not output	
Number of pulses	Internal data retained. Output reset	Not output	
Current setting	Internal output retained	Not output	Updated to S2 data at either FF1 or FF2 by enable data of (2)
ENABLE	Internal output retained	Not output	

The initial mode of this product is as follows.
The IC operation can be initialized as follows:

(1) Turns ON V_{DD}.
(2) Make RESET input "L".
(3) Input serial initial data.

In initial mode, the operating status of the IC is as shown in Table 5-15.

Table 5-15. Operations in Initial Mode

Item	Specifications
Current consumption	100 μA
OSC	Oscillation stops. Input of external clock is inhibited.
V_D	Input inhibited.
FF1 to FF7	"L" level
PULSE OUT	"L" level
EXP0 to EXP3	Undefined in the case of (1) above. Previous value is retained in the case of (2) above. Can be updated by serial data in the case of (3) above.
Serial operation	Can be accessed after initialization in the case of (1) above. Can be accessed after RESET has gone "H" in the case of (2) above. Can be accessed in the case of (3) above.

Step pulse output is inhibited and FF7 is made "L" if the following conditions are satisfied.

(1) If the set number of pulses (2nd/5th: standard data) is 00H.
(2) If the checksum value is other than 00H.
(3) If the start up wait time is set to 1 V_D or longer.
(4) If the start up wait time + start up drive wait time is set to 1 V_D or longer.
(5) If start up wait is completed earlier than LATCH (↓).
(6) If V_D is not input.

Cautions on Correct Use

(1) With this product, input the data for start up wait and start up drive wait. Because the standard data are set or updated by these wait times, if the start up wait time and start up drive wait time are not input, the data are not updated.

(2) The start up wait time must be longer than LATCH.

(3) If the rising of the start up drive wait time is the same as the falling of the last output pulse, a count error occurs, and the IC may malfunction.

(4) Input the initial data in a manner that it does not straddle the video sync signal (V_D). If it does, the initial data is not latched.

(5) Transmit the standard data during the start up wait time (FF1). If it is input at any other time, the data may
not be transmitted correctly.

(6) If the LGND potential is undefined, the data may not be input correctly. Keep the LGND potential to the minimum level. It is recommended that LGND and PGND be divided for connection (single ground) to prevent the leakage of noise from the output circuit.

6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		–0.5 to +6.0	V
	V_M		–0.5 to +11.2	V
Input voltage	V_{IN}		–0.5 to V_{DD}+ 0.5	V
Reference voltage	V_{REF}		500	mV
H bridge drive current Note 1	$I_{M(DC)}$	DC	±150	mA/phase
Instantaneous H bridge drive current Note 1	$I_{M(pulse)}$	PW ≤ 10 ms, Duty ≤ 5%	±300	mA/phase
Power consumption Note 2	P_T		1.0	W
Peak junction temperature	$T_{CH(MAX.)}$		150	°C
Storage temperature	T_{stg}		–55 to +150	°C

Notes 1. Permissible current per phase with the IC mounted on a PCB.

2. When the IC is mounted on a glass epoxy PCB (10 cm x 10 cm x 1 mm).

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range

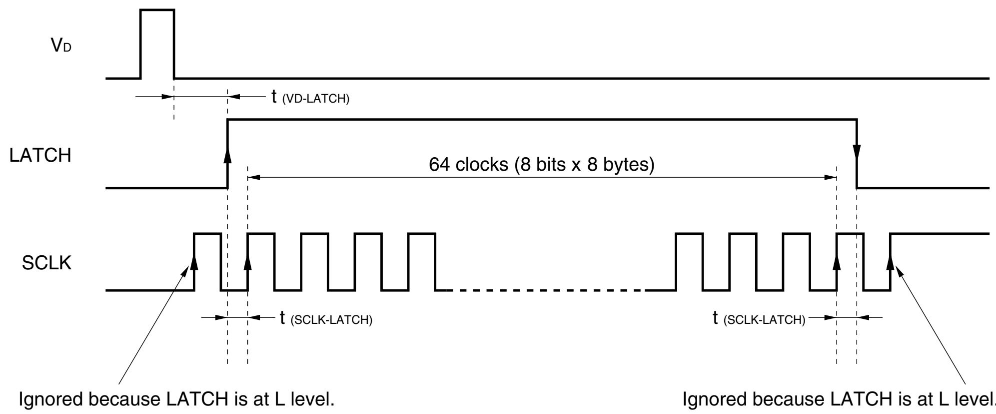
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	2.7		5.5	V
	V_M	4.8		11	V
Input voltage	V_{IN}	0		V_{DD}	V
Reference voltage	V_{REF}	225	250	275	mV
EXP pin input voltage	V_{EXPIN}			V_{DD}	V
EXP pin input current	I_{EXPIN}			100	μA
H bridge drive current	$I_{M(DC)}$	–100		+100	mA
H bridge drive current	$I_{M(pulse)}$ Note 1	–200		+200	mA
Clock frequency (OSC_{IN})	f_{CLK} Note 2	3.9	4	4.2	MHz
Clock frequency amplitude	V_{fCLK} Note 2	0.7 V_{DD}		V_{DD}	V
Serial clock frequency (SCLK)	f_{SCLK}			5.0	MHz
Video sync signal width	$PW_{(VD)}$ Note 3	250			ns
LATCH signal wait time	$t_{(VD\text{-}LATCH)}$ Note 4	400			ns
SCLK wait time	$t_{(SCLK\text{-}LATCH)}$ Note 4	400			ns
SDATA setup time	t_{setup} Note 4	80			ns
SDATA hold time	t_{hold} Note 4	80			ns
Chopping frequency	f_{OSC} Note 3	32		124	kHz
Reset signal pulse width	t_{RST}	100			μs
Operating temperature	T_A	–10		+70	°C
Peak junction temperature	$T_{CH(MAX.)}$			125	°C

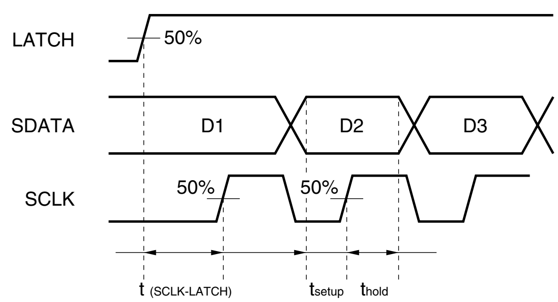
Notes 1. PW ≤ 10 ms, duty ≤ 5%

2. C_{OSC} = 33 pF, V_{REF} = 250 mV

3. f_{CLK} = 4 MHz

4. Serial data delay time(see the figure on the next page.)


VD
t (VD-LATCH)
LATCH
64 clocks (8 bits x 8 bytes)
SCLK
t (SCLK-LATCH)
t (SCLK-LATCH)
Ignored because LATCH is at L level.
Ignored because LATCH is at L level.


LATCH
50%
SDATA
D1
D2
D3
SCLK
50%
50%
t (SCLK-LATCH)
tsetup
thold

ELECTRICAL CHARACTERISTICS

DC Characteristics (Unless otherwise specified, V_{DD} = 3.3 V, V_M = 6.0 V, V_{REF} = 250 mV, T_A = 25°C, f_{CLK} = 4 MHz, C_{OSC} = 33 pF, C_{FIL} = 1000 pF, EVR = 100 mV (0000))

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Off V_M pin current	$I_{MO(RESET)}$	No load, reset period			1.0	μA
V_{DD} pin current	I_{DD}	Output open			3.0	mA
V_{DD} pin current	$I_{DD(RESET)}$	Reset period			100	μA
High level input voltage	V_{IH}	LATCH, SCLK, SDATA, V_D, RESET, OSC_{IN}	0.7 V_{DD}			V
Low level input voltage	V_{IL}				0.3 V_{DD}	V
Input hysteresis voltage	V_H			300		mV
Monitor output voltage 1 (EXT α, β)	$V_{OM\,\alpha(H)}$, $V_{OM\,\beta(H)}$	5th byte	0.9 V_{DD}			V
	$V_{OM\,\alpha(L)}$, $V_{OM\,\beta(L)}$	5th byte			0.1 V_{DD}	V
Monitor output voltage 2 (EXP0 to EXP3 : open drain)	$V_{OEXP(H)}$	Pull up (V_{DD})			V_{DD}	V
	$V_{OEXP(L)}$	I_{OEXP} = 100 μA			0.1 V_{DD}	V
High level input current	I_{IH}	V_{IN} = V_{DD}			0.06	mA
Low level input current	I_{IL}	V_{IN} = 0 V	−1.0			μA
Reset pin high level input current	$I_{IH(RST)}$	V_{RST} = V_{DD}			1.0	μA
Reset pin low level input current	$I_{IL(RST)}$	V_{RST} = 0	−1.0			μA
Input pull down resistor	R_{IND}	LATCH, SCLK, SDATA, V_D	50		200	kΩ
H bridge ON resistance Note 1	R_{ON}	I_M = 100 mA		3.5	5.0	Ω
Chopping frequency (internal oscillation: C_{OSC} = 100 pF)	$f_{OSC(1)}$	DATA: 00000 (4th byte)		0		kHz
	$f_{OSC(2)}$	DATA: 11111 (4th byte)	100	124	150	
Step frequency	f_{STEP}	Minimum step		4		kHz
V_D delay time Note 2	Δt_{VD}				250	ns
Sine wave peak output current Note 3	I_M	L = 25 mH/R = 100 Ω (1 kHz) EVR = 200 mV (1010) R_S = 6.8 Ω, f_{OSC} = 64 kHz		52		mA
FIL pin voltage Note 4	V_{EVR}	EVR = 200 mV (1010)	370	400	430	mV
FIL pin step voltage Note 4	$V_{EVRSTEP}$	Minimum step		20		mV

AC Characteristics (Unless otherwise specified, V_{DD} = 3.3 V, V_M = 6.0 V, T_A = 25°C, f_{CLK} = 4 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
H bridge output circuit turn on time	t_{ONH}	I_M = 100 mA Note 5		1.0	2.0	μs
H bridge output circuit turn off time	t_{OFFH}	I_M = 100 mA Note 5		1.0	2.0	μs

Notes 1. Total of ON resistance at top and bottom of output H bridge

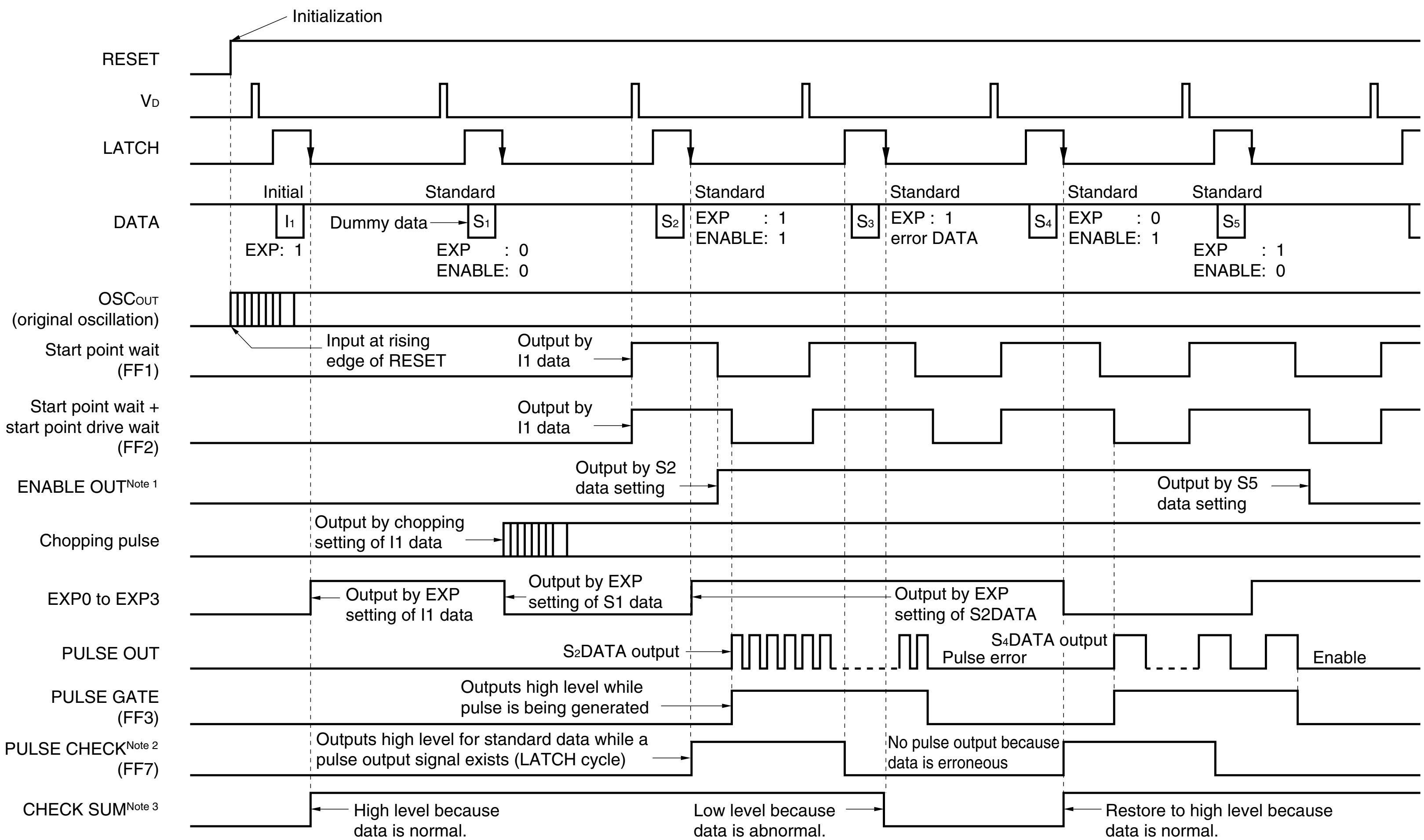
2. By OSC_{IN} and V_D sync circuit

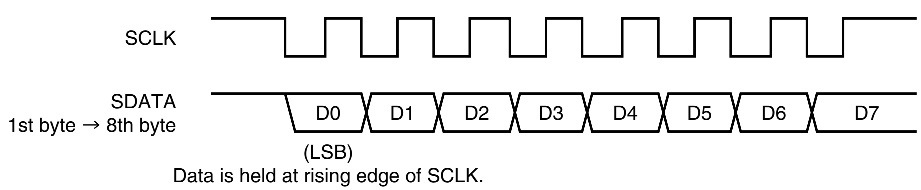
3. FB pin is monitored.

4. FIL pin is monitored. A voltage about twice that of the EVR value is output to the FIL pin.

5. 10 to 90% of the pulse peak value without filter capacitor (C_{FIL})

TIMING CHART (1)



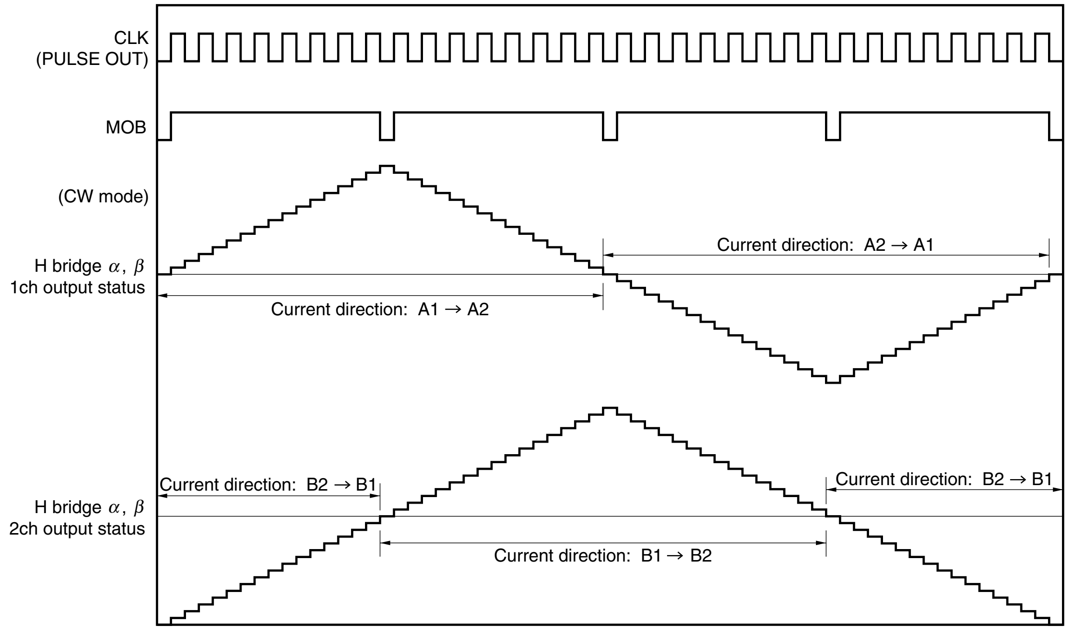


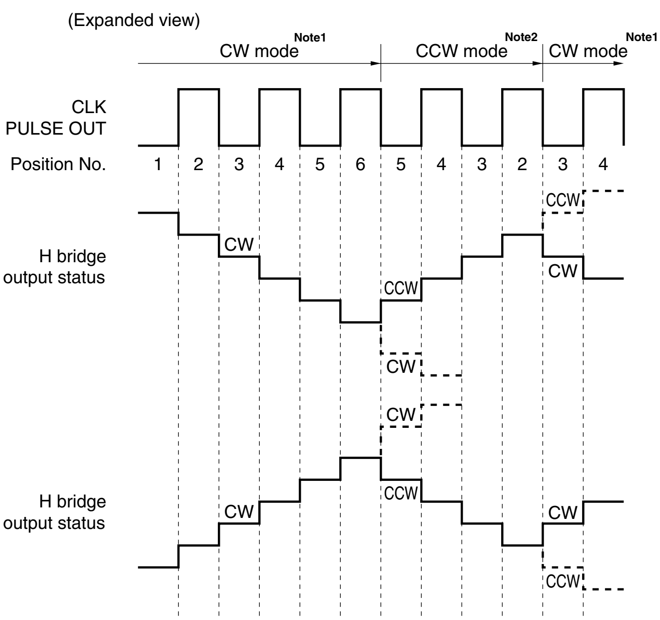
Notes 1. ENABLE is set at the falling edge of FF1 when the level changes from low to high, and at the falling edge of FF2 when the level changes from high to low.

2. FF7 is an output signal that is used to check for the presence or absence of a pulse in the standard data, is updated at the falling edge of LATCH and reset once at the rising edge of LATCH. If CHECK SUM is other than “00H”, FF7 goes low, inhibiting pulse output, even if a pulse is generated.

3. CHECK SUM output is updated at the falling edge of LATCH.

TIMING CHART (2)





Notes1. In CW mode : Position No. is incremented.
2. In CCW mode : Position No. is decremented.

Remarks 1. The current value of the actual wave is approximated to the value shown on the next page.
2. The C_1, C_2, D_1, and D_2 pins of β channel correspond to the A_1, A_2, B_1, and B_2 pins of α channel.
3. The CW mode is set if the D7 bit of the 2nd and 5th bytes of the standard data is “0”.
4. The CCW mode is set if the D7 bit of the 2nd and 5th bytes of the standard data is “1”.

RELATION BETWEEN ROTATION ANGLE, PHASE CURRENT, AND VECTOR QUANTITY (64-DIVISION MICRO STEP)

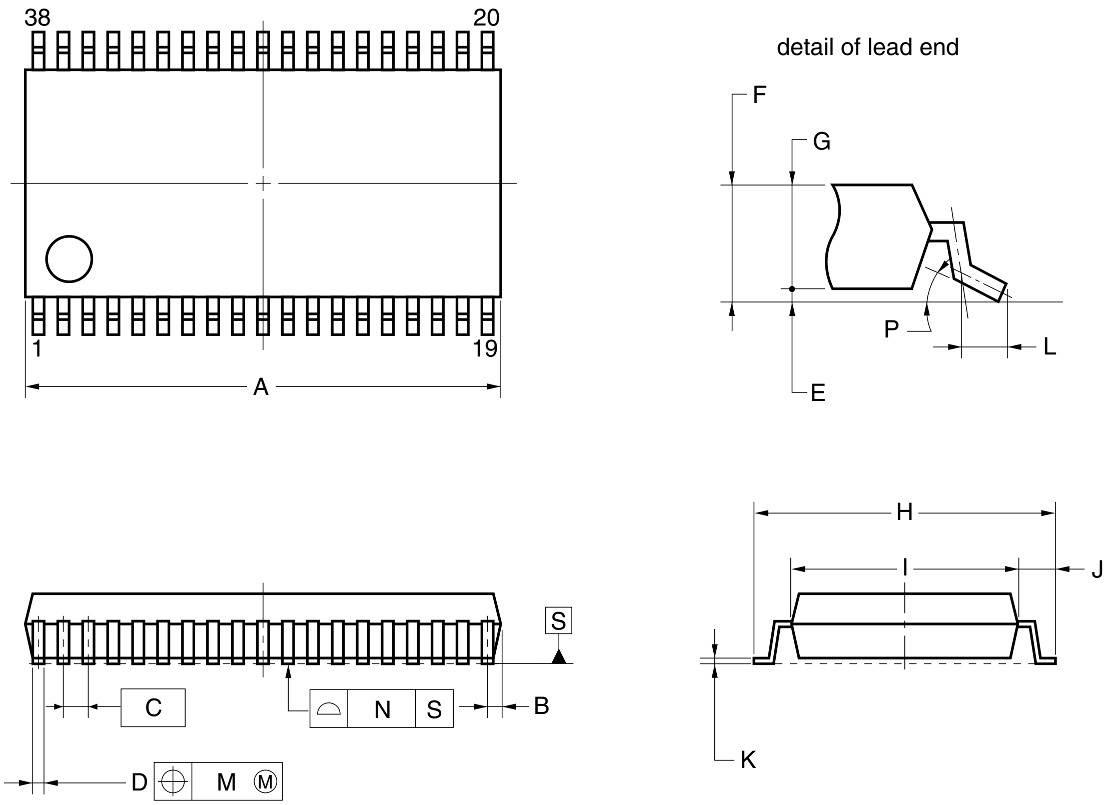
(Values of μPD16835A for reference)

Step	Rotation angle (θ)	A phase current			B phase current			Vector quantity
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	TYP.
θ 0	0	–	0	–	–	100	–	100
θ 1	5.6	2.5	9.8	17.0	–	100	–	100.48
θ 2	11.3	12.4	19.5	26.5	93.2	98.1	103	100
θ 3	16.9	22.1	29.1	36.1	90.7	95.7	100.7	100.02
θ 4	22.5	31.3	38.3	45.3	87.4	92.4	97.4	100.02
θ 5	28.1	40.1	47.1	54.1	83.2	88.2	93.2	99.99
θ 6	33.8	48.6	55.6	62.6	78.1	83.1	88.1	99.98
θ 7	39.4	58.4	63.4	68.4	72.3	77.3	82.3	99.97
θ 8	45	65.7	70.7	75.7	65.7	70.7	75.7	99.98
θ 9	50.6	72.3	77.3	82.3	58.4	63.4	68.4	99.97
θ 10	56.3	78.1	83.1	88.1	48.6	55.6	62.6	99.98
θ 11	61.9	83.2	88.2	93.2	40.1	47.1	54.1	99.99
θ 12	67.5	87.4	92.4	97.4	31.3	38.3	45.3	100.02
θ 13	73.1	90.7	95.7	100.7	22.1	29.1	36.1	100.02
θ 14	78.8	93.2	98.1	103	12.4	19.5	26.5	100
θ 15	84.4	–	100	–	2.5	9.8	17.0	100.48
θ 16	90	–	100	–	–	0	–	100

Remark These data do not indicate guaranteed values.

7. PACKAGE DRAWING

38-PIN PLASTIC SSOP (7.62 mm (300))



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.7±0.3
B	0.65 MAX.
C	0.65 (T.P.)
D	$0.37^{+0.05}_{-0.1}$
E	0.125±0.075
F	1.675±0.125
G	1.55
H	7.7±0.2
I	5.6±0.2
J	1.05±0.2
K	$0.2^{+0.1}_{-0.05}$
L	0.6±0.2
M	0.10
N	0.10
P	$3°^{+7°}_{-3°}$

P38GS-65-BGG-1

8. RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document "**SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E)**.

Type of Surface Mount Device

μPD16835AGS-BGG: 38-pin plastic shrink SOP (7.62 mm (300))

Process	Soldering conditions	Symbol
Infrared Ray Reflow	Peak temperature: 235°C or below (Package surface temperature), Reflow time: 30 seconds or less (at 210°C or higher), Maximum number of reflow processes: 3 time or less, Number of days: None [Note], Flux: Rosin-based flux with low chlorine content (chlorine 0.2 Wt% or below) is recommended.	IR35-00-3
Vapor Phase Soldering	Peak temperature: 215°C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200°C or higher), Maximum number of reflow processes: 3 time or less, Number of days: None [Note], Flux: Rosin-based flux with low chlorine content (chlorine 0.2 Wt% or below) is recommended.	VP15-00-3
Wave Soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature: 120°C or below (Package surface temperature), Flux: Rosin-based flux with low chlorine content (chlorine 0.2 Wt% or below) is recommended.	WS60-00-1
Partial Heating Method	Pin temperature: 300°C or below, Heat time: 3 seconds or less (Per each side of the device).	–

Note Number of days the device can be stored after the dry pack has been opened, at conditions of 25°C, 65%RH.

Caution Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.