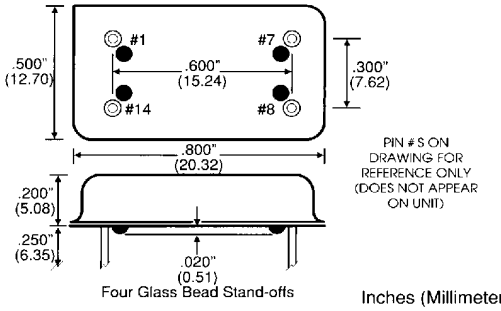
TRI-STATE CLOCK OSCILLATOR

P1100–3S SERIES

- "True" Tri–State (High Impedance) Output.
- High Speed CMOS Output.
- TTL–Compatible: Drives up to 10 Standard TTL Loads.
- Enable/Disable Input is HC-, HCT, and TTL–Compatible.
- Hermetically Sealed in Metal Package.

DIMENSIONS P1100–3S



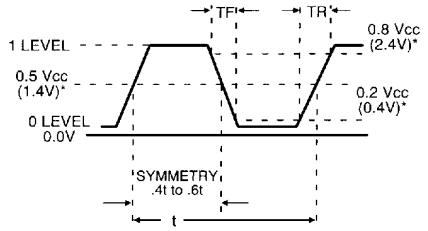
Inches (Millimeters)

PIN	CONNECTION
1	Enable/Disable Input
7	Case Ground
8	Output
14	Input (Vcc)

Model	Frequency Stability 0°C to 70°C
P1145-3S	±0.005% (50 ppm)
P1100-3S	±0.01% (100 ppm)
P1114-3S	±0.05% (500 ppm)
P1115-3S	±0.1% (1000 ppm)

STANDARD SPECIFICATIONS:

Frequency Range:	500 kHz TO 100 MHz
Operating Temperature Range:	0°C to 70°C
Overall Frequency Stability:	±0.01% (100ppm) Standard 50ppm to 1000ppm also available.
Input Voltage(Vcc):	5Vdc ±10%
Input Current:	10mA to 60 mA without load. (Varies with frequency and load)
Requirement for Enable/Disable Input at pin #1:	Enable State (Logic "1"): 0.6 x Vcc minimum (Vih), 10µA maximum (Iih) Disable State (Logic "0"): 0.4 volt maximum (Vil), 150µA maximum (Iih)
Output at pin #8 Corresponding to each Input State:	Enable state: Normal Output Disable state: High–impedance Output



* Voltage levels in ( ) refer to TTL levels.

Test Load:	50 pF (HC Device); 10-TTL +20 pF (TTL Device)
Output Symmetry:	60/40 to 40/60 (55/45 to 45/55 Typical)
Rise & Fall Times:	6nS Maximum with 10 TTL Load
Logic Level "1":	4.5 V Min.(HC Device) 2.4 V Min.(TTL Device)
Logic Level "0":	0.5 V Max.(HC Device) 0.4 V Max.(TTL Device)
Sealing Method:	Resistance Weid
Leads:	Nickel Plated; Solder Dipped