19-3286; Rev 0; 5/04

Low-Jitter 106.25MHz/212.5MHz Fibre-Channel Clock Generator

General Description

The MAX3610 is a low-jitter, high-performance, dual-rate clock generator optimized for 1Gbps/2Gbps/4Gbps Fibre-Channel applications. When connected with an external AT-cut crystal, the device generates a precision clock output by integrating a crystal oscillator with Maxim's low-noise phase-locked loop (PLL) providing a low-cost solution. By coupling Maxim's low-noise PLL design featuring a low-jitter generation VCO with an inexpensive fundamental mode crystal, the MAX3610 provides the optimum combination of low cost, flexibility, and high performance.

The MAX3610 output frequency is selectable. When using a 26.5625MHz crystal, the output clock rate can be set to either 106.25MHz or 212.5MHz. When operating at 106.25MHz, the typical phase jitter is $0.7ps_{RMS}$ from 12kHz to 20MHz. The MAX3610A has low-voltage positive-emitter-coupled logic (LVPECL) clock output drivers. The MAX3610B has low-voltage differential-signal (LVDS) clock output drivers. The MAX3610 output drivers can also be disabled.

The MAX3610 operates from a single +3.3V supply. The PECL version typically consumes 165mW, while the LVDS version typically consumes 174mW. Both devices are available in die form and have a 0°C to +85°C operating temperature range.

Applications

Fibre-Channel Hard Disk Drives

Host Bus Adapters

Raid Controllers

Fibre-Channel Switches

Features

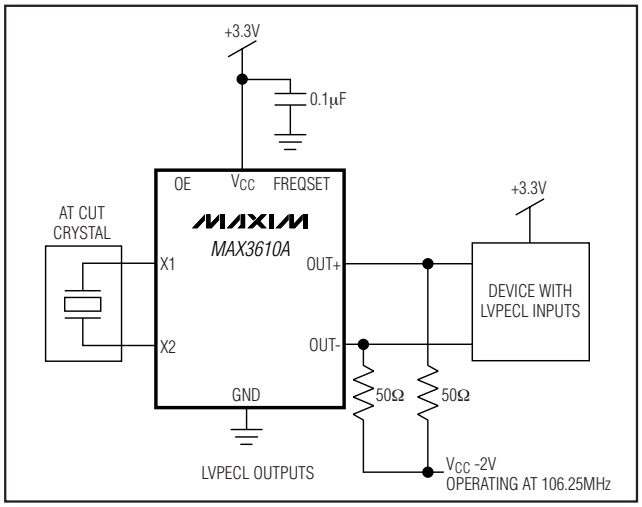
- **Clock Output Frequencies: 106.25MHz or 212.5MHz**
- **Phase Jitter: $0.7ps_{RMS}$**
- **LVPECL or LVDS Output**
- **Excellent Power-Supply Noise Rejection**
- **Supply Current: 50mA at +3.3V Supply (LVPECL)**
  53mA at +3.3V Supply (LVDS)
- **0°C to +85°C Temperature Range**
- **Optional Output Disable**

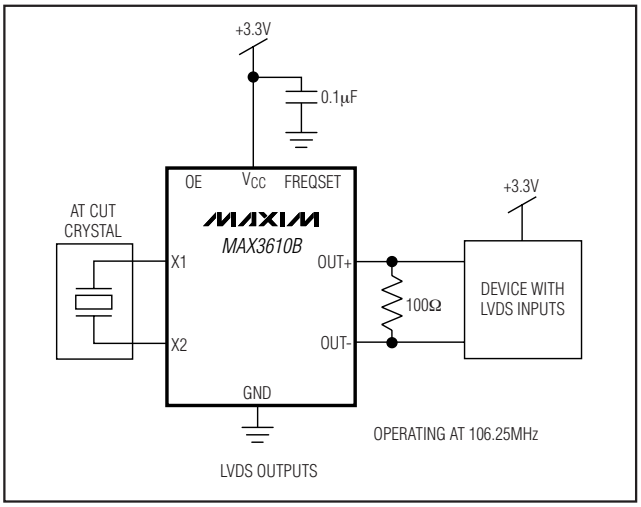
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	OUTPUTS
MAX3610AU/D	0°C to +85°C	Die	LVPECL
MAX3610BU/D	0°C to +85°C	Die	LVDS

Dice are designed to operate from 0°C to +85°C, but are tested and guaranteed only at T_A = +25°C.

Typical Operating Circuits





Low-Jitter 106.25MHz/212.5MHz Fibre-Channel Clock Generator

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .....-0.5V to +5.0V
Voltage at FREQSET, OE.....-0.5V to (V_{CC} + 0.5V)
Voltage at X1 .....-0.5V to +0.8V
Voltage at X2.....0 to 2V
PECL Output Current 56mA
LVDS Output Voltage .....-0.5V to (V_{CC} + 0.5V)
Operating Temperature Range.....0°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Processing Temperature.....+400°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Note 2)	LVPECL		50	65	mA
			LVDS		53	67	
LVPECL OUTPUT SPECIFICATIONS (Note 3)							
Output High Voltage	V_{OH}	0°C to +85°C		V_{CC} - 1.025		V_{CC} - 0.88	V
Output Low Voltage	V_{OL}	0°C to +85°C		V_{CC} - 1.81		V_{CC} - 1.62	V
LVDS OUTPUT SPECIFICATIONS (Figure 1)							
LVDS Output High Voltage	V_{OH}					1.475	V
LVDS Output Low Voltage	V_{OL}			0.925			V
LVDS Differential Output Voltage	$\|V_{OD}\|$			250		400	mV
LVDS Change in Magnitude of Differential Output for Complementary States	$\Delta\|V_{OD}\|$					25	mV
LVDS Offset Output Voltage (Output Common-Mode Voltage)	V_{OS}			1.125		1.275	V
LVDS Change in Magnitude of Output Offset Voltage for Complementary States	$\Delta\|V_{OS}\|$					25	mV
LVDS Differential Output Impedance				80	100	140	Ω
LVDS Output Current		Outputs shorted together				12	mA
CONTROL INPUT SPECIFICATIONS (FREQSET, OE)							
TTL Control Input-Voltage High	V_{IH}			2			V
TTL Control Input-Voltage Low	V_{IL}					0.8	V
Input Current (Input High)	I_{IH}			-10		+10	µA
Input Current (Input Low)	I_{IL}			-50		+10	µA
CLOCK OUTPUT SPECIFICATIONS							
Clock Output Frequency		FREQSET = TTL High, VCC, or NC			106.25		MHz
		FREQSET = TTL Low or GND			212.5		
Crystal Oscillation Circuit Input Capacitance					12		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Phase Jitter	PJ_{RMS}	12kHz to 20MHz			0.7	1.0	ps_{RMS}
Accumulated Deterministic Jitter Due to Reference Spurs					3.0		ps_{P-P}
Accumulated Deterministic Jitter Due to Power-Supply Noise		(Note 4)	10kHz		3.0		ps_{P-P}
			100kHz		27	69	
			200kHz		15	43	
			1MHz		7		
Clock-Output Edge Speeds	t_R, t_F	20% to 80%	LVPECL outputs	250		600	ps
			LVDS outputs	200		600	
Clock-Output Duty Cycle				49		51	%
Oscillation Startup Time		(Note 5)				5	ms
Clock-Output SSB Phase Noise		Measured at 106.25MHz	100Hz		-90		dBc/Hz
			1kHz		-112		
			10kHz		-115		
			100kHz		-123		
			1MHz		-142		
			10MHz		-147		

Note 1: AC parameters are guaranteed by design and characterization.
Note 2: Outputs are enabled and unloaded.
Note 3: When LVPECL output is disabled to high impedance, the typical output off-current is <100µA for nominal LVPECL signal levels at the output.
Note 4: Measured with 50mV_{P-P} sinusoidal signal on the supply, from 10kHz to 1MHz.
Note 5: Including oscillator startup time and PLL acquisition time, measured after V_{CC} reaches 3.0V from power on.

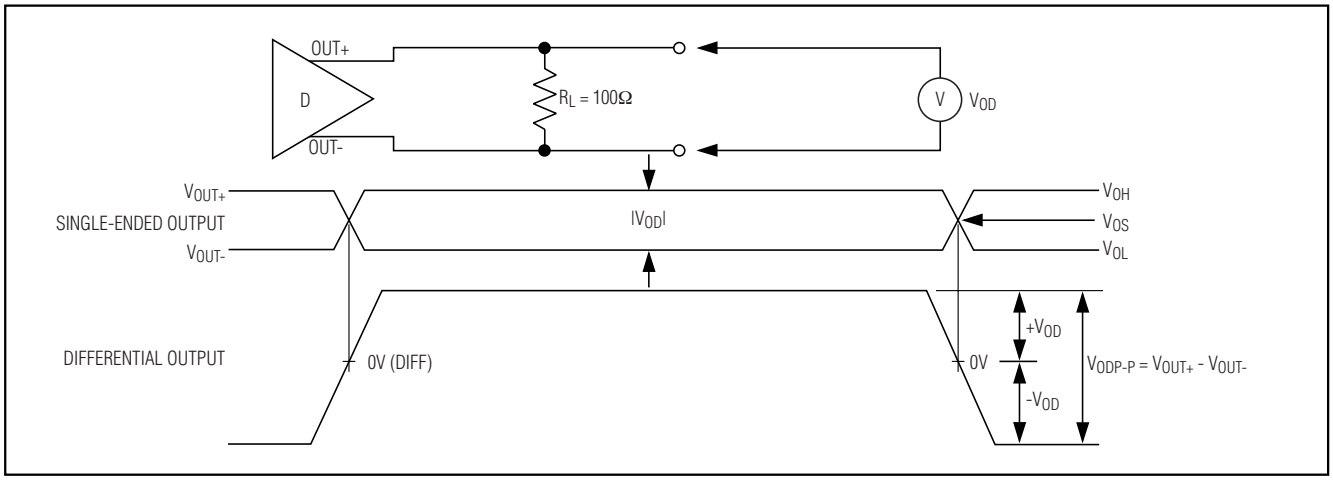


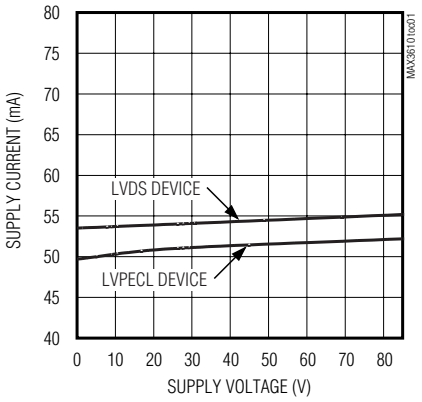
Figure 1. LVDS Swing Definitions

Low-Jitter 106.25MHz/212.5MHz Fibre-Channel Clock Generator

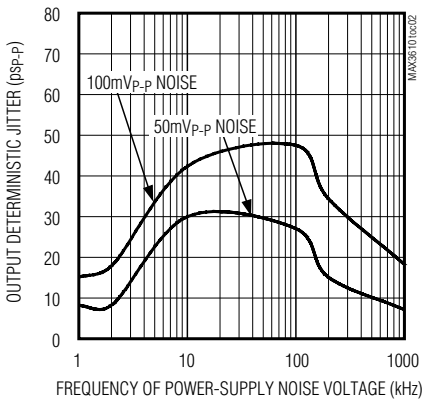
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

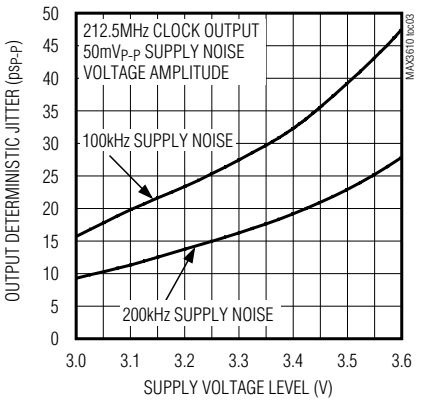
POWER-SUPPLY CURRENT vs. TEMPERATURE



OUTPUT DETERMINISTIC JITTER DUE TO POWER-SUPPLY NOISE vs. FREQUENCY



OUTPUT DETERMINISTIC JITTER DUE TO POWER-SUPPLY NOISE vs. SUPPLY VOLTAGE



Pin Description

PAD	NAME	FUNCTION
1, 2, 3, 6, 7, 9, 10, 11, 15–18	N.C.	No Connection
4	X1	Crystal Oscillator Input
5	X2	Crystal Oscillator Output
8	OE	Output Enable. On-chip pullup resistor. Connect OE to logic-high, V_{CC}, or leave open to enable the output clock. Connect OE to logic-low or GND to disable the output clock. LVPECL output clock is set to high impedance when disabled. LVDS output clock is latched to a differential high when disabled.
12	OUT-	Negative Clock Output, LVPECL or LVDS
13	GND	Ground
14	OUT+	Positive Clock Output, LVPECL or LVDS
19	FREQSET	Output Frequency Select. On-chip pullup resistor. Connect FREQSET to logic-high, V_{CC}, or leave open to set the output clock rate to 106.25MHz. Connect FREQSET to logic-low or GND to set the output clock rate to 212.5MHz.
20	V_{CC}	+3.3V Supply

Functional Diagram

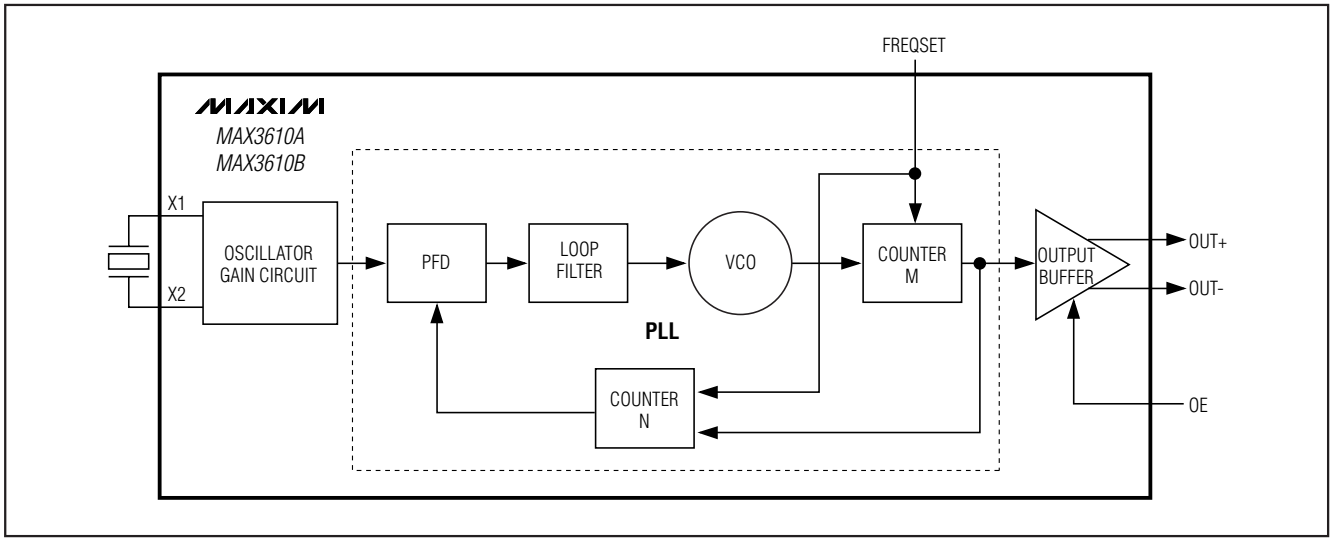


Figure 2. Functional Diagram

Detailed Description

The MAX3610 contains all of the blocks needed to form a precision Fibre-Channel clock except for the external crystal, which must be supplied separately. Figure 2 shows a functional block diagram of the MAX3610. The MAX3610 consists of a crystal oscillator, a low-noise PLL, selectable clock-divider circuitry, and an output buffer.

Optimal performance is achieved by integrating the crystal oscillator with a low-noise PLL. The PLL consists of a digital phase/frequency detector (PFD) and low-jitter generation VCO. The VCO signal is scaled by clock-divider circuitry and applied to the output buffer. The MAX3610 is available with either LVPECL or LVDS output buffers (see the *Ordering Information*).

Oscillator Gain Circuit

The input capacitance of the oscillator gain circuit is trimmed to 12pF of capacitance and produces oscillations at 26.5625MHz when interfaced with the appropriate external crystal (see Table 1 for the external crystal specifications).

PLL

The PLL generates a 1.7GHz high-speed clock signal based on the 26.5625MHz crystal oscillator output. Clock-divider circuit M generates the output clock by scaling the VCO output frequency. Clock-divider circuit N applies a scaled version of the output clock signal to the PFD. A TTL low applied to FREQSET, sets clock-divider M ratio to 16, and clock-divider N ratio to 8. With FREQSET pulled low, the output clock rate is 212.5MHz. A TTL high applied to FREQSET sets the clock-divider M ratio to 32, and clock-divider N ratio to 4. With FREQSET pulled high, the output clock rate is 106.25MHz.

Output Drivers

The MAX3610 is available with either LVPECL (MAX3610A) or LVDS (MAX3610B) output buffers. When not needed, the output buffers can be disabled. When disabled, the LVPECL output buffer goes to a high-impedance state. However, the LVDS outputs go to a differential 1 (OUT+ latched high and OUT- latched low) when the outputs are disabled.

Design Procedure

Crystal Resonator Specifications

The MAX3610 is designed to operate with an inexpensive fundamental mode crystal. Table 1 specifies the characteristics of a typical crystal to be interfaced with the MAX3610.

Low-Jitter 106.25MHz/212.5MHz Fibre-Channel Clock Generator

Table 1. Crystal Resonator Specifications

PARAMETER	VALUE
Crystal	Fundamental AT-cut
Nominal Oscillator Frequency	26.5625MHz
Shunt Capacitance (Co)	2pF
Co/Cs	280
Load Capacitance (Note 6)	12pF
Equivalent Series Resistance (ESR)	5Ω to 40Ω
Maximum Crystal Drive Level	500µW

Note 6: The load capacitance includes the oscillation-circuit input capacitance, as well as the parasitic capacitance caused from the assembling/packaging of the blank crystal and IC.

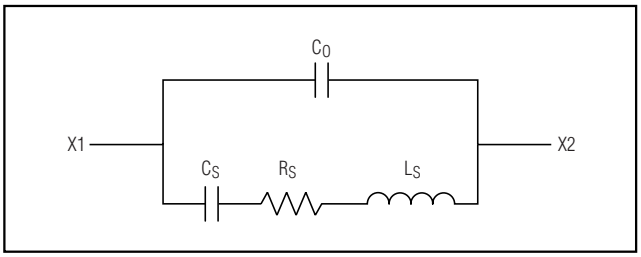


Figure 3. Equivalent Crystal Resonator Circuit Model

Applications Information

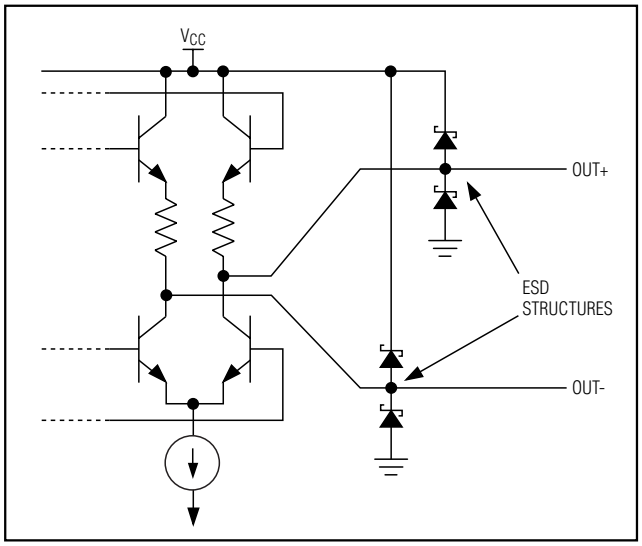


Figure 4. LVPECL Output Stage

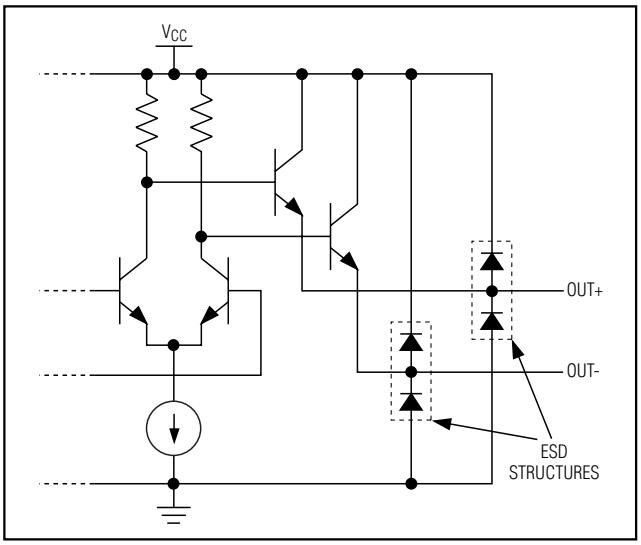


Figure 5. LVDS Output Stage

Table 2. Bond Pad Coordinates

PAD	NAME	COORDINATES	
		X (µm)	Y (µm)
BP1	N.C.	36.1	1362.4
BP2	N.C.	13.7	1193
BP3	N.C.	13.7	1060
BP4	X1	17.9	742.2
BP5	X2	16.5	613.4
BP6	N.C.	16.5	474.8
BP7	N.C.	16.5	344.6
BP8	OE	15.1	210.2
*BP9	N.C.	16.5	39.4
BP10	N.C.	167.7	33.8
BP11	N.C.	1119.7	36.6
BP12	OUT-	1613.9	50.6
BP13	GND	1613.9	187.8
BP14	OUT+	1613.9	325
BP15	N.C.	1612.5	613.4
BP16	N.C.	1611.1	753.4
BP17	N.C.	577.9	1366.6
BP18	N.C.	435.1	1369.4
BP19	FREQSET	306.3	1369.4
BP20	V_{CC}	169.1	1366.6

**Index pad*

Pad Information

Bond pad coordinates specify center pad location. All bond pad coordinates are referenced to the lower most left corner of the index pad (see *Application Note* HFAN 9.0).

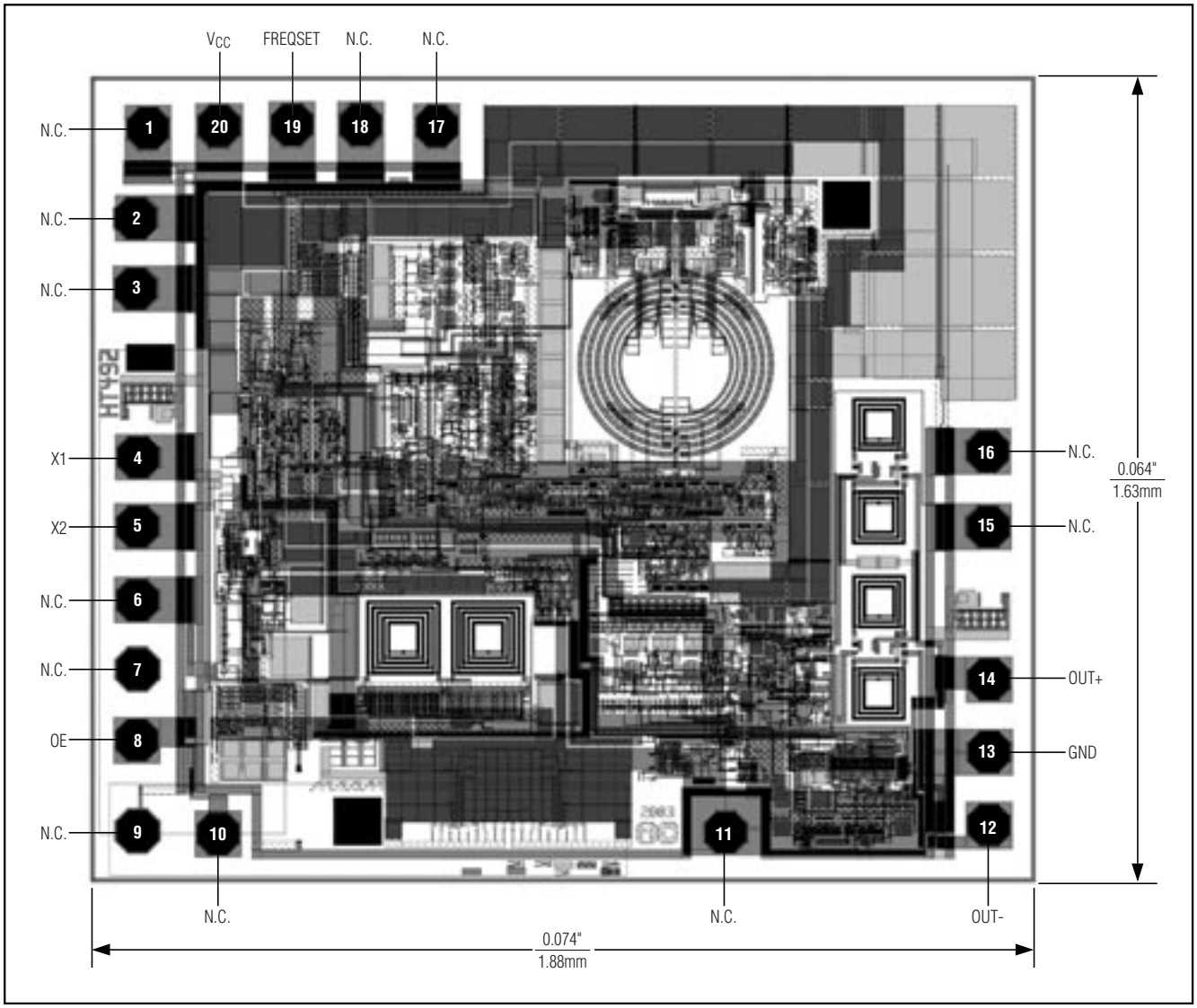
Low-Jitter 106.25MHz/212.5MHz Fibre-Channel Clock Generator

Chip Topography

TRANSISTOR COUNT: 2920
SUBST ELECTRICALLY ISOLATED
PROCESS: SiGe BIPOLAR
DIE SIZE: 1.88mm x 1.63mm

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.



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