SONY

CXD1270Q/R

Modem LSI with built-in DTMF for Cellular Use

Description

The CXD1270Q/R, is a cellular radio telephone IC, combines cellular radio telephone DATA SAT LSI CXD1231Q with DTMF signal generating circuit.

CXD1270Q
48 pin QFP (Plastic)

CXD1270R
48 pin VQFP (Plastic)

Features

- Conforms with North American AMPS standards and British TACS standards
- SAT detection circuit produces few errors even with weak electric field
- DTMF signal output by pulse density modulation

Structure

Silicon gate CMOS IC

Applications

AMPS/TACS cellular

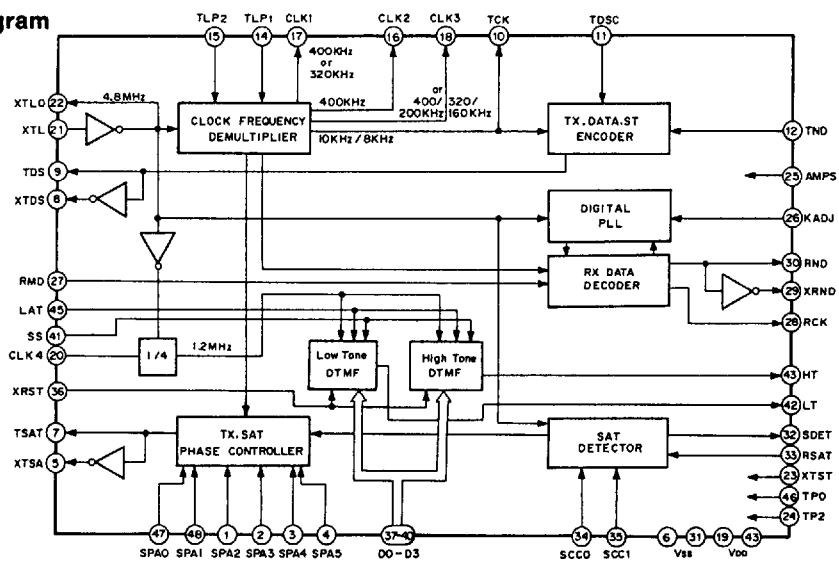
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	−0.3 to +7.0	V
• Input voltage	V_I	−0.3 to V_{DD}+0.3	V
• Output voltage	V_O	−0.3 to V_{DD}+0.3	V
• Operating temperature	Topr	−34 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

Recommended Operating Conditions

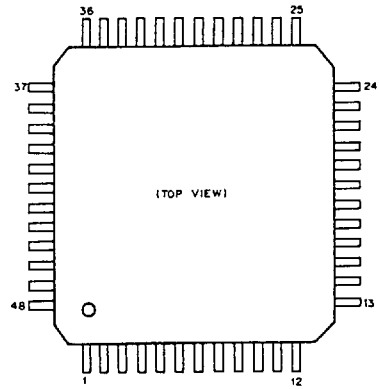
• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	−34 to +75	°C

Block Diagram



E90783A13 – ST

Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
1	SPA2	I	TX SAT phase compensation input 2
2	SPA3	I	TX SAT phase compensation input 3
3	SPA4	I	TX SAT phase compensation input 4
4	SPA5	I	TX SAT phase compensation input 5 (MSB)
5	XTSA	O	TSAT (Pin 7) inverting output
6	Vss	——	GND
7	TSAT	O	TX SAT output
8	XTDS	O	TDS (Pin 9) inverting output
9	TDS	O	TX manchester DATA and ST output
10	TCK	O	TX DATA and ST CLK output
11	TDSC	I	ON/OFF control input of RX manchester DATA and ST
12	TND	I	TX NRZ and DATA input
13	ENBL	I	High impedance control input of TDS (Pin 8) and XTDS (Pin 9)
14	TLP1	I	Frequency select 1 of CLK3 (Pin 18)
15	TLP2	I	Frequency select 2 of CLK3 (Pin 18)
16	CLK2	O	CLK output for SCF (400kHz)
17	CLK1	O	CLK output for SCF (AMPS; 400kHz, TACS; 320kHz)
18	CLK3	O	CLK output for SCF
19	V_{DD}	——	+5V
20	CLK4	O	1/4 frequency division output of crystal oscillator (1.2MHz)
21	XTL	I	Crystal oscillator input (4.8MHz)
22	XTLO	O	Crystal oscillator output
23	XTST	I	Test input (Normally fixed at low level)
24	TP2	I	

Pin No.	Symbol	I/O	Description
25	AMPS	I	AMPS/TACS mode select input (AMPS mode at open and TACS mode at low level)
26	KADJ	I	PLL lock range select input for RX manchester DATA decoder
27	RMD	I	RX manchester DATA input
28	RCK	O	CLK output extracted from RX DATA
29	XRND	O	RND (Pin 30) inverting output
30	RND	O	RX NRZ DATA output
31	Vss	——	GND
32	SDET	O	SAT detection output
33	RSAT	I	RX SAT input
34	SCC0	I	SAT collar code lower bit input
35	SCC1	I	SAT collar code upper bit input
36	XRST	I	Reset input (Active at low level)
37	D0	I/O	DTMF frequency set up bit input 0 (LSB) (Normally input mode)
38	D1	I/O	DTMF frequency set up bit input 1 (Normally input mode)
39	D2	I/O	DTMF frequency set up bit input 2 (Normally input mode)
40	D3	I/O	DTMF frequency set up bit input 3 (MSB) (Normally input mode)
41	SS	I/O	DTMF Start/Stop select input (Start at high level) (Normally input mode)
42	LT	O	DTMF low tone output
43	V_{DD}	——	+5V
44	HT	O	DTMF high tone output
45	LAT	I	DTMF set up LATCH input
46	TP0	I	Test input (Normally fixed at high level)
47	SPA0	I	TX SAT phase compensation input 0 (LSB)
48	SPA1	I	TX SAT phase compensation input 1

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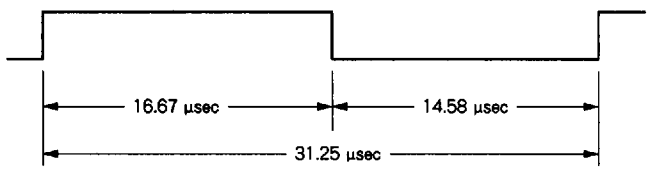
320kHz Clock Duty



CLK3 Chart

AMPS	Open ("H")		"L"	
TLP2	Don't care		"L"	
TLP1	"H"	"L"	"H"	"L"
CLK3	400kHz	200kHz	320kHz	160kHz

Electrical Characteristics

1) DC characteristics

(V_{DD}=5V ± 10%, Vss=0V, Topr=–34 to +75°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current	I_{DD}	At operation		5		mA
	I_{DDS}	At stand still V_{IH}=V_{DD}, V_{IL}=Vss			0.1	mA
Output voltage	V_{OH}	I_{OH}=–2mA	V_{DD}–0.5			V
	V_{OL}	I_{OL}=4mA			0.4	V
Input leak current 1	I_{LI1}	Normal pin	–10		10	μA
Input leak current 2	I_{LI2}	Bidirectional pin (During input)	–40		40	μA
Input voltage	V_{IHC}	CMOS input	0.7V_{DD}			V
	V_{ILC}				0.3V_{DD}	V
	V_{IHT}	TTL input	2.2			V
	V_{ILT}				0.8	V
	V_{T^+}	Schmitt trigger input	0.8V_{DD}			V
	V_{T^-}				0.2V_{DD}	V
	V_{T^+}–V_{T^-}		0.7	0.9		V

2) I/O level of each pin

I/O level		Pin name
Input level	CMOS level	SPA0 to SPA5, TDSC, TND, TLP1, TLP2, XTST, TP2, AMPS, KADJ, RMD, RSAT, SCC0, SCC1, D0 to D3, SS, LAT, TP0
	TTL level	ENBL
	Schmitt trigger	XRST
Output level	CMOS level	XTSA, TSAT, TDS, XTDS, TCK, CLK1 to CLK4, RCK, XRND, RND, SDET
	Tri-state	LT, HT

3) Oscillation cell electrical characteristics

(V_{DD}=5V ± 10%, Vss=0V, Topr=–34 to +75°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logical threshold	LVth			V_{DD}/2		V
Input voltage	V_{IH}		0.7V_{DD}			V
	V_{IL}				0.3V_{DD}	V
Incorporated feedback resistance	R_{FB}	V_{IH}=Vss or V_{DD}	500K	2M	5M	Ω
Output voltage	V_{OH}	I_{OH}=–1mA	V_{DD}/2			V
	V_{OL}	I_{OL}=1mA			V_{DD}/2	V

4) I/O capacitance

(V_{DD}=V_I=0V, f_M=1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			9	pF
Output pin	C_{OUT}			11	pF
I/O pin	$C_{I/O}$			11	pF

5) Pull up/down processing pin

Processing	Pin name
Pull up	SPA0 to SPA5, ENBL, TLP2, AMPS
Pull down	TND

6) AC characteristics

(V_{DD}=5V ± 10%, Vss=0V, Topr=–34 to +75℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Set up time for D0 to D3 LAT			30			ns

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Functions

CXD1270Q/R is a DATA and SAT LSI designed for the cellular radio telephone system. Combined with the switched capacitor filter CXD1230M or CXD1237Q/R it conforms with North American AMPS (Advanced Mobile Phone Service) and British TACS (Total Access Communication System) standards.
It features the following functions.

1) Decoding of the received DATA.
2) Detection of the received SAT.
3) SAT transmission in the same frequency and phase as for received SAT.
4) Encoding of the transmitting DATA and ST.

The following is description of each function.

Decoding of the received DATA

With the cellular radio telephone system, DATA for selecting a channel is exchanged between land and mobile stations during cell movement after circuit connection. This DATA is called WIDE BAND DATA coded in the Manchester code. Transfer speed is 20kbaud for AMPS standards and 16kbaud for TACS standards. The following diagram shows the logical values "1" and "0" of the Manchester code.

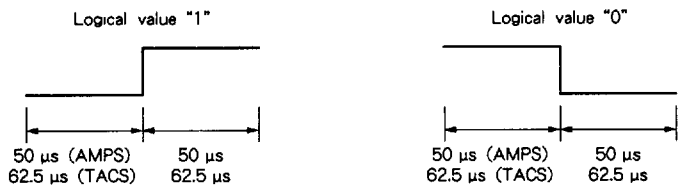


Fig. 1. Manchester code

To decode DATA input in this Manchester code, clock components are extracted by DPLL and the second half values of each bit are picked up using the clock. The decoded DATA is output as NRZ data from the output RND (Pin 30) and XRND (Pin 29) and its bit-clock is output from the output RCK (Pin 28).
Timing of RCK with RND or XRND is shown in Fig. 2.

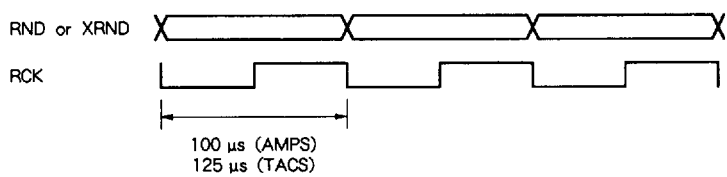


Fig. 2. Timing of RCK with RND or XRND

Detection of the received SAT

With the cellular radio telephone system, sine wave signals called SAT (Supervisory Audio Tone) are exchanged between land and mobile stations after radio link with either AMPS or TACS standards. SAT has three waves, 5.97kHz, 6.00kHz and 6.03kHz; frequency is selected from those during cell movement. The selected one is notified in SAT collar code to the mobile station by land station. During circuit connection, land and mobile stations confirm each other through reception of the designated SAT frequency.

When SAT signal with the frequency designated in SAT collar code is detected, SDET (Pin 32) becomes "H".

SAT transmission in the same frequency and phase as for received SAT

The land station confirms a mobile station through receiving SAT signal in the same frequency and phase as it has transmitted. The mobile station is required to transmit SAT signal in the same frequency and phase as received. For this purpose, the mobile station transmits the signal by phase-correcting DPLL output locked in the received SAT. Connecting the amount of phase depends on the transmitting circuit delay; this is correctly executed by varying 64 stages in 3.6° steps (0° to 226.8°) and then further shifting the phase by 180° by means of selecting the output TSAT pin (Pin 7) and XTSA (inverting output of TSAT, Pin 5). Thus the phase can be compensated from 0° to 360° in 3.6° steps.

Table below shows the compensated value of the phase assuming that the TSAT output for (SPA5, SPA4, SPA3, SPA2, SPA1, SPA0) = (0, 0, 0, 0, 0, 0) is standard.

SPA5	SPA4	SPA3	SPA2	SPA1	SPA0	Phase delay	
						TSAT	XTSA
0	0	0	0	0	0	0°	180°
0	0	0	0	0	1	3.6°	183.6°
0	0	0	0	1	0	7.2°	187.2°
⋮						⋮	⋮
1	1	0	0	0	0	172.8°	352.8°
1	1	0	0	0	1	176.4°	356.4°

Table 1. Phase delay at pins TSAT and XTSA assuming that TSAT output for (SPA5, SPA4, SPA3, SPA2, SPA1, SPA0) = (0, 0, 0, 0, 0, 0) is standard.

Encoding of the transmitting DATA and ST

ST (Signaling Tone) is a signal transmitted when conversation ends or when the bell is rang. The frequency is 10kHz for AMPS and 8kHz for TACS standards. It is output from TDS (Pin 9) and XTDS (Pin 8) with the DATA and ST (NRZ) input to TND (Pin 12), in synchronization with the clock output from TCK (Pin 10), and encoded in the Manchester code. However, it does not transmit the encoded data when the control input TDSC (Pin 11) is at "L" but fixes TDS to "H" and XTDS to "L".

Timing of TCK and TND is shown in Fig. 3.

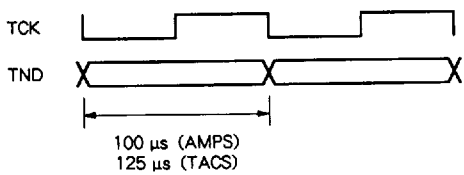


Fig. 3. Timing of TCK and TND

DTMF Block

(1) Setting of frequency (frequency division ratio)

Low Tone (Hz)	Frequency division ratio N	Realized frequency f (Hz)	D3	D2	D1	D0
697	143	699.3	0	0	0	0
770	130	769.2	0	0	0	1
852	117	854.7	0	0	1	0
941	106	943.3	0	0	1	1
2K	50	2000	0	1	0	0

High Tone (Hz)	Frequency division ratio N	Realized frequency f (Hz)	D3	D2	D1	D0
1209	83	1204.8	1	0	0	0
1336	75	1333.3	1	0	0	1
1477	68	1470.6	1	0	1	0
1633	61	1639.3	1	0	1	1
2K	50	2000	1	1	0	0

Note) Besides the frequency for LT and HT, employed for the usual push button, a 2kHz frequency can be output at both LT and HT.

(2) Setting of LT, HT Start/Stop

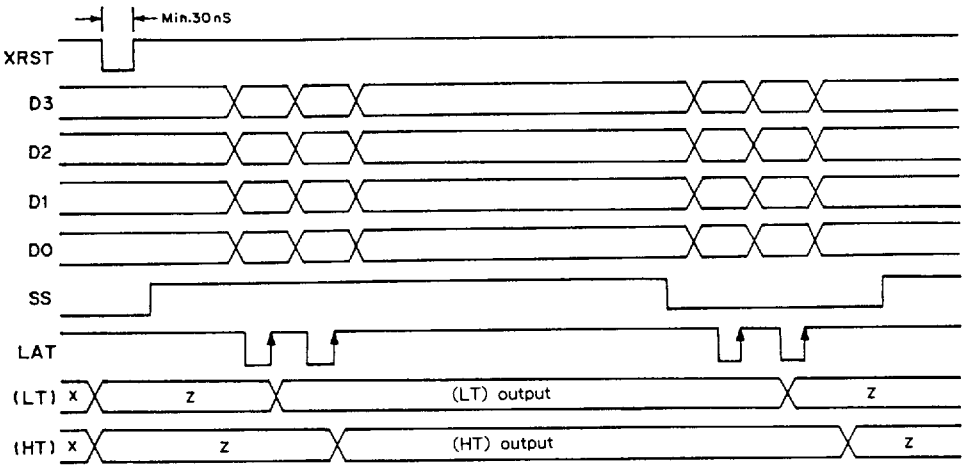
Start/Stop for both LT and HT is controlled through SS input signal.

	SS	LAT
LT, HT Start	1	⌐
LT, HT Stop	0	⌐

(3) LT, HT output

LT and HT outputs are output by pulse density modulation system. This system means frequency, obtained at frequency division ratio N determined by D0 to D3, divided 1/12 frequency division sine wave counter, and outputs pulse waveform varied with density suitable for each count value. These outputs, tri-state output system, is controlled through start/stop signal.

(4) Timing chart



Note) LT, HT distinction is controlled through D3.
D3= "High" ...HT, D3= "Low" ...LT
After resetting, at the point where the first SS= "High" is read at LAT rising edge, LT (HT) output starts. At the same time data of D0 to D3 is loaded in and the frequency division ratio is set.
Also, SS= "Low" is read and LT (HT) is stopped. In such case, for D3 only it is necessary to set "Low" and "High" for the respective distinction of LT and HT. However D0 to D2 is ignored.

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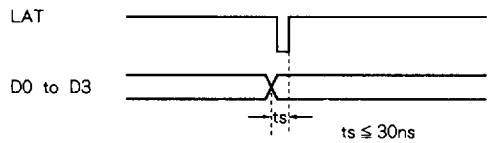
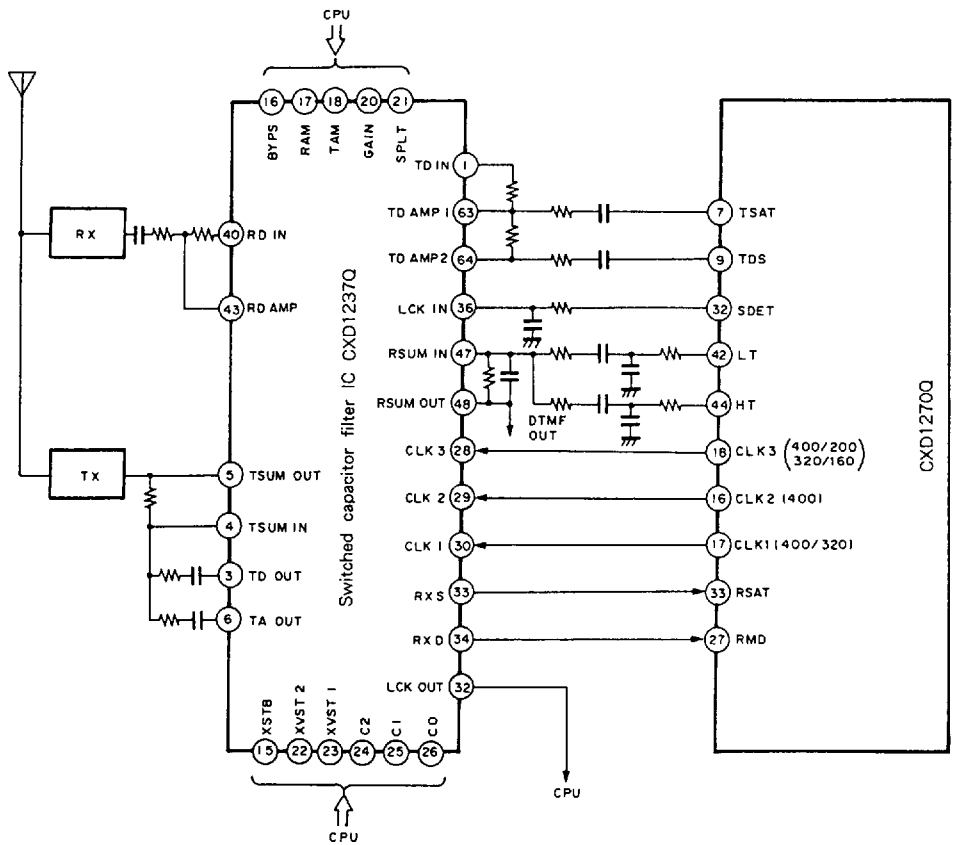
AC Characteristics Timing Diagram

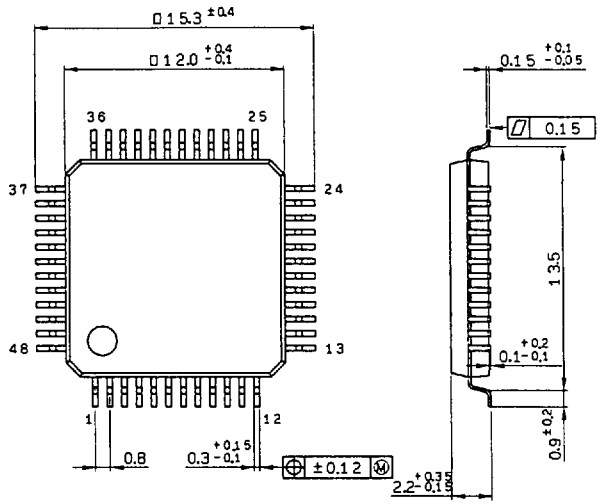


CXD1270Q/R and CXD1237Q/R Connecting Example (CXD1237: QFP Pin No.)



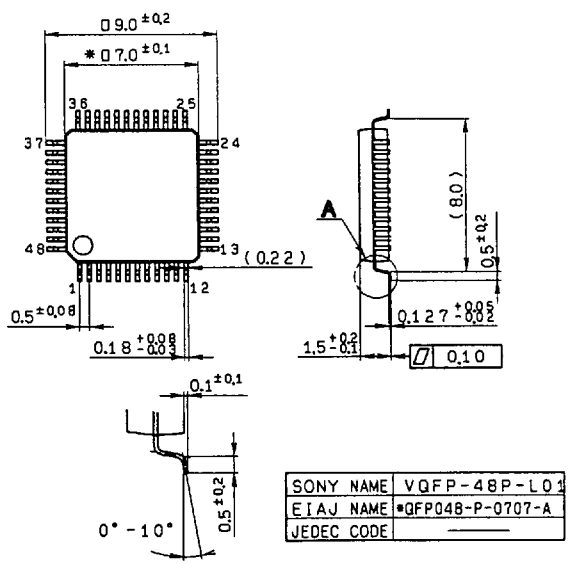
Package Outline Unit : mm

CXD1270Q 48pin QFP (Plastic) 0.7g



SONY NAME	QFP-48P-L04
EIAJ NAME	*QFP048-P-1212-B
JEDEC CODE	———

CXD1270R 48pin VQFP (Plastic) 0.2g



SONY NAME	VQFP-48P-L01
EIAJ NAME	*QFP048-P-0707-A
JEDEC CODE	———

Detailed diagram of A

Note) Dimensions marked with * does not include resin residue.

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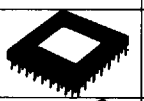
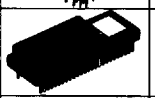
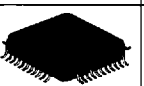
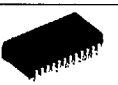
Package Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	DIP	DUAL IN-LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		SIP	SINGLE IN LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		ZIP	ZIG ZAG IN-LINE PACKAGE		P	2.54mm (100MIL) Zig-Zag in-line	Through Hole Lead	1-direction
		PGA	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	Package under side
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN-LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
		SZIP	SHRINK ZIG-ZAG IN-LINE PACKAGE		P	1.778mm (70MIL) Zig-Zag in-line	Through Hole Lead	1-direction
Surface mounted	Standard flat package	QFP	QUAD FLAT L LEADED PACKAGE		P C	1.0mm 0.8mm 0.65mm	Gull-Wing	4-direction
		SOP	SMALL OUTLINE L-LEADED PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull-Wing	2-direction
		TSOP	THIN SMALL OUTLINE PACKAGE		P	0.5mm (0.55mm)	Gull-Wing	2-direction
	Standard chip carrier	QFJ	QUAD FLAT J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	4-direction
		QFN	QUAD FLAT NON-LEADED PACKAGE		C	1.27mm (50MIL)	Leadless	Package under side

*P·····Plastic, C···Ceramic

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