

MOS INTEGRATED CIRCUIT μ PD75104A, 75108A

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

μ PD75108A is a 4-bit single-chip CMOS microcomputer having a data processing capability comparable to that of an 8-bit microcomputer. Operating at high speeds, the microcomputer allows data to be manipulated in units of 1, 4, or 8 bits. In addition, various bit manipulation instructions are provided to reinforce I/O manipulation capability. Equipped with I/Os for interfacing with peripheral circuits operating on a different supply voltage, outputs that can directly drive LEDs, and analog inputs, μ PD75108A is suitable for controlling such small equipments as cameras and VCRs.

Detailed functions are described in the following user's manual. Be sure to read it for designing.
 μ PD751XX Series User's Manual: IEM-922

FEATURES

- Internal memory
 - Program memory (ROM)
 - : 8064 $\times$ 8 bits (μ PD75108A)
 - : 4096 $\times$ 8 bits (μ PD75104A)
 - Data memory (RAM)
 - : 512 $\times$ 4 bits (μ PD75108A)
 - : 320 $\times$ 4 bits (μ PD75104A)
- Architecture "75X" rivaling 8-bit microcomputers
- 43 systematically organized instructions
 - A wealth of bit manipulation instructions
 - 8-bit data transfer, compare, operation, increment, and decrement instructions
 - 1-byte relative branch instructions
 - GETI instruction executing 2-/3-byte instruction with one byte
- High speed. Minimum instruction execution time: 0.95 μ s (at 4.19 MHz, 5V)
- Instruction execution time change function: 0.95 μ s/1.91 μ s/15.3 μ s (at 4.19 MHz)
- I/O port pins as many as 58
- Three channels of 8-bit timers
- 8-bit serial interface
- Multiplexed vector interrupt function

Unless there are differences among μ PD75104A and 75108A functions, μ PD75108A is treated as the representative model throughout this manual.

The information in this document is subject to change without notice.

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD75104AGC-xxx-AB8	64-pin plastic QFP (□ 14 mm)	Standard
μPD75108AGC-xxx-AB8	64-pin plastic QFP (□ 14 mm)	Standard

Remarks: xxx is ROM code number.

Please refer to "Quality Grade on NEC Semiconductor Devices" (Document Number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

FUNCTIONAL OUTLINE

Item		Specifications
Number of Basic Instructions		43
Minimum Instruction Execution Time		Changeable in three steps: 0.95 μs, 1.91 μs, and 15.3 μs at 4.19 MHz
Internal Memory	ROM	8064 × 8 bits (μPD75108A), 4096 × 8 bits (μPD75104A)
	RAM	512 × 4 bits (μPD75108A), 320 × 4 bits (μPD75104A)
General-Purpose Register		(4 bits × 8) × 4 banks or (8 bits × 4) × 4 banks
Accumulator		Three accumulators selectable according to the bit length of manipulated data: • 1-bit accumulator (CY), 4-bit accumulator (A), and 8-bit accumulator (XA)
I/O Port		58 port pins • CMOS input pins (Pull-up resistor can be connected to 4 out of 10 pins in bit units.): 10 • CMOS I/O pins (can directly drive LEDs. Pull-up resistors can be connected to 24 out of 32 pins in bit units.): 32 • Medium voltage N-ch open-drain I/O pins: 12 (can directly drive LEDs. Pull-up resistors can be connected in bit units.) • Comparator input pins (4-bit accuracy): 4
Timer/Counter		• 8-bit timer/event counter × 2 • 8-bit basic interval timer (can be used as watchdog timer)
Serial Interface		• 8 bits • LSB first/MSB first mode selectable • Two transfer modes (transfer/reception and reception only modes)
Vector Interrupt		External: 3, Internal: 4
Test Input		External: 2
Standby		• STOP and HALT modes
Instruction Set		• Various bit manipulation instructions (set, reset, test, Boolean operation) • 8-bit data transfer, compare, operation, increment, and decrement • 1-byte relative branch instructions • GETI instruction constituting 2 or 3-byte instruction with 1 byte
Others		• Power-ON reset circuit (mask option) • Bit manipulation memory (bit sequential buffer: 16 bits)
Package		• 64-pin plastic QFP (□ 14 mm)

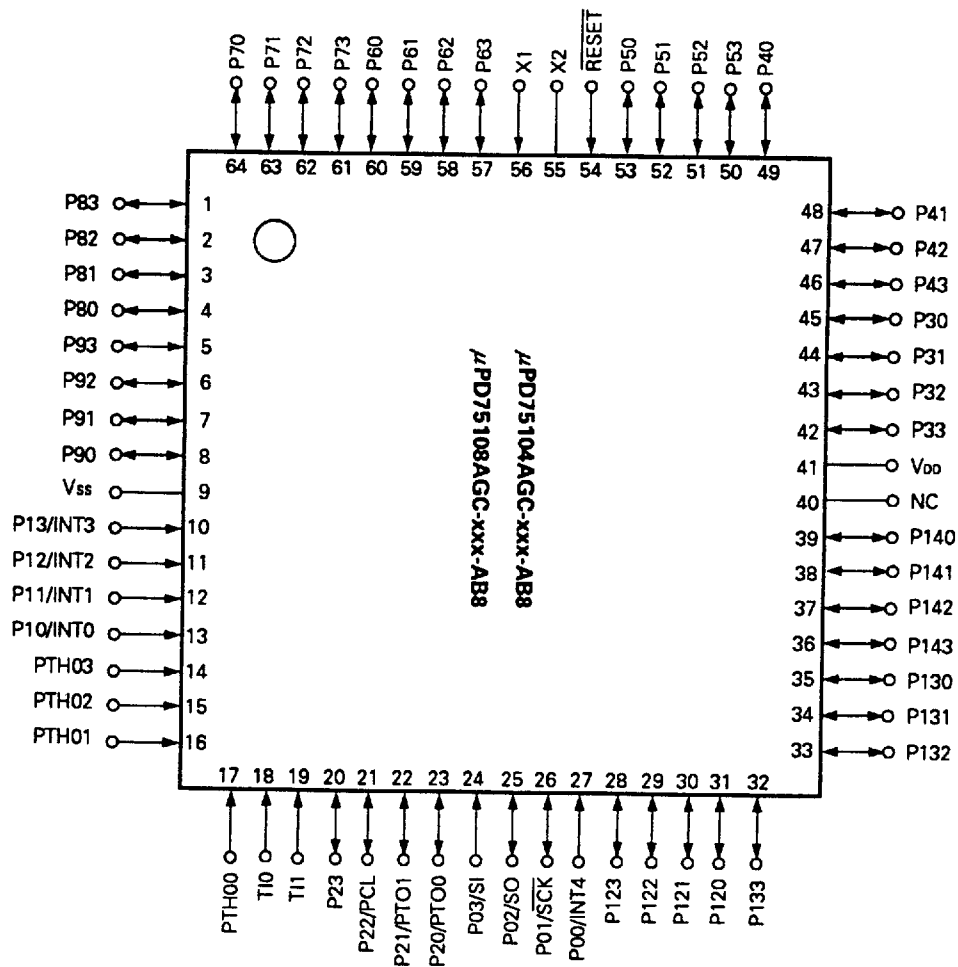
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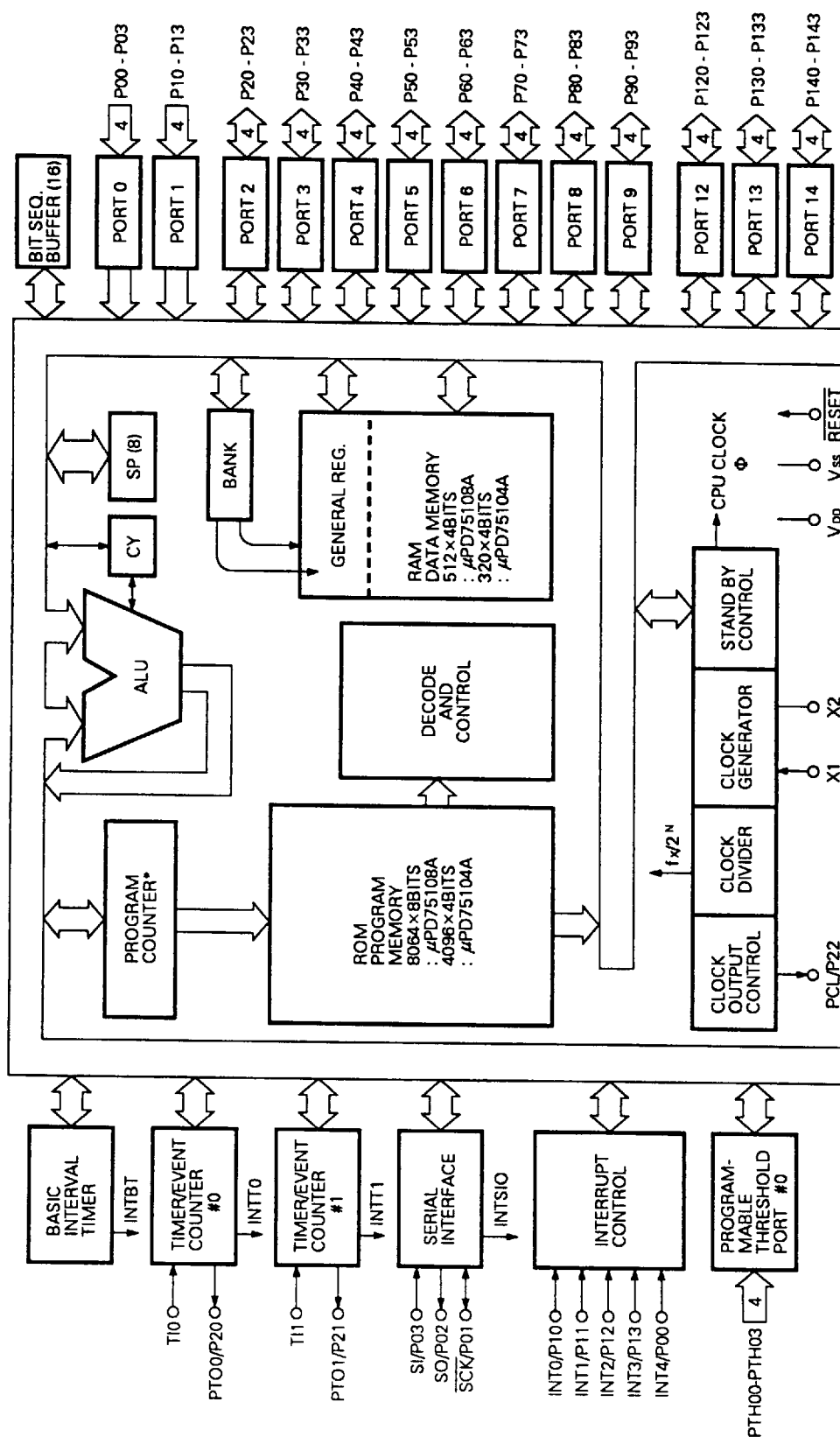
1. PIN CONFIGURATION (TOP VIEW)

- 64-Pin Plastic QFP (□ 14 mm)



P00-P03	: Port 0	SCK	: Serial Clock Input/Output
P10-P13	: Port 1	SO	: Serial Output
P20-P23	: Port 2	SI	: Serial Input
P30-P33	: Port 3	PTO0, PTO1	: Timer Output
P40-P43	: Port 4	PCL	: Clock Output
P50-P53	: Port 5	PTH00-PTH03	: Comparator Input
P60-P63	: Port 6	INT0, INT1, INT4	: External Vector Interrupt Input
P70-P73	: Port 7	INT2, INT3	: External Test Input
P80-P83	: Port 8	TI0, TI1	: Timer Input
P90-P93	: Port 9	X1, X2	: Oscillation Pin
P120-P123	: Port 12	RESET	: Reset Input
P130-P133	: Port 13	NC	: No Connection
P140-P143	: Port 14	VDD	: Positive Power Supply
		VSS	: GND

2. BLOCK DIAGRAM



*: 13 bits: μPD75108A
12 bits: μPD75104A

3. PIN FUNCTIONS

3.1 PORT PINS

Pin Name	I/O	Shared with:	Function	8-Bit I/O	At Reset	I/O Circuit Type*1	
P00	Input	INT4	4-bit input port (PORT 0)	x	Input	Ⓑ	
P01	I/O	SCK				Ⓕ	
P02	I/O	SO				E	
P03	Input	SI				Ⓑ	
P10	Input	INT0	4-bit input port (PORT 1)		Input*2	Ⓑ-A	
P11		INT1					
P12		INT2					
P13		INT3					
P20**	I/O	PTO0	4-bit I/O port (PORT 2)	x	Input	E	
P21**		PTO1					
P22**		PCL					
P23**		—					
P30-P33**	I/O	—	4-bit programmable I/O port (PORT 3) Can be specified for input or output bitwise.		Input	E	
P40-P43**	I/O	—	4-bit I/O port (PORT 4)		o	Input*2	E-A
P50-P53**	I/O	—	4-bit I/O port (PORT 5)			Input*2	E-A
P60-P63**	I/O	—	4-bit programmable I/O port (PORT 6) Can be specified for input or output bitwise.		o	Input*2	E-A
P70-P73**	I/O	—	4-bit I/O port (PORT 7)	Input*2		E-A	
P80-P83**	I/O	—	4-bit I/O port (PORT 8)	o	Input*2	E-A	
P90-P93**	I/O	—	4-bit I/O port (PORT 9)		Input*2	E-A	
P120-P123**	I/O	—	4-bit N-ch open-drain I/O port (PORT 12) Built-in pull-up resistors can be specified in bit units (by mask option). Open-drain withstanding voltage: 12 V	o	Input*2	M	
P130-P133**	I/O	—	4-bit N-ch open-drain I/O port (PORT 13) Built-in pull-up resistors can be specified in bit units (by mask option). Open-drain withstanding voltage: 12 V		Input*2	M	
P140-P143**	I/O	—	4-bit N-ch open-drain I/O port (PORT 14) Built-in pull-up resistors can be specified in bit units (by mask option). Open-drain withstanding voltage: 12 V	—	Input*2	M	

*1: Circles indicate Schmitt trigger input pins.

2: With pull-up resistor connected: high level

Without pull-up resistor connected: high impedance

3: Can directly drive LEDs.

3.2 PINS OTHER THAN PORTS

Pin Name	I/O	Shared with:	Function	At Reset	I/O Circuit Type*1
PTH00-PTH03	Input	—	4-bit variable threshold voltage analog input port	—	N
TI0	Input	—	External event pulse inputs for timer/event counter. Also serves as edge-detected vector interrupt input. 1-bit input also possible.	—	Ⓑ
TI1					
PTO0	I/O	P20	Outputs for timer/event counter	Input	E
PTO1		P21			
$\overline{\text{SCK}}$	I/O	P01	Serial clock I/O	Input	Ⓕ
SO	I/O	P02	Serial data output	Input	E
SI	Input	P03	Serial data input	Input	Ⓑ
INT4	Input	P00	Edge-detected vectored interrupt input (both rising and falling edges detected)	Input	Ⓑ
INT0	Input	P10	Edge-detected vectored interrupt inputs (valid edge selectable)	Input*2	Ⓑ-A
INT1		P11			
INT2	Input	P12	Edge-detected testable inputs (rising edge detected)	Input*2	Ⓑ-A
INT3		P13			
PCL	I/O	P22	Clock output	Input	E
X1, X2	—	—	Crystal/ceramic system clock oscillator connections. Input external clock to X1, and signal in reverse phase with X1 to X2.	—	—
$\overline{\text{RESET}}$	Input	—	System reset input (low level active type)	—	Ⓑ
NC	—	—	No Connection	—	—
V _{DD}	—	—	Positive power supply	—	—
V _{SS}	—	—	GND	—	—

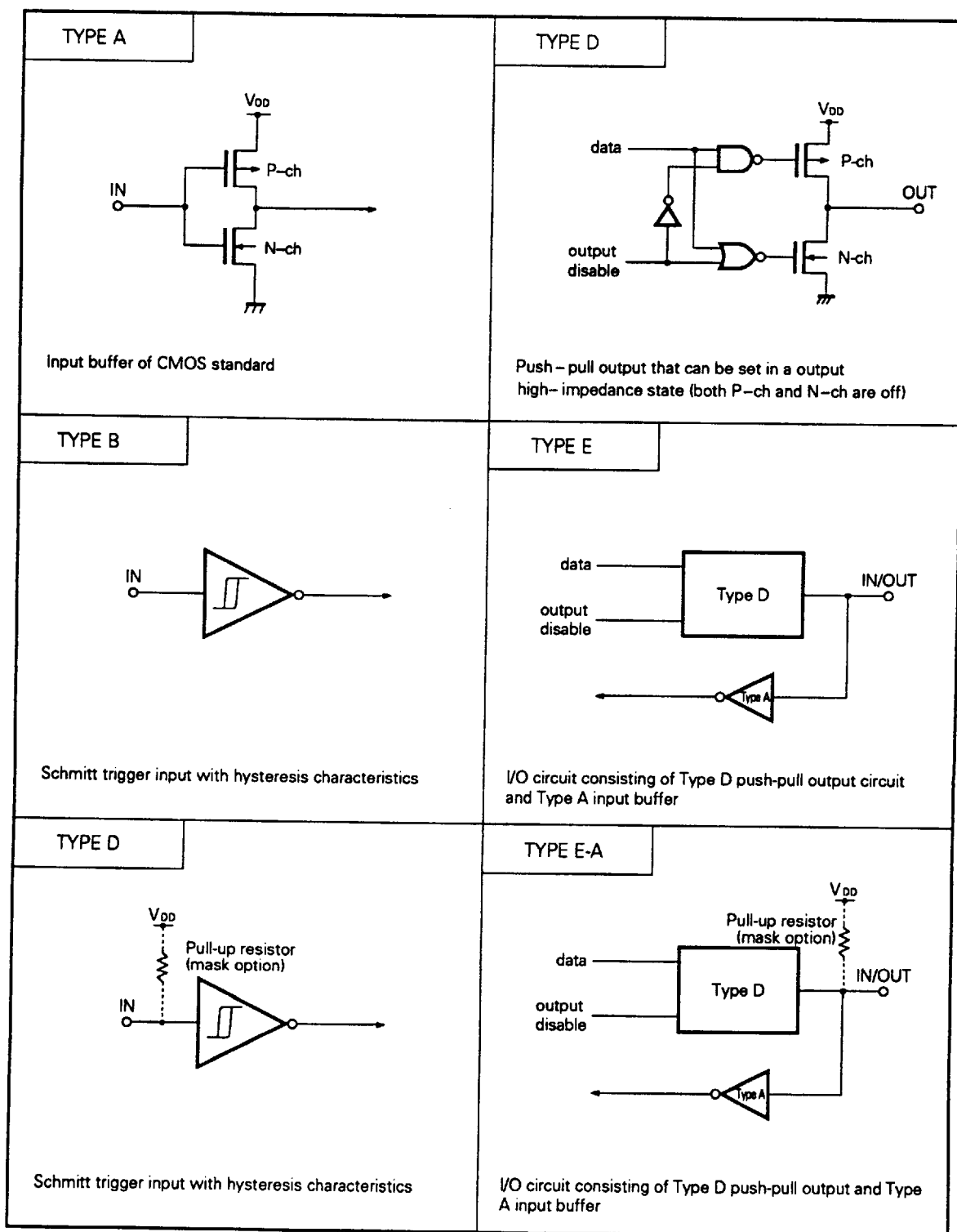
*1: Circles indicate Schmitt trigger input pins.

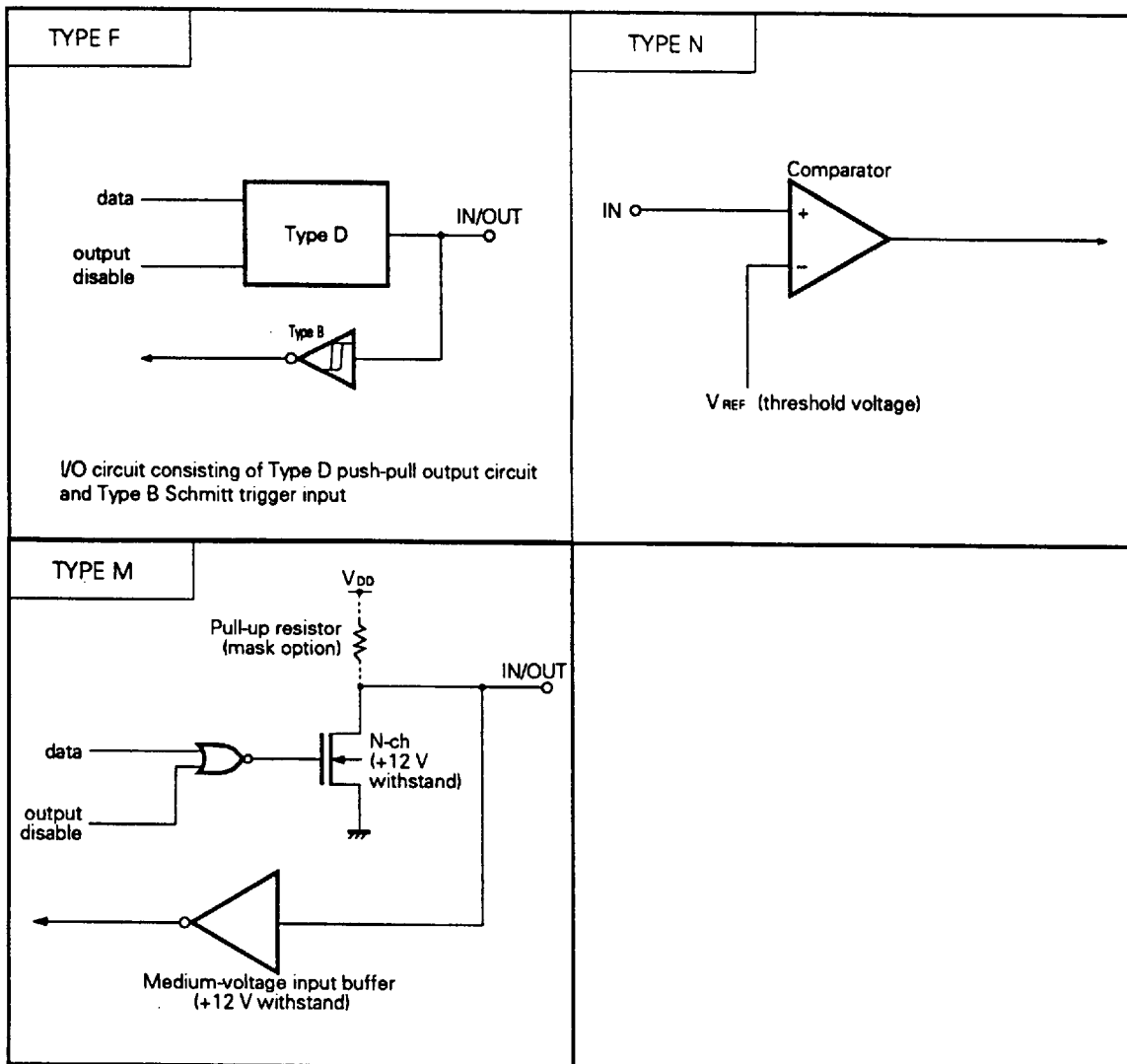
2: With pull-up resistor connected: high level

Without pull-up resistor connected: high impedance

3.3 PIN INPUT/OUTPUT CIRCUITS

The following shows a simplified input/output circuit diagram for each pin of the μ PD75108A.





3.4 RECOMMENDED PROCESSING OF UNUSED PINS

Pin	Recommended connections
PTH00-PTH03	Connect to V _{ss} or V _{DD}
TI0	
TI1	
P00	Connect to V _{ss}
P01-P03	Connect to V _{ss} or V _{DD}
P10-P13	• Connect to V_{DD} when a pull-up resistor is provided. • Connect to V_{ss} when a pull-up resistor is not provided.
P20-P23	• Input: Connect to V_{ss} • Output: Open
P30-P33	
P40-P43	• When a pull-up resistor is provided: Input: Connect to V_{DD} Output: Open • When a pull-up resistor is not provided: Input: Connect to V_{ss} or V_{DD} Output: Open
P50-P53	
P60-P63	
P70-P73	
P80-P83	
P90-P93	
P120-P123	
P130-P133	
P140-P143	
RESET	Connect to V _{DD} *
NC	Open or connect to V _{DD}

*: Connect this pin to the V_{DD} pin only when a power-ON reset circuit is provided as a mask option.

3.5 NOTES ON USING THE P00/INT4, AND $\overline{\text{RESET}}$ PINS

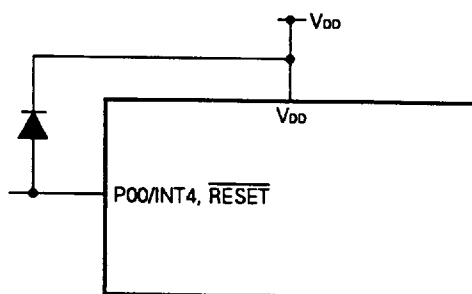
In addition to the functions described in Sections 3.1 and 3.2, an exclusive function for setting the test mode, in which the internal functions of the μ PD75108A are tested (solely used for IC tests), is provided to the P00/INT4 and $\overline{\text{RESET}}$ pins.

If a voltage exceeding V_{DD} is applied to either of these pins, the μ PD75108A is put into test mode. Therefore, even when the μ PD75108A is in normal operation, if noise exceeding the V_{DD} is input into any of these pins, the μ PD75108A will enter the test mode, and this will cause problems for normal operation.

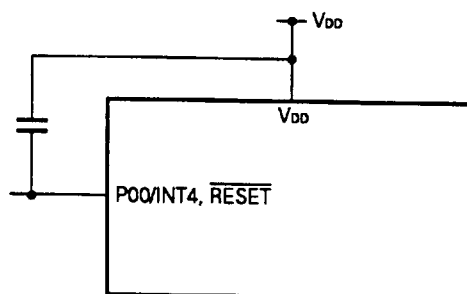
As an example, if the wiring to the P00/INT4 pin or the $\overline{\text{RESET}}$ pin is long, stray noise may be picked up to these pins and the above mentioned problem may occur.

Therefore, all wiring to these pins must be made short enough to not pick up stray noise. If noise cannot be avoided, suppress the noise using a capacitor or diode as shown in the figure below.

- Connect a diode across P00/INT4 and $\overline{\text{RESET}}$, and V_{DD} .



- Connect a capacitor across P00/INT4 and $\overline{\text{RESET}}$, and V_{DD} .



4. MEMORY CONFIGURATION

- Program memory (ROM) ... 8064×8 bits (0000H-1F7FH) : μ PD75108A
... 4096×8 bits (0000H-0FFFH) : μ PD75104A
 - 0000H, 0001H: Vector table to which address from which program is started is written after reset
 - 0002H-000BH: Vector table to which address from which program is started is written after interrupt
 - 0020H-007FH: Table area referenced for GETI instruction
- Data memory (RAM)
 - Data area 512×4 bits (000H-1FFH) : μ PD75108A
 320×4 bits (000H-13FH) : μ PD75104A
 - Peripheral hardware area 128×4 bits (F80H-FFFH)

(a) μPD75108A

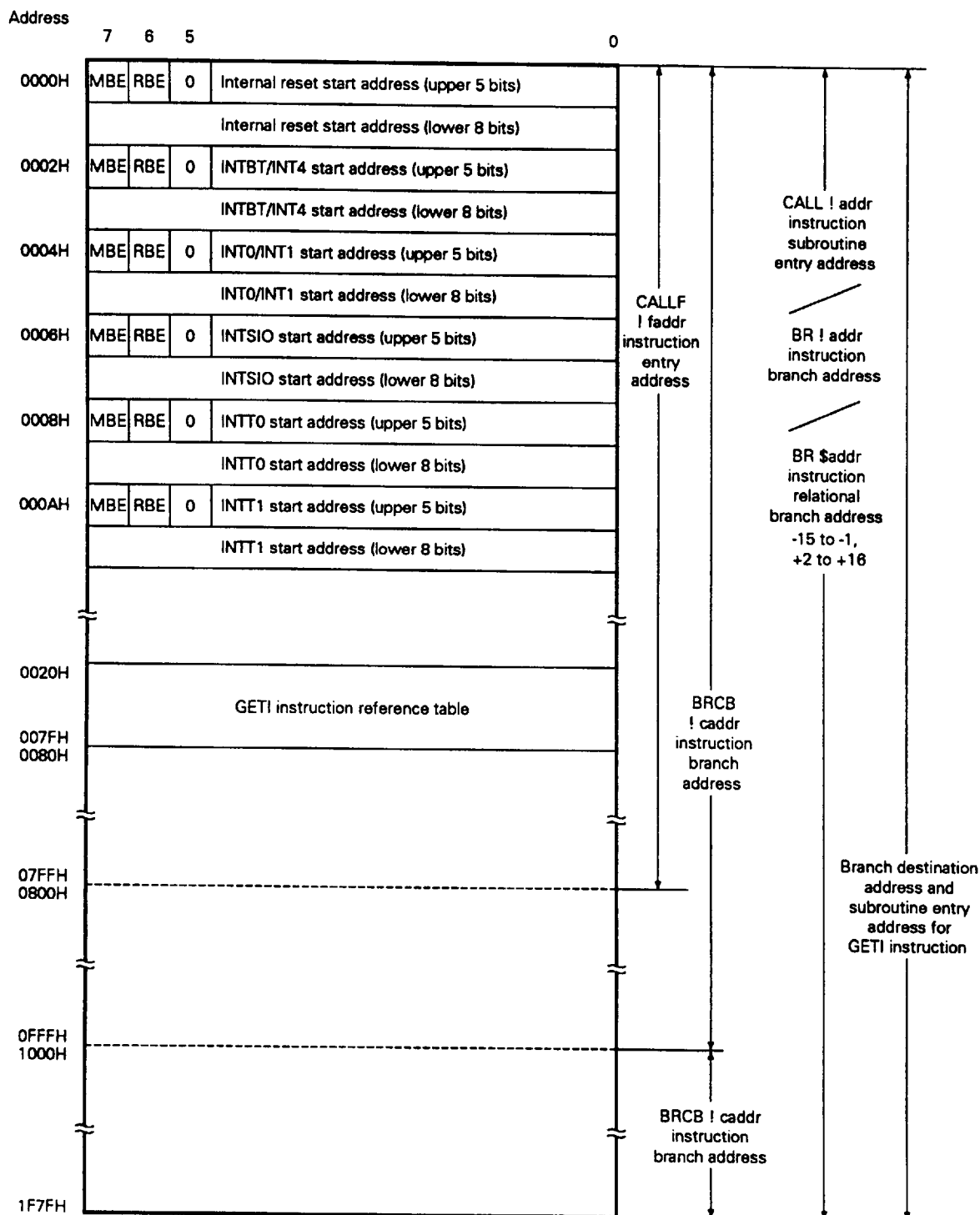


Fig. 4-1 Program Memory Map (1/2)

Remarks: In addition to the above addresses, program can be branched to addresses specified by the PC with the contents of its lower 8 bits changed by BR PCDE or BR PCXA instruction.

(b) μPD75104A

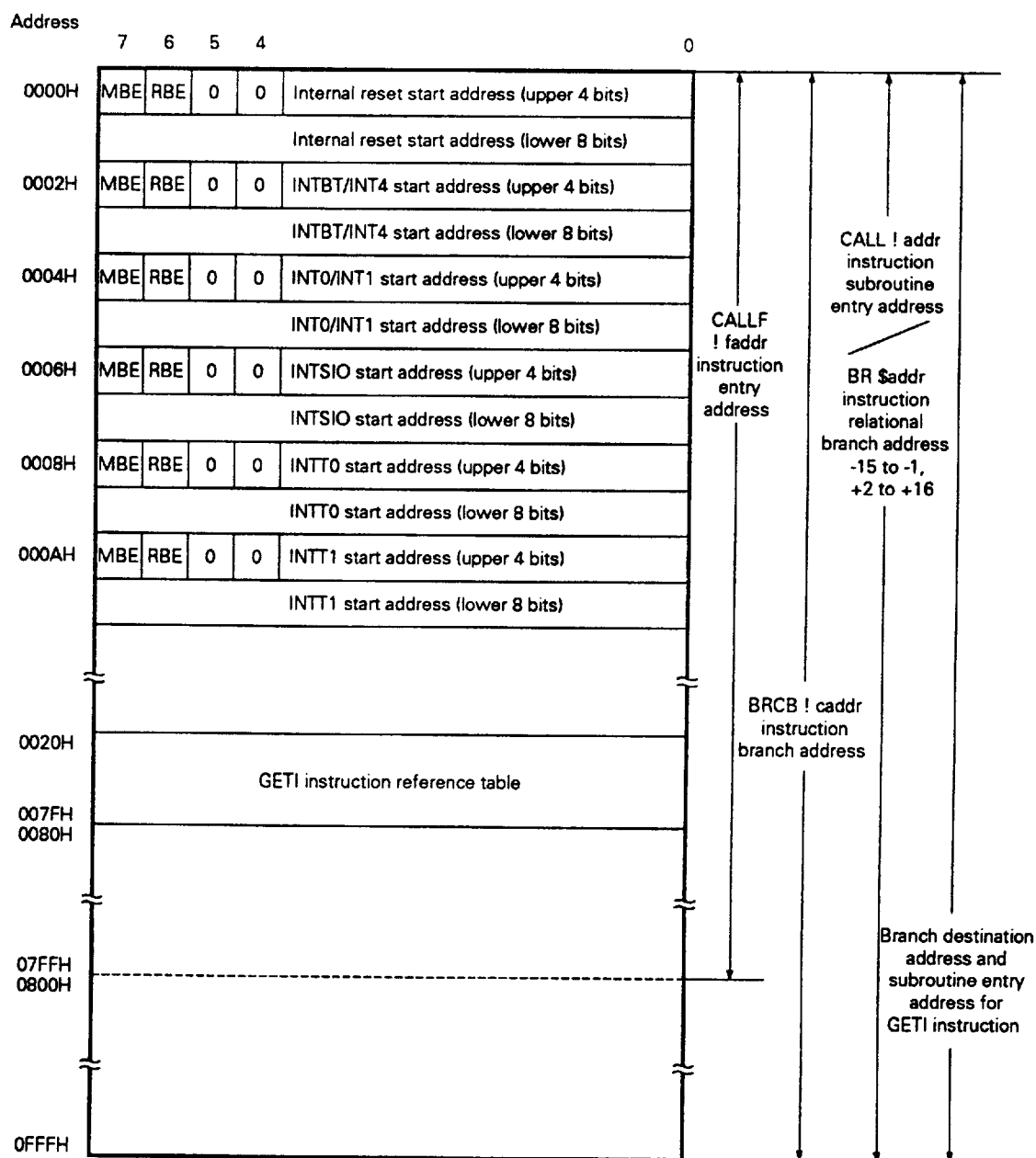


Fig. 4-1 Program Memory Map (2/2)

Remarks: In addition to the above addresses, program can be branched to addresses specified by the PC with the contents of its lower 8 bits changed by BR PCDE or BR PCXA instruction.

(a) μ PD75108A

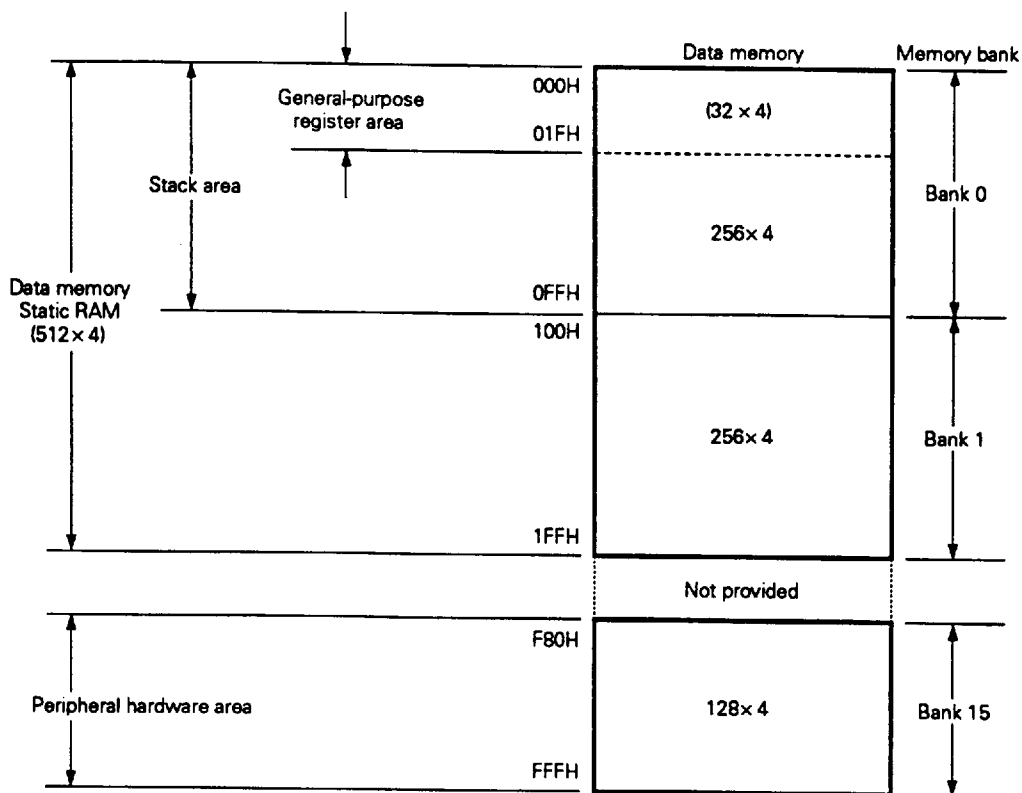


Fig. 4-2 Data Memory Map(1/2)

(b) μPD75104A

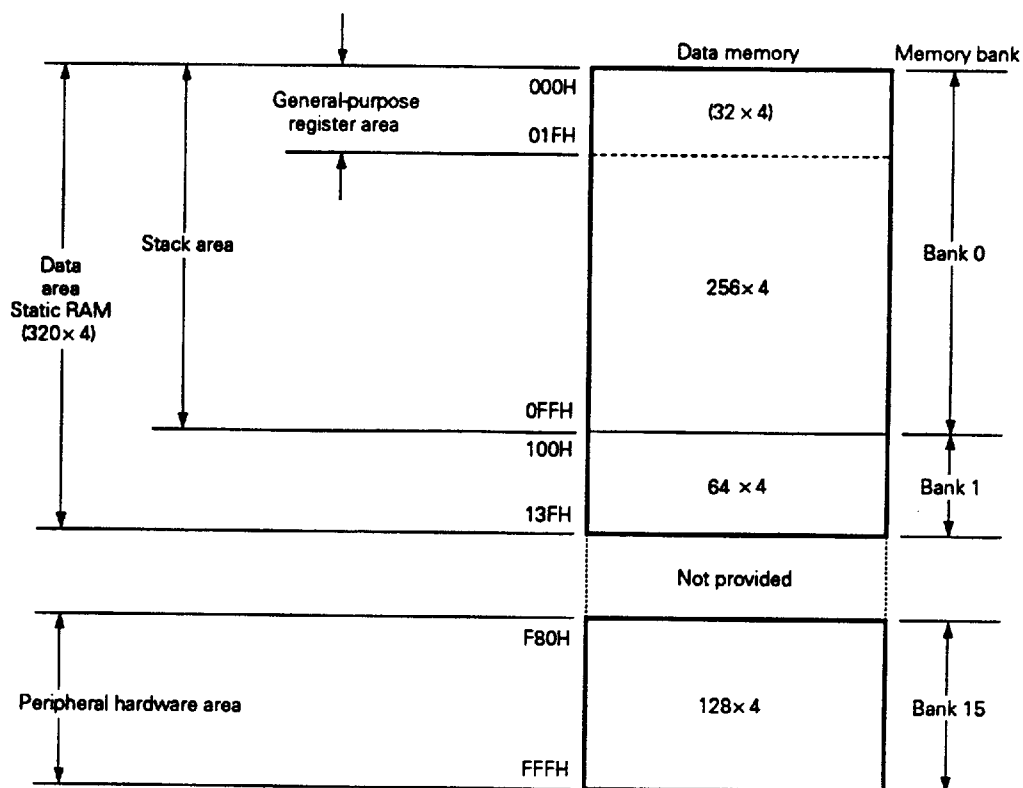


Fig. 4-2 Data Memory Map(2/2)

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

I/O ports are classified into the following 3 kinds:

- CMOS input (PORT0, 1) : 8
- CMOS input/output (PORT2, 3, 4, 5, 6, 7, 8, 9) : 32
- N-ch open-drain input/output (PORT12, 13, 14) : 12

Total : 52

Table 5-1 Port Function

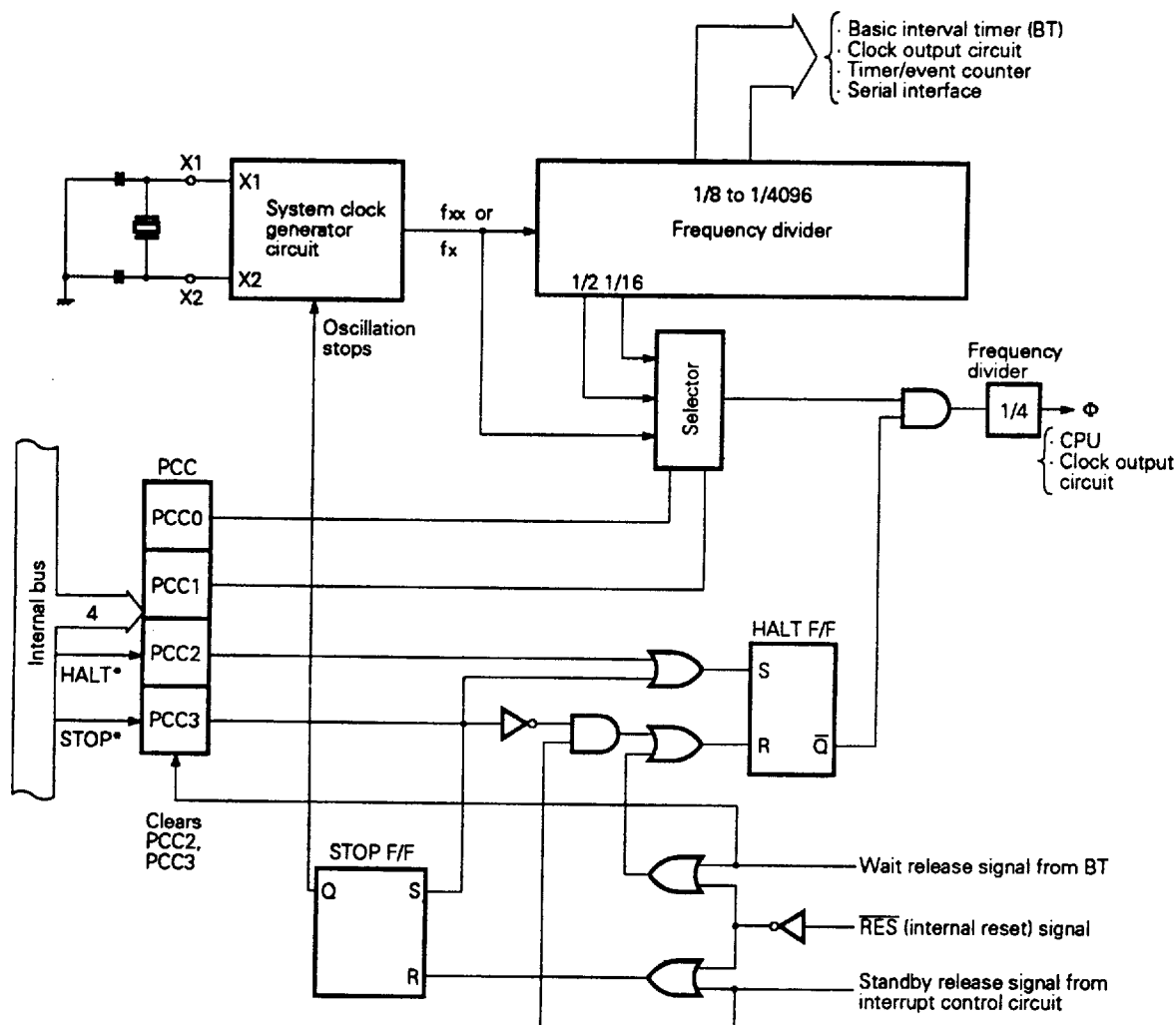
Port (Symbol)	Function	Operation and Features	Remarks
PORT0	4-bit input	Can always be read or tested regardless of operation mode of shared pin	Shared with SI, SO, SCK, and INT4 pins
PORT1			Shared with INT0 to 3 pins each bit can be connected to pull-up resistor by mask option.
PORT3 PORT6	4-bit I/O*	Can be set in input or output mode bitwise	Each bit of Port 6 pins can be connected to pull-up resistor by mask option
PORT2		Can be set in input or output mode in 4-bit units. Ports 4 and 5, 6 and 7, 8 and 9 can be used in pairs to input or output 8-bit data	Shared with PTO0, PTO1, and PCL pins.
PORT4			Each bit can be connected to pull-up resistor by mask option
PORT5			
PORT7			
PORT8 PORT9			
PORT12 PORT13 PORT14	4-bit I/O* (N-ch open-drain, 12V)	Can be set in input or output mode in 4-bit units. Ports 12 and 13 can be used in pairs to input or output 8-bit data	Each bit can be connected to pull-up resistor by mask option

*: Can directly drive LED.

5.2 CLOCK GENERATOR CIRCUIT

The clock generator circuit generates clocks to control CPU operation modes by supplying clocks to the CPU and peripheral hardware. In addition, this circuit can change the instruction execution time.

- 0.95 μs/1.91 μs/15.3 μs (operating at 4.19 MHz)



Remarks 1: fxx= Crystal/ceramic oscillator

2: fx = External clock frequency

3: * indicates the instruction execution

4: PCC: Processor clock control register

5: One clock cycle (tcv) of Φ is one machine cycle of an instruction. For tcv, refer to AC characteristics in 12. ELECTRICAL SPECIFICATIONS.

Fig. 5-1 Clock Generator Block Diagram

5.3 CLOCK OUTPUT CIRCUIT

The clock output circuit outputs clock pulse from the P22/PCL pin. This clock output circuit is used to output clock pulses to the remote control output, peripheral LSIs, etc.

- Clock output (PCL) : Φ , 524 kHz, 262 kHz (operating at 4.19 MHz)

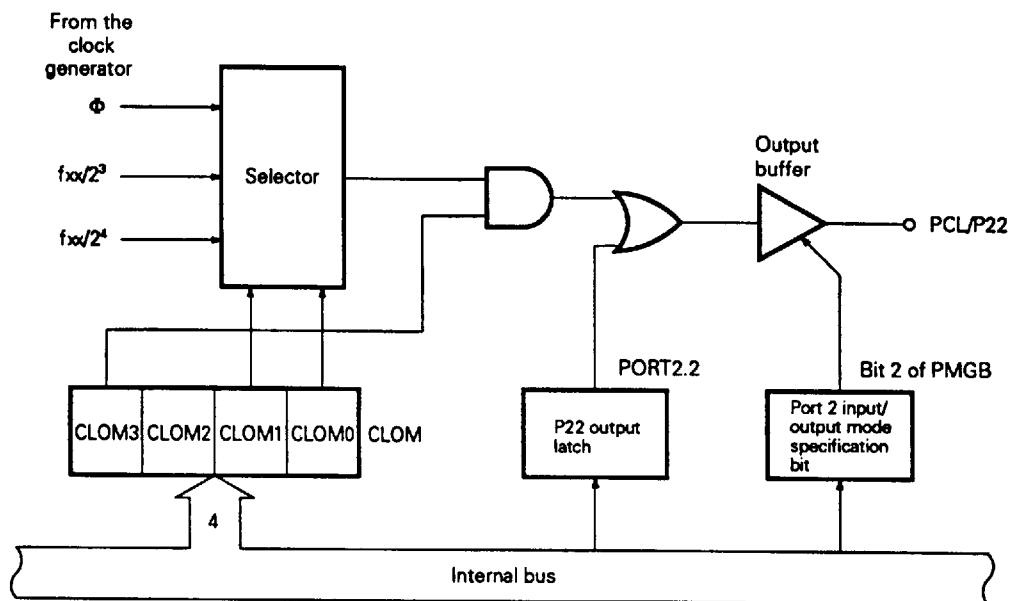
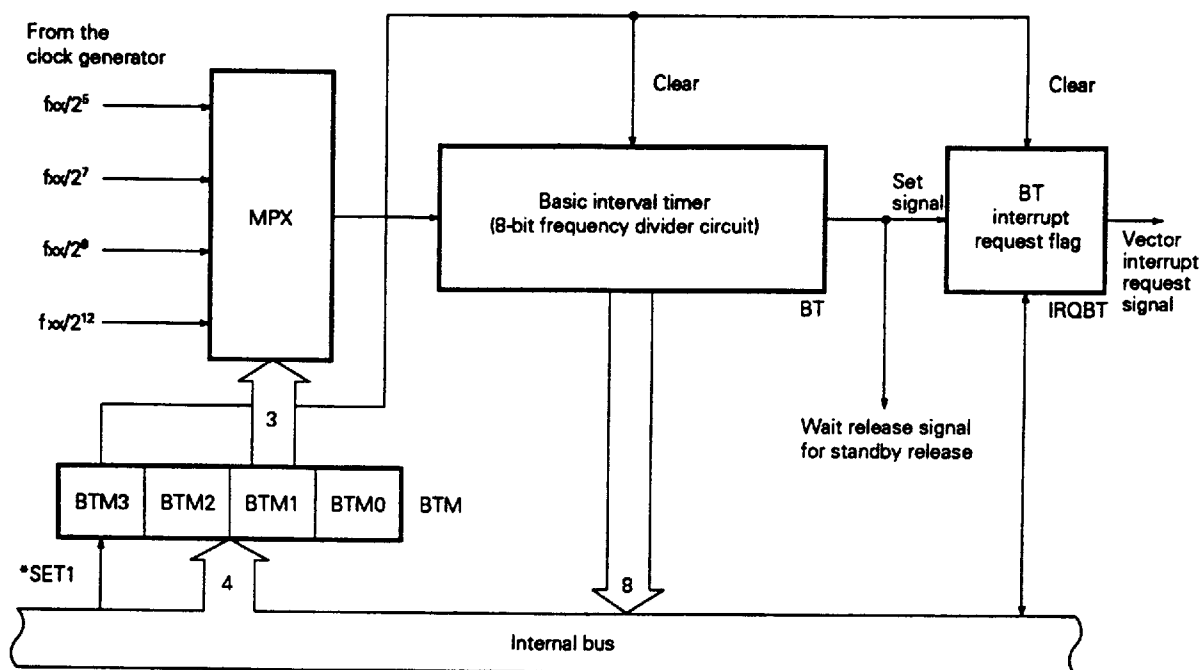


Fig. 5-2 Clock Output Circuit Configuration

5.4 BASIC INTERVAL TIMER

The basic interval timer has these functions:

- Interval timer operation which generates a reference time interrupt
- Watchdog timer application which detects a program runaway
- Selects the wait time for releasing the standby mode and counts the wait time
- Reads out the count value



Remarks: *: Instruction execution

Fig. 5-3 Basic Interval Timer Configuration

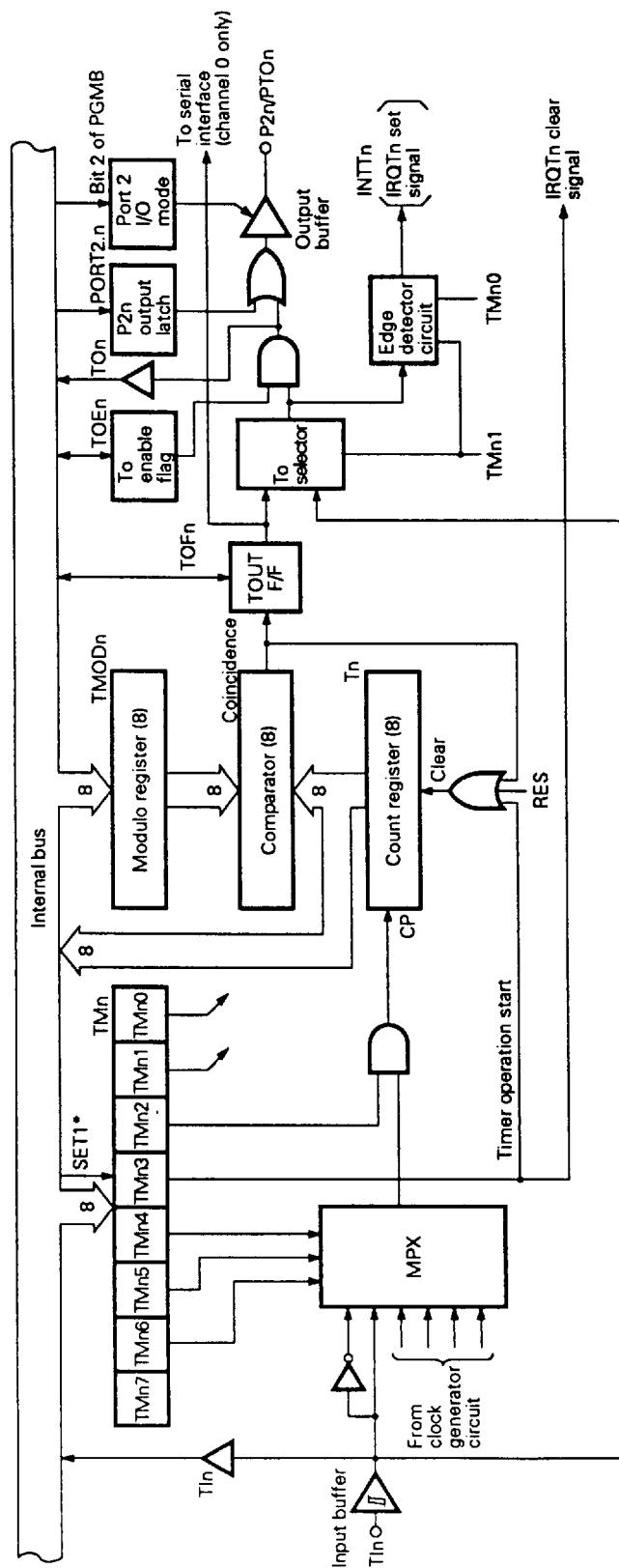
5.5 TIMER/EVENT COUNTER

μPD75108A contains two channels of timer/event counters.

These two channels are almost identical in terms of configuration and function except the count pulse (CP) that can be selected and the function to supply clocks to the serial interface.

The functions of the timer/event counter include:

- Programmable interval timer operation
- Output of square wave at an arbitrary frequency to PTO_n pin
- Event counter operation
- Input of TIn pin signal as external interrupt input signal
- Dividing TIn pin input by N to output to PTO_n pin (frequency divider operation)
- Supply of serial shift clock to serial interface circuit (channel 0 only)
- Reading counting status



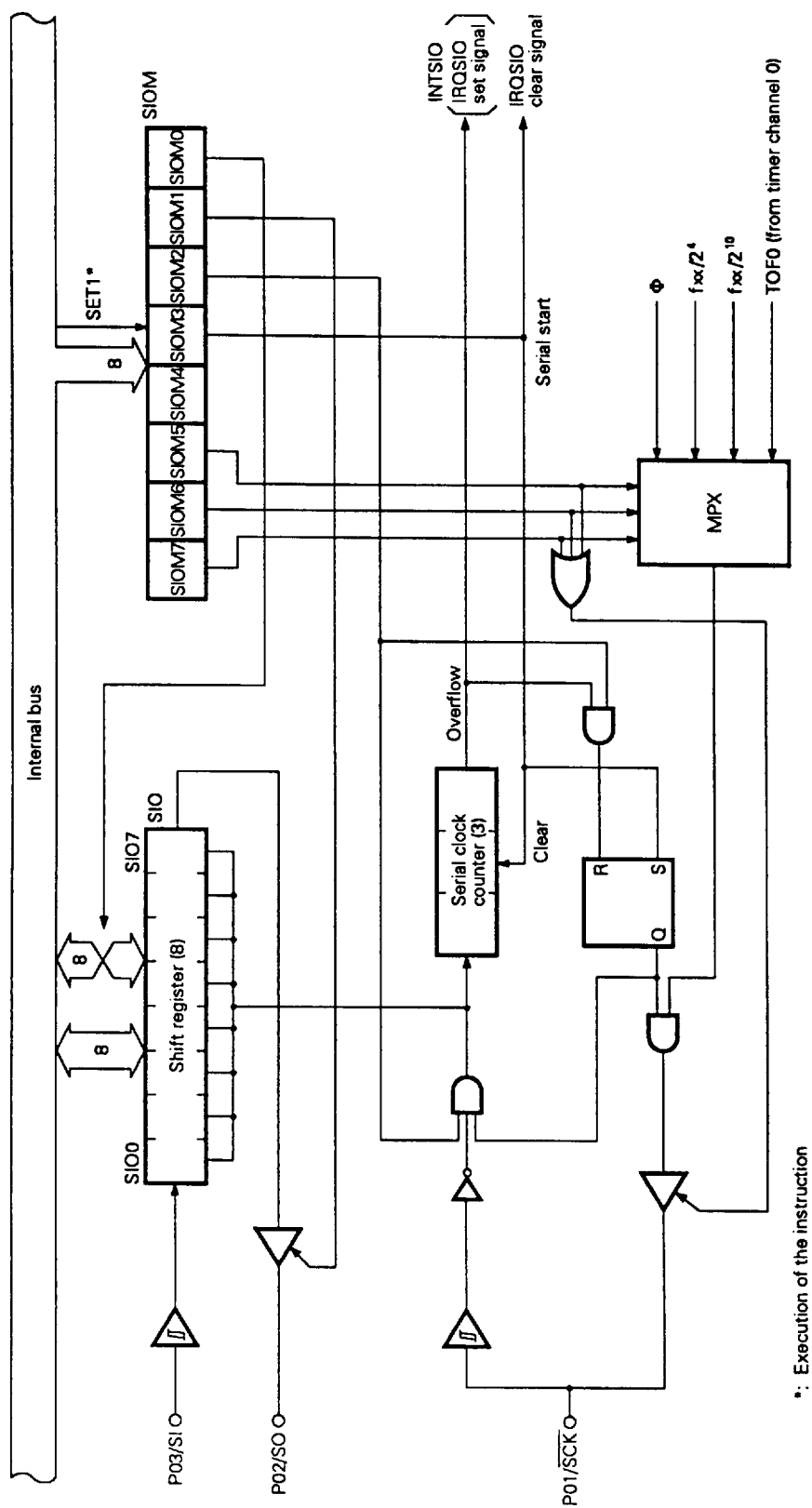
*: SET1: Execution of the instruction

Fig. 5-4 Timer/Event Counter Block Diagram (n = 0, 1)

5.6 SERIAL INTERFACE

The μ PD75108A is equipped with clock 8-bit serial interface that operates in the following two modes:

- Operation stop mode
- Three-line serial I/O mode



5.7 PROGRAMMABLE THRESHOLD PORT (ANALOG INPUT PORT)

μ PD75108A is equipped with a 4-bit analog input port (consisting of PTH00 to PTH03 pins) whose threshold voltage is programmable. This programmable threshold port is configured as shown in Figure 5-6.

The threshold voltage (V_{REF}) can be changed in 16 steps ($V_{DD} \times 0.5/16 - V_{DD} \times 15.5/16$), and analog signals can be directly input.

When V_{REF} is set to $V_{DD} \times 7.5/16$, the programmable threshold port can also be used as a digital signal input port.

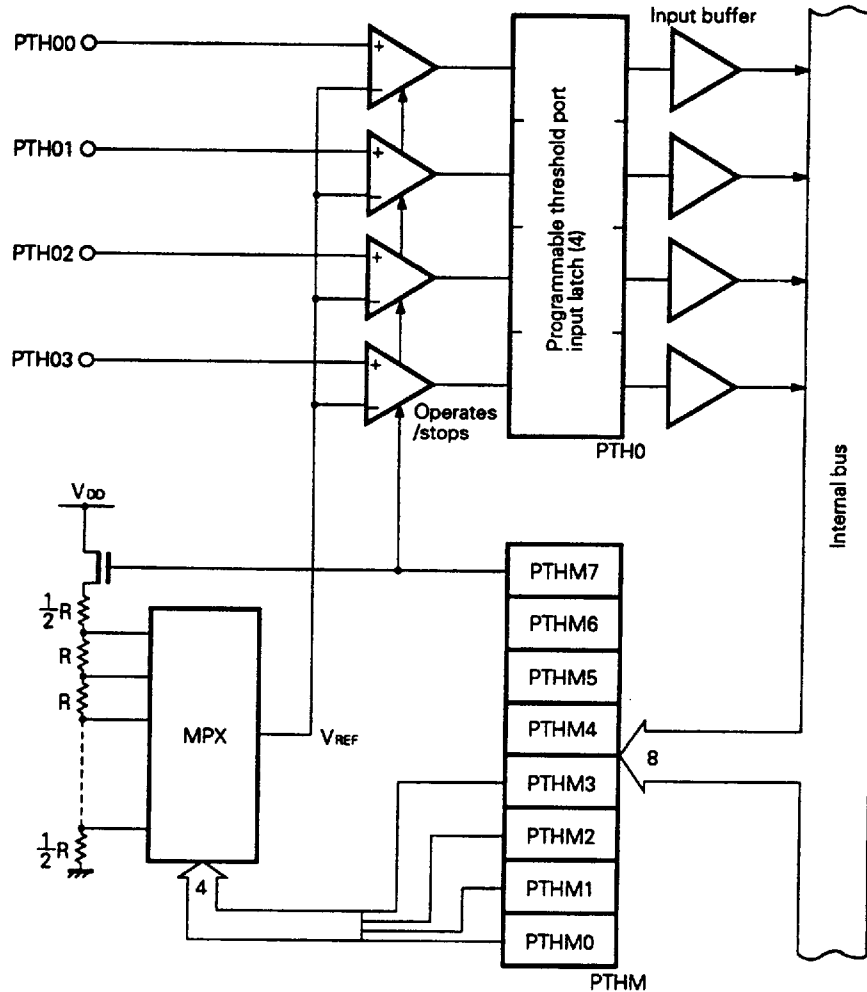
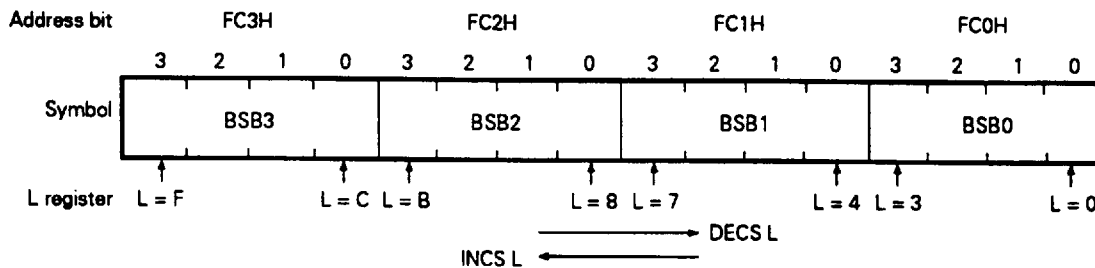


Fig. 5-6 Programmable Threshold Port Configuration

5.8 BIT SEQUENTIAL BUFFER 16 BITS

The bit sequential buffer is a data memory specifically provided for bit manipulation. With this buffer, addresses and bit specifications can be sequentially up-dated in bit manipulation operation. Therefore, this buffer is very useful for processing long data in bit units.



Remarks: For the pmem.@L addressing, the specification bit is shifted according to the L register.

Fig. 5-7 Bit Sequential Buffer Format

5.9 POWER-ON FLAG (MASK OPTION)

The power-ON flag (PONF) is set to only when the power-ON reset circuit operates and power-ON reset signal has been generated (see Fig. 8-1).

The PONF flag is mapped at bit 0 of memory space address FD1H, and can be manipulated by a bit manipulation instruction. However, it cannot be set by the SET1 instruction.

6. INTERRUPT FUNCTIONS

The μPD75108A has 7 different interrupt sources and can perform multiplexed interrupt processing with priority assigned. In addition to that, the μPD75108A is also provided with two types of edge detection testable inputs.

The interrupt control circuit of the μPD75108A has these functions:

- Hardware controlled vector interrupt function which can control whether or not to accept an interrupt by using the interrupt enable flag (IExxx) and interrupt master enable flag (IME).
- The interrupt start address can be arbitrarily set.
- Multiplexed interrupt function that can specify priority by the interrupt priority selector register (IPS).
- Interrupt request flag (IRQxxx) test function (an interrupt generation can be confirmed by means of software).
- Standby mode release (Interrupts to be released can be selected by the interrupt enable flag).

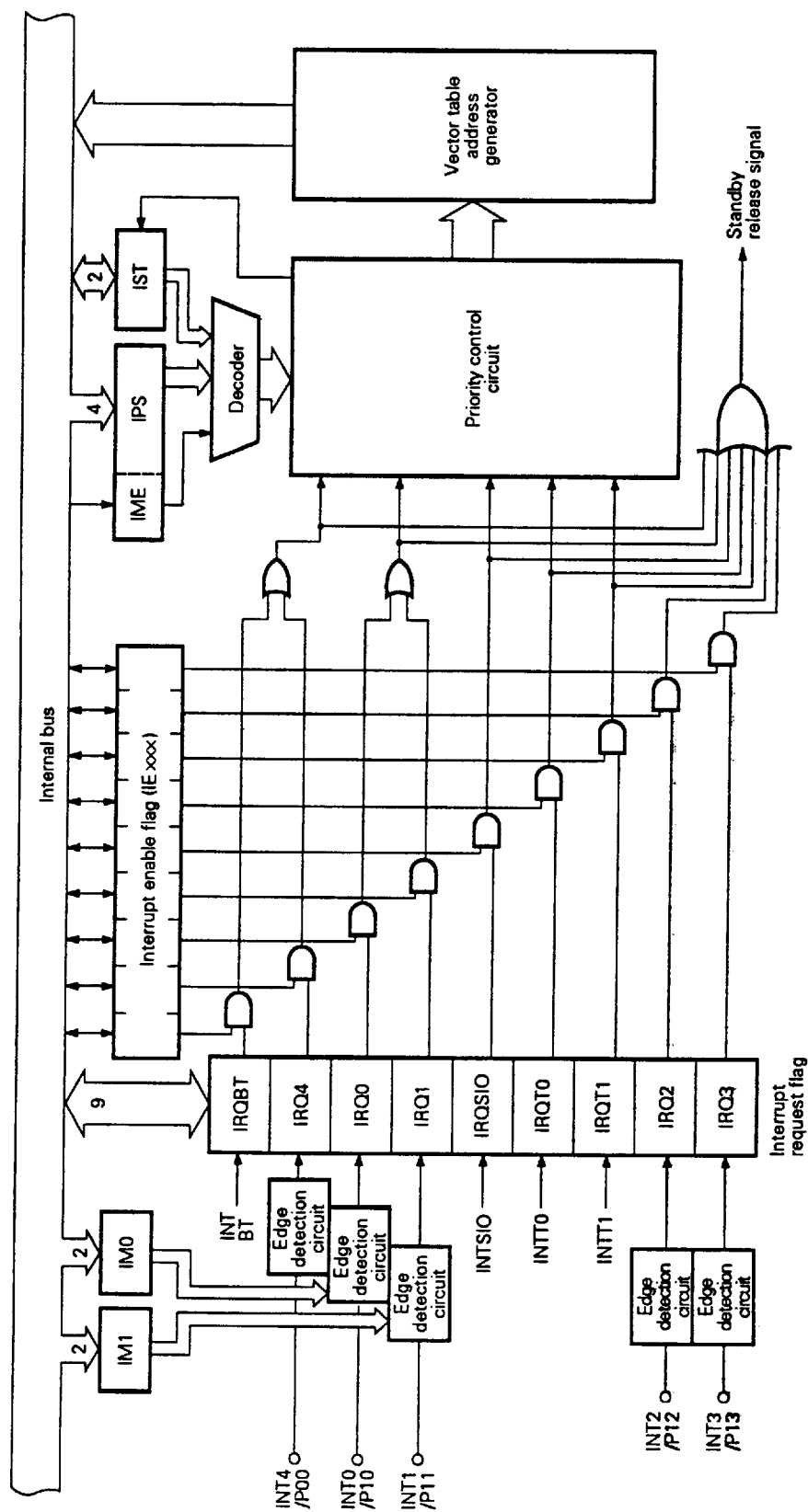


Fig. 6-1 Interrupt Control Block Diagram

7. STANDBY FUNCTIONS

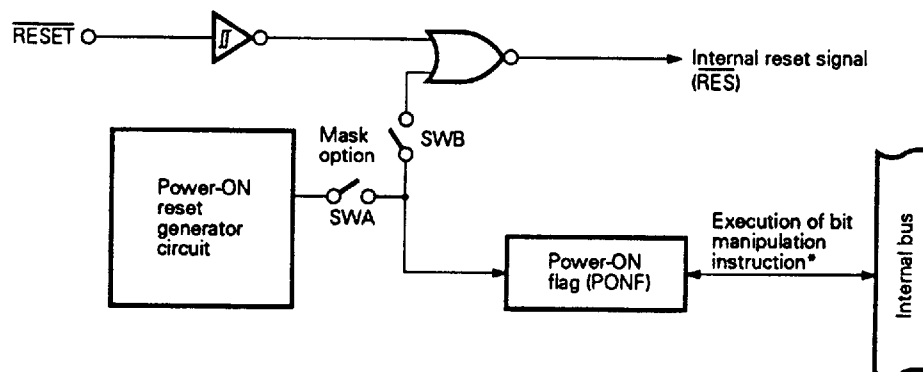
The μPD75108A has two different standby modes (STOP mode and HALT mode) to reduce the power consumption of the microcomputer chip while waiting for program execution.

Table 7-1 Each Status in Standby Mode

		STOP Mode	HALT Mode
Setting Instruction		STOP instruction	HALT instruction
Operation Status	Clock Oscillator circuit	Clock oscillation stops	Only CPU clock Φ is stopped
	Basic Interval Timer	Stops	Operates (sets IRQBT at reference time intervals)
	Serial Interface	Operates only when input of external $\overline{SCK}$ or output of T00 is selected as serial clock (where external T10 is input to timer/event counter 0)	Operates when serial clock other than Φ is specified
	Timer/Event Counter	Operates only when TIn pin input signal is specified as count clock	Operates ,
	Clock output circuit	Stops	Outputs when clock other than CPU clock Φ is used
	CPU	Stops	Stops
Release Signal		Interrupt request signal enabled by interrupt enable flag, or $\overline{RESET}$ input	

8. RESET FUNCTION

The reset ($\overline{\text{RES}}$) signal generator circuit is configured as shown in Figure 8-1.

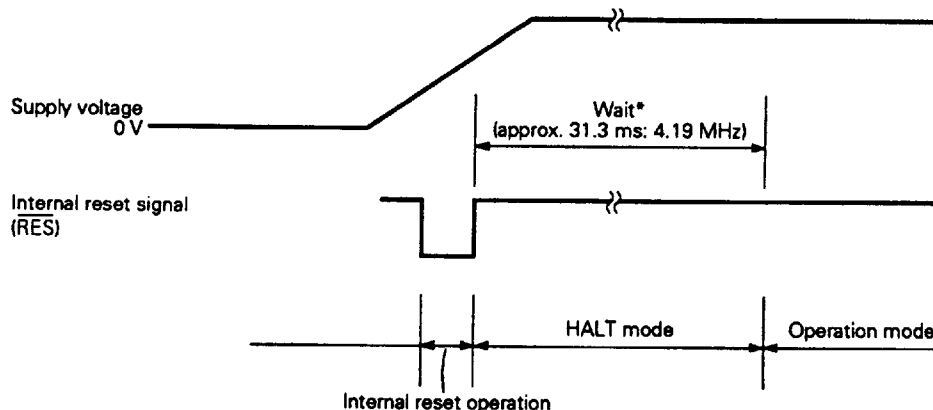


*: PONF cannot be set to 1 by SET1 instruction.

Fig. 8-1 Reset Signal Generator Circuit

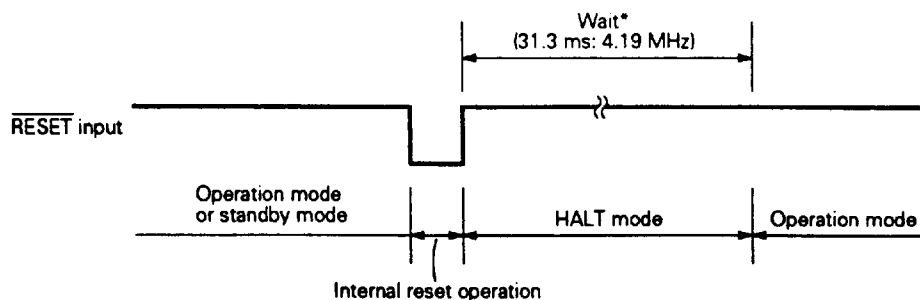
The Power-ON reset generator circuit generates an internal reset signal when the supply voltage rises. This pulse can be used in three ways by specifying a mask option through SWA and SWB shown in Fig. 8-1. (Refer to 11. MASK OPTION SELECTION.)

The reset operations performed by the Power-On reset circuit and the RESET input signal are illustrated in Figs. 8-2 and 8-3, respectively.



*: The wait time does not include the time required after the $\overline{\text{RES}}$ signal has been generated until the oscillation starts.

Fig. 8-2 Reset by Power-ON Reset Circuit



*: The wait time does not include the time required after the $\overline{\text{RES}}$ signal has been generated until the oscillation starts.

Fig. 8-3 Reset by $\overline{\text{RESET}}$ Signal

The status of each internal hardware device after the reset operation has been performed is shown in Table 8-1.

Table 8-1 Hardware Device Status After Reset (1/2)

Hardware		$\overline{\text{RESET}}$ input during standby mode	Power-ON Reset or $\overline{\text{RESET}}$ Input during Operation
Program Counter (PC)		Lower 5 bits of program memory address 0000H are set to PC ₁₂₋₈ ,*1 and contents of address 0001H are set to PC ₇₋₀ .	Lower 5 bits of program memory address 0000H are set to PC ₁₂₋₈ ,*1 and contents of address 0001H are set to PC ₇₋₀ .
PSW	Carry Flag (CY)	Retained	Undefined
	Skip Flags (SK0-SK2)	0	0
	Interrupt Status Flags (IST0, IST1)	0	0
	Bank Enable Flags (MBE, RBE)	Bit 6 of program memory address 0000H is set in RBE, and bit 7 is set in MBE.	Bit 6 of program memory address 0000H is set in RBE, and bit 7 is set in MBE.
Stack Pointer (SP)		Undefined	Undefined
Data Memory (RAM)		Retained*2	Undefined
General-Purpose Registers (X,A,H,L,D,E,B,C)		Retained	Undefined
Bank Selector Registers (MBS, RBS)		0, 0	0, 0
Basic interval timer	Counter (BT)	Undefined	Undefined
	Mode Register (BTM)	0	0
Timer/Event Counter (n = 0, 1)	Counter (Tn)	0	0
	Modulo Register (TMODn)	FFH	FFH
	Mode Register (TMn)	0	0
	TOEn, TOFn	0, 0	0, 0
Serial Interface	Shift Register (SIO)	Retained	Undefined
	Mode Register (SIOM)	0	0

*1: PC₁₁₋₈ for μPD75104A

2: Data at data memory addresses 0F8H to 0FDH become undefined when the $\overline{\text{RESET}}$ signal has been input.

Table 8-1 Hardware Device Status After Reset (2/2)

Hardware		RESET input during standby mode	Power-ON Reset or RESET Input during Operation
Clock Generator Circuit, Clock Output Circuit	Processor Clock Control Register (PCC)	0	0
	Clock Output Mode Register (CLOM)	0	0
Interrupt	Interrupt Request Flags (IRQ _{xxx})	Reset (0)	Reset (0)
	Interrupt Enable Flags (IE _{xxx})	0	0
	Priority Selector Register (IPS)	0	0
	INT0, 1 Mode Registers (IM0, IM1)	0, 0	0, 0
Digital Port	Output Buffer	Off	Off
	Output Latch	Cleared (0)	Cleared (0)
	I/O Mode Registers (PMGA, PMGB, PMGC)	0	0
Analog Port	PTH00-PTH03 Input Latches	Undefined	Undefined
	Mode Register (PTHM)	0	0
Power-ON Flag (PONF)		Retained	1 or undefined*
Bit Sequential Buffer (BSB0-BSB3)		0	0

*: Power-ON reset: 1

RESET input during operation: undefined

9. INSTRUCTION SET

(1) Operand representation and description

Describe one or more operands in the operand field of each instruction according to the operand representation and description methods of the instruction (for details, refer to RA75X Assembler Package User's Manual - Language (EEU-730)). With some instructions, only one operand should be selected from several operands. The uppercase characters, +, and - are keywords and must be described as is.

Describe an appropriate numeric value or label as immediate data.

The symbols in the register and flag symbols can be described as labels in the places of mem, fmem, pmem, and bit (for details, refer to μPD751XX Series User's Manual (IEM-922)). However, fmem and pmem restricts the label that can be described.

Representation	Description
reg	X, A, B, C, D, E, H, L
reg1	X, B, C, D, E, H, L
rp	XA, BC, DE, HL
rp1	BC, DE, HL
rp2	BC, DE
rp'	XA, BC, DE, HL, XA', BC', DE', HL'
rp'1	BC, DE, HL, XA', BC', DE', HL'
rpa	HL, HL+, HL-, DE, DL
rpa1	DE, DL
n4	4-bit immediate data or label
n8	8-bit immediate data or label
mem	8-bit immediate data or label*
bit	2-bit immediate data or label
fmem	FB0H to FBFH, FF0H to FFFH immediate data or label
pmem	FC0H to FFFH immediate data or label
addr	μPD75104A 0000H to 0FFFH immediate data or label
	μPD75108A 0000H to 1F7FH immediate data or label
caddr	12-bit immediate data or label
faddr	11-bit immediate data or label
taddr	20H to 7FH immediate data (where bit0 = 0) or label
PORTn	PORT0 - PORT9, PORT12 - PORT14
IExxx	IEBT, IESIO, IET0, IET1, IE0 - IE4
RBn	RB0 - RB3
MBn	MB0, MB1, MB15

*: Only even address can be described as mem for 8-bit data processing.

(2) Legend of operation field

A	: A register; 4-bit accumulator
B	: B register; 4-bit accumulator
C	: C register; 4-bit accumulator
D	: D register; 4-bit accumulator
E	: E register; 4-bit accumulator
H	: H register; 4-bit accumulator
L	: L register; 4-bit accumulator
X	: X register; 4-bit accumulator
XA	: Register pair (XA); 8-bit accumulator
BC	: Register pair (BC); 8-bit accumulator
DE	: Register pair (DE); 8-bit accumulator
HL	: Register pair (HL); 8-bit accumulator
XA'	: Expansion register pair (XA')
BC'	: Expansion register pair (BC')
DE'	: Expansion register pair (DE')
HL'	: Expansion register pair (HL')
PC	: Program counter
SP	: Stack pointer
CY	: Carry flag; or bit accumulator
PSW	: Program status word
MBE	: Memory bank enable flag
RBE	: Register bank enable flag
PORT _n	: Port n (n = 0 - 9, 12 - 14)
IME	: Interrupt mask enable flag
IPS	: Interrupt priority selection register
IE _{xxx}	: Interrupt enable flag
RBS	: Register bank selection register
MBS	: Memory bank selection register
PCC	: Processor clock control register
.	: Delimiter of address and bit
(xx)	: Contents addressed by xx
xxH	: Hexadecimal data

(3) Symbols in addressing area field

*1	MB = MBE · MBS (MBS = 0, 1, 15)		Data memory addressing
*2	MB = 0		
*3	MBE = 0 : MB = 0 (00H-7FH) MB = 15 (80H-FFH) MBE = 1 : MB = MBS (MBS = 0, 1, 15)		
*4	MB = 15, fmem = FB0H-FBFH, FF0H-FFFH		
*5	MB = 15, pmem = FC0H-FFFH		
*6	μPD75104A	addr = 0000H-0FFFH	Program memory addressing
	μPD75108A	addr = 0000H-1F7FH	
*7	addr = (Current PC) - 15 to (Current PC) - 1 (Current PC) + 2 to (Current PC) + 16		
*8	μPD75104A	caddr = 0000H-0FFFH (PC ₁₁ = 0)	
	μPD75108A	caddr = 0000H-0FFFH (PC ₁₂ = 0) or 1000H-1F7FH (PC ₁₂ = 1)	
*9	faddr = 0000H-07FFH		
*10	taddr = 0020H-007FH		

- Remarks**
- MB indicates memory bank that can be accessed.
 - In *2, MB = 0 regardless of MBE and MBS.
 - In *4 and *5, MB = 15 regardless of MBE and MBS.
 - *6 to *10 indicate areas that can be addressed.

(4) Machine cycle field

In this field, S indicates the number of machine cycles required when an instruction having a skip function skips. The value of S varies as follows:

- When no instruction is skipped S = 0
- When 1-byte or 2-byte instruction is skipped S = 1
- When 3-byte instruction (BR ! adder or CALL ! adder) is skipped S = 2

Note: The GETI instruction is skipped in one machine cycle.

One machine cycle equals to one cycle of the CPU clock Φ, (= t_{cy}), and can be changed in three steps depending on the setting of the processor clock control register (PCC).

Instructions	Mne- monics	Operand	Bytes	Ma- chine Cyc- les	Operation	Addressing Area	Skip Conditions
Transfer	MOV	A, #n4	1	1	$A \leftarrow n4$		String effect A
		reg1, #n4	2	2	$reg1 \leftarrow n4$		
		XA, #n8	2	2	$XA \leftarrow n8$		String effect A
		HL, #n8	2	2	$HL \leftarrow n8$		String effect B
		rp2, #n8	2	2	$rp2 \leftarrow n8$		
		A, @HL	1	1	$A \leftarrow (HL)$	*1	
		A, @HL+	1	2+S	$A \leftarrow (HL)$, then $L \leftarrow L+1$	*1	L = 0
		A, @HL-	1	2+S	$A \leftarrow (HL)$, then $L \leftarrow L-1$	*1	L = FH
		A, @rpa1	1	1	$A \leftarrow (rpa1)$	*2	
		XA, @HL	2	2	$XA \leftarrow (HL)$	*1	
		@HL, A	1	1	$(HL) \leftarrow A$	*1	
		@HL, XA	2	2	$(HL) \leftarrow XA$	*1	
		A, mem	2	2	$A \leftarrow (mem)$	*3	
		XA, mem	2	2	$XA \leftarrow (mem)$	*3	
		mem, A	2	2	$(mem) \leftarrow A$	*3	
		mem, XA	2	2	$(mem) \leftarrow XA$	*3	
		A, reg	2	2	$A \leftarrow reg$		
		XA, rp'	2	2	$XA \leftarrow rp'$		
		reg1, A	2	2	$reg1 \leftarrow A$		
		rp'1, XA	2	2	$rp'1 \leftarrow XA$		
	XCH	A, @HL	1	1	$A \leftrightarrow (HL)$	*1	
		A, @HL+	1	2+S	$A \leftrightarrow (HL)$, then $L \leftarrow L+1$	*1	L = 0
		A, @HL-	1	2+S	$A \leftrightarrow (HL)$, then $L \leftarrow L-1$	*1	L = FH
		A, @rpa1	1	1	$A \leftrightarrow (rpa1)$	*2	
		XA, @HL	2	2	$XA \leftrightarrow (HL)$	*1	
		A, mem	2	2	$A \leftrightarrow (mem)$	*3	
		XA, mem	2	2	$XA \leftrightarrow (mem)$	*3	
		A, reg1	1	1	$A \leftrightarrow reg1$		
		XA, rp'	2	2	$XA \leftrightarrow rp'$		
Table Refer- ence	MOVT	XA, @PCDE	1	3	• μPD75104A $XA \leftarrow (PC_{11-8}+DE)_{ROM}$		
					• μPD75108A $XA \leftarrow (PC_{12-8}+DE)_{ROM}$		
		XA, @PCXA	1	3	• μPD75104A $XA \leftarrow (PC_{11-8}+XA)_{ROM}$		
					• μPD75108A $XA \leftarrow (PC_{12-8}+XA)_{ROM}$		

Instructions	Mne- monics	Operand	Bytes	Ma- chine Cyc- les	Operation	Addressing Area	Skip Conditions
Bit transfer	MOV1	CY, fmem.bit	2	2	$CY \leftarrow (fmem.bit)$	*4	
		CY, pmem.@L	2	2	$CY \leftarrow (pmem_{7:2}+L_{3:2}.bit(L_{1:0}))$	*5	
		CY, @H+mem. bit	2	2	$CY \leftarrow (H+mem_{3:0}.bit)$	*1	
		fmem.bit, CY	2	2	$(fmem.bit) \leftarrow CY$	*4	
		pmem.@L, CY	2	2	$(pmem_{7:2}+L_{3:2}.bit(L_{1:0})) \leftarrow CY$	*5	
		@H+mem.bit, CY	2	2	$(H+mem_{3:0}.bit) \leftarrow CY$	*1	
Arith- metic opera- tion	ADDS	A, #n4	1	1+S	$A \leftarrow A+n4$		carry
		XA, #n8	2	2+S	$XA \leftarrow XA+n8$		carry
		A, @HL	1	1+S	$A \leftarrow A+(HL)$	*1	carry
		XA, rp'	2	2+S	$XA \leftarrow XA+rp'$		carry
		rp'1, XA	2	2+S	$rp'1 \leftarrow rp'1+XA$		carry
	ADDC	A, @HL	1	1	$A, CY \leftarrow A+(HL)+CY$	*1	
		XA, rp'	2	2	$XA, CY \leftarrow XA+rp'+CY$		
		rp'1, XA	2	2	$rp'1, CY \leftarrow rp'1+XA+CY$		
	SUBS	A, @HL	1	1+S	$A \leftarrow A-(HL)$	*1	borrow
		XA, rp'	2	2+S	$XA \leftarrow XA-rp'$		borrow
		rp'1, XA	2	2+S	$rp'1 \leftarrow rp'1-XA$		borrow
	SUBC	A, @HL	1	1	$A, CY \leftarrow A-(HL)-CY$	*1	
		XA, rp'	2	2	$XA, CY \leftarrow XA-rp'-CY$		
		rp'1, XA	2	2	$rp'1, CY \leftarrow rp'1-XA-CY$		
	AND	A, #n4	2	2	$A \leftarrow A \wedge n4$		
		A, @HL	1	1	$A \leftarrow A \wedge (HL)$	*1	
		XA, rp'	2	2	$XA \leftarrow XA \wedge rp'$		
		rp'1, XA	2	2	$rp'1 \leftarrow rp'1 \wedge XA$		
	OR	A, #n4	2	2	$A \leftarrow A \vee n4$		
		A, @HL	1	1	$A \leftarrow A \vee (HL)$	*1	
		XA, rp'	2	2	$XA \leftarrow XA \vee rp'$		
		rp'1, XA	2	2	$rp'1 \leftarrow rp'1 \vee XA$		
	XOR	A, #n4	2	2	$A \leftarrow A \nabla n4$		
		A, @HL	1	1	$A \leftarrow A \nabla (HL)$	*1	
		XA, rp'	2	2	$XA \leftarrow XA \nabla rp'$		
		rp'1, XA	2	2	$rp'1 \leftarrow rp'1 \nabla XA$		
Accumulator Manipulation	RORC	A	1	1	$CY \leftarrow A_0, A_3 \leftarrow CY, A_{n-1} \leftarrow A_n$		
	NOT	A	2	2	$A \leftarrow \bar{A}$		
Incre- ment/ decre- ment	INCS	reg	1	1+S	$reg \leftarrow reg+1$		reg = 0
		rp1	1	1+S	$rp1 \leftarrow rp1+1$		rp1 = 00H
		@HL	2	2+S	$(HL) \leftarrow (HL)+1$	*1	(HL) = 0
		mem	2	2+S	$(mem) \leftarrow (mem)+1$	*3	(mem) = 0
	DECS	reg	1	1+S	$reg \leftarrow reg-1$		reg = FH
		rp'	2	2+S	$rp' \leftarrow rp'-1$		rp' = FFH

Instructions	Mne- monics	Operand	Bytes	Ma- chine Cyc- les	Operation	Addressing Area	Skip Conditions
Com- pare	SKE	reg, #n4	2	2+S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2+S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1+S	Skip if A = (HL)	*1	A = (HL)
		XA, @HL	2	2+S	Skip if XA = (HL)	*1	XA = (HL)
		A, reg	2	2+S	Skip if A = reg		A = reg
		XA, rp'	2	2+S	Skip if XA = rp'		XA = rp'
Carry flag Manipu- lation	SET1	CY	1	1	$CY \leftarrow 1$		
	CLR1	CY	1	1	$CY \leftarrow 0$		
	SKT	CY	1	1+S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	$CY \leftarrow \overline{CY}$		
Memory/ Bit Manipu- lation	SET1	mem.bit	2	2	(mem.bit) $\leftarrow 1$	*3	
		fmem.bit	2	2	(fmem.bit) $\leftarrow 1$	*4	
		pmem.@L	2	2	(pmem7:2 + L3:2.bit(L1:0)) $\leftarrow 1$	*5	
		@H+mem.bit	2	2	(H + mem3:0.bit) $\leftarrow 1$	*1	
	CLR1	mem.bit	2	2	(mem.bit) $\leftarrow 0$	*3	
		fmem.bit	2	2	(fmem.bit) $\leftarrow 0$	*4	
		pmem.@L	2	2	(pmem7:2 + L3:2.bit(L1:0)) $\leftarrow 0$	*5	
		@H+mem.bit	2	2	(H+mem3:0.bit) $\leftarrow 0$	*1	
	SKT	mem.bit	2	2+S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2+S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2+S	Skip if (pmem7:2+L3:2.bit(L1:0)) = 1	*5	(pmem.@L) = 1
		@H+mem.bit	2	2+S	Skip if (H + mem3:0.bit) = 1	*1	(@H+mem.bit) = 1
	SKF	mem.bit	2	2+S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2+S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2+S	Skip if (pmem7:2+L3:2.bit(L1:0)) = 0	*5	(pmem.@L) = 0
		@H+mem.bit	2	2+S	Skip if (H + mem3:0.bit) = 0	*1	(@H+mem.bit) = 0
	SKTCLR	fmem.bit	2	2+S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2+S	Skip if (pmem7:2+L3:2.bit(L1:0)) = 1 and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2+S	Skip if (H+mem3:0.bit) = 1 and clear	*1	(@H+mem.bit) = 1
	AND1	CY, fmem.bit	2	2	$CY \leftarrow CY \wedge (fmem.bit)$	*4	
		CY, pmem.@L	2	2	$CY \leftarrow CY \wedge (pmem7:2+L3:2.bit(L1:0))$	*5	
		CY, @H+mem.bit	2	2	$CY \leftarrow CY \wedge (H+mem3:0.bit)$	*1	
	OR1	CY, fmem.bit	2	2	$CY \leftarrow CY \vee (fmem.bit)$	*4	
		CY, pmem.@L	2	2	$CY \leftarrow CY \vee (pmem7:2+L3:2.bit(L1:0))$	*5	
		CY, @H+mem.bit	2	2	$CY \leftarrow CY \vee (H+mem3:0.bit)$	*1	
	XOR1	CY, fmem.bit	2	2	$CY \leftarrow CY \vee (fmem.bit)$	*4	
		CY, pmem.@L	2	2	$CY \leftarrow CY \vee (pmem7:2+L3:2.bit(L1:0))$	*5	
		CY, @H+mem.bit	2	2	$CY \leftarrow CY \vee (H+mem3:0.bit)$	*1	

Instructions	Mne- monics	Operand	Bytes	Ma- chine Cyc- les	Operation	Addressing Area	Skip Conditions
Branch	BR	addr	—	—	• μPD75104A PC₁₁₋₀ ← addr (The most suitable instruction is selectable from among BRCB ! caddr, and BR \$ addr depending on the assembler.) • μPD75108A PC₁₂₋₀ ← addr (The most suitable instruction is selectable from among BR ! addr, BRCB ! caddr, and BR \$ addr depending on the assembler.)	*6	
		! addr	3	3	• μPD75108A PC₁₂₋₀ ← addr	*6	
		\$ addr	1	2	• μPD75104A PC₁₁₋₀ ← addr • μPD75108A PC₁₂₋₀ ← addr	*7	
		BRCB	! caddr	2	• μPD75104A PC₁₁₋₀ ← caddr₁₁₋₀ • μPD75108A PC₁₂₋₀ ← PC₁₂ + caddr₁₁₋₀	*8	
		BR	PCDE	3	• μPD75104A PC₁₁₋₀ ← PC₁₁₋₀ + DE • μPD75108A PC₁₂₋₀ ← PC₁₂₋₀ + DE		
					• μPD75104A PC₁₁₋₀ ← PC₁₁₋₀ + XA • μPD75108A PC₁₂₋₀ ← PC₁₂₋₀ + XA		
	Subrou- tine/ Stack Control	CALL	! addr	3	• μPD75104A (SP-4)(SP-1)(SP-2) ← PC₁₁₋₀ (SP-3) ← MBE, RBE, 0, 0 PC₁₁₋₀ ← addr, SP ← SP-4 • μPD75108A (SP-4)(SP-1)(SP-2) ← PC₁₁₋₀ (SP-3) ← MBE, RBE, 0, PC₁₂ PC₁₂₋₀ ← addr, SP ← SP-4	*6	

Instructions	Mne- monics	Operand	Bytes	Ma- chine Cyc- les	Operation	Addressing Area	Skip Conditions
Subrou- tine/ Stack Control (Cont'd)	CALLF	! faddr	2	2	• μPD75104A (SP-4)(SP-1)(SP-2) ← PC₁₁₋₀ (SP-3) ← MBE, RBE, 0, 0 PC₁₁₋₀ ← 0, faddr, SP ← SP-4 • μPD75108A (SP-4)(SP-1)(SP-2) ← PC₁₁₋₀ (SP-3) ← MBE, RBE, 0, PC₁₂ PC₁₂₋₀ ← 00, faddr, SP ← SP-4	*9	
	RET		1	3	• μPD75104A MBE, RBE, x, x ← (SP+1) PC₁₁₋₀ ← (SP)(SP+3)(SP+2) SP ← SP+4 • μPD75108A MBE, RBE, x, PC₁₂ ← (SP+1) PC₁₁₋₀ ← (SP)(SP+3)(SP+2) SP ← SP+4		
	RETS		1	3+S	• μPD75104A MBE, RBE, x, x ← (SP+1) PC₁₁₋₀ ← (SP)(SP+3)(SP+2) SP ← SP+4, then skip unconditionally • μPD75108A MBE, RBE, x, PC₁₂ ← (SP+1) PC₁₁₋₀ ← (SP)(SP+3)(SP+2) SP ← SP+4, then skip unconditionally		Unconditioned
	RETI		1	3	• μPD75104A MBE, RBE, x, x ← (SP+1) PC₁₁₋₀ ← (SP)(SP+3)(SP+2) PSW ← (SP+4)(SP+5), SP ← SP+6 • μPD75108A MBE, RBE, x, PC₁₂ ← (SP+1) PC₁₁₋₀ ← (SP)(SP+3)(SP+2) PSW ← (SP+4)(SP+5), SP ← SP+6		
	PUSH	rp	1	1	(SP-1)(SP-2) ← rp, SP ← SP-2		
		BS	2	2	(SP-1) ← MBS, (SP-2) ← RBS, SP ← SP-2		
	POP	rp	1	1	rp ← (SP+1)(SP), SP ← SP+2		
		BS	2	2	MBS ← (SP+1), RBS ← (SP), SP ← SP+2		

Instructions	Mne- monics	Operand	Bytes	Ma- chine Cyc- les	Operation	Addressing Area	Skip Conditions
Inter- rupt Control	EI		2	2	IME (IPS.3) ← 1		
		IExxx	2	2	IExxx ← 1		
	DI		2	2	IME (IPS.3) ← 0		
		IExxx	2	2	IExxx ← 0		
I/O	IN*	A, PORT _n	2	2	A ← PORT _n (n = 0-9, 12-14)		
		XA, PORT _n	2	2	XA ← PORT _{n+1} , PORT _n (n = 4, 8, 9, 12)		
	OUT*	PORT _n , A	2	2	PORT _n ← A (n = 2-9, 12-14)		
		PORT _n , XA	2	2	PORT _{n+1} , PORT _n ← XA (n = 4, 8, 9, 12)		
CPU Control	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		
Special	SEL	RB _n	2	2	RBS ← n (n = 0-3)		
		MB _n	2	2	MBS ← n (n = 0, 1, 15)		
	GETI	taddr	1	3	• μPD75104A • Where TBR instruction, PC_{11:0} ← (taddr)_{3:0}+(taddr+1) • Where TCALL instruction, (SP-4)(SP-1)(SP-2) ← PC_{11:0} (SP-3) ← MBE, RBE, 0, 0 PC_{11:0} ← (taddr)_{3:0}+(taddr+1) SP ← SP-4 • Except for TBR and TCALL instructions, Instruction execution of (taddr)(taddr+1)	*10	Depends on referenced instruction
					• μPD75108A • Where TBR instruction, PC_{12:0} ← (taddr)_{4:0}+(taddr+1) • Where TCALL instruction, (SP-4)(SP-1)(SP-2) ← PC_{11:0} (SP-3) ← MBE, RBE, 0, PC₁₂ PC_{12:0} ← (taddr)_{4:0}+(taddr+1) SP ← SP-4 • Except for TBR and TCALL instructions, Instruction execution of (taddr)(taddr+1)		

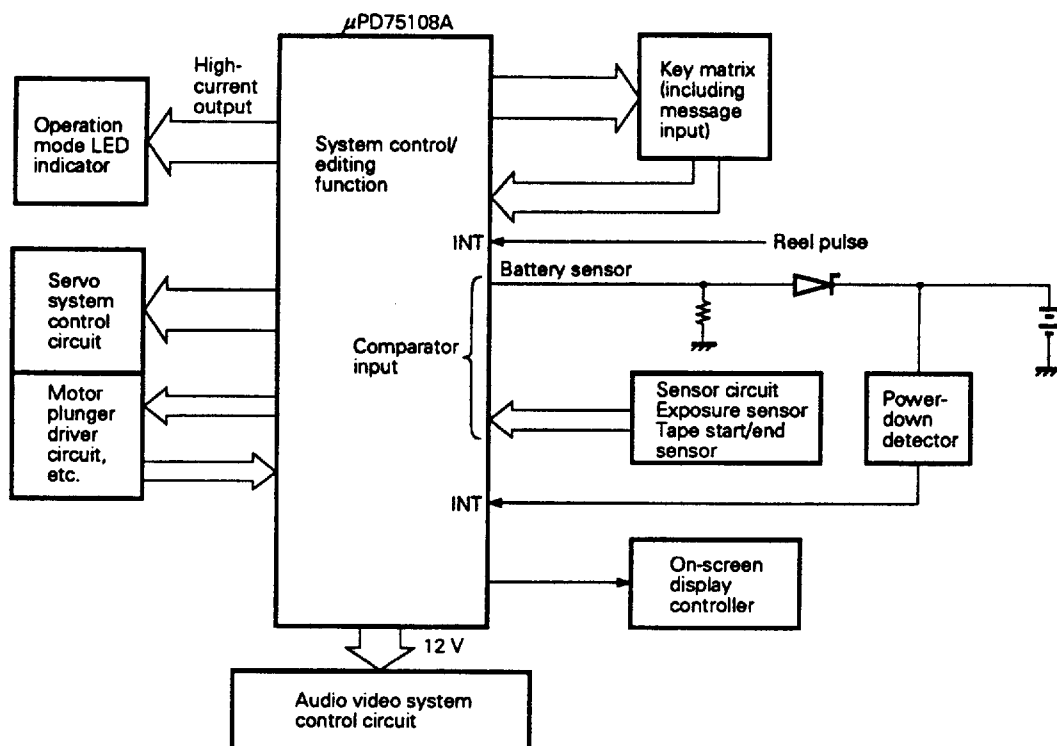
*: When executing the IN/OUT instruction, MBE = 0, or MBE = 1, and MBS = 15.

Remarks: TBR and TCALL instructions are assembler instructions for GETI instruction table definition.

★

10. APPLICATION EXAMPLES

10.1 VCR CAMERA



11. MASK OPTION SELECTION

μPD75108A has the following mask options. Options to be built in can be selected.

(1) Pin

Pin	Mask Option
P10 - P13	Pull-down resistor can be built in bitwise.
P40 - P43	
P50 - P53	
P60 - P63	
P70 - P73	
P80 - P83	
P90 - P93	
P120 - P123	
P130 - P133	
P140 - P143	

(2) Power-ON reset generation circuit, power-ON flag (PONF)

One from the following three ways can be selected.

Mask Option Specification		Switching Selection (Refer to Fig. 8-1.)		Internal Reset Signal (RES)
Power-On Reset Generator Circuit	Power-On Flag (PONF)	SWA	SWB	
Provided	Provided	ON	ON	Generates automatically
Not provided	Provided	ON	OFF	Not generate autoamtically
Not provided	Not provided	OFF	OFF	—

12. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply Voltage	V _{DD}			-0.3 to +7.0	V
Input Voltage	V _{I1}	Other than ports 12 to 14		-0.3 to V _{DD} +0.3	V
	V _{I2} *1	Ports 12 to 14	w/pull-up resistor	-0.3 to V _{DD} +0.3	V
			Open drain	-0.3 to +13	V
Output Voltage	V _O			-0.3 to V _{DD} +0.3	V
High-Level Output Current	I _{OH}	1 pin		-15	mA
		All pins		-30	mA
Low-Level Output Current	I _{OL} *2	1 pin	Peak	30	mA
			rms	15	mA
		Total of ports 0, 2 to 4, 12 to 14	Peak	100	mA
			rms	60	mA
		Total of ports 5 to 9	Peak	100	mA
			rms	60	mA
Operating Temperature	T _{opt}			-40 to +85	°C
Storage Temperature	T _{stg}			-65 to +150	°C

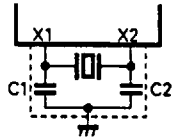
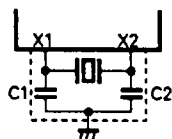
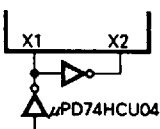
*1: The power supply impedance (pull-up resistor) must be 50 kΩ or higher when a voltage higher than 10 V is applied to ports 12 to 14.

2: $rms = Peak\ value \times \sqrt{Duty}$

- ★ Note: Even if one of the parameters exceed its absolute maximum rating even momentarily, the quality of the product may be degraded. The absolute maximum rating therefore specifies the upper or lower limit of the value at which the product can be used without physical damages. Be sure not to exceed or fall below this value when using the product.

OSCILLATOR CIRCUIT CHARACTERISTICS

(T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Oscillator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic		Oscillation frequency(f _{osc})*1	V _{DD} = Oscillation voltage range	2.0		5.0*3	MHz
		Oscillation stabilization time*2	After V _{DD} come to MIN. of oscillation voltage range	4			ms
Crystal		Oscillation frequency (f _{osc})*1		2.0	4.19	5.0*3	MHz
		Oscillation stabilization time*2	V _{DD} = 4.5 to 6.0 V	10			ms
				30			ms
External Clock		X1 input frequency (f _x)*1		2.0		5.0*3	MHz
		X1 input high-, low-level widths (t _{xH} , t _{xL})		100		250	ns

*1: The oscillation frequency and X1 input frequency are indicated only to express the characteristics of the oscillator circuit. For instruction execution time, refer to AC Characteristics.

2: Time required for oscillation to stabilize after V_{DD} has come to MIN. of oscillation voltage range or the STOP mode has been released.

3: When the oscillation frequency is 4.19 MHz < f_{osc} ≤ 5.0 MHz, do not select PCC = 0011 as the instruction execution time: otherwise, one machine cycle is set to less than 0.95 μs, falling short of the rated minimum value of 0.95 μs.

Note: When using the oscillation circuit of the system clock, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity:

- Keep the wiring length as short as possible.
- Do not cross the wiring over the other signal lines. Also, do not route the wiring in the vicinity of lines through which a high alternating current flows.
- Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V_{SS}. Do not connect the ground pattern through which a high current flows.
- Do not extract signals from the oscillation circuit.

RECOMMENDED OSCILLATOR CIRCUITS CONSTANTS
RECOMMENDED CERAMIC OSCILLATORS

Manufacturer	Product Name	External Capacitance (pF)		Oscillation Voltage Range (V)	
		C1	C2	MIN.	MAX.
Murata Mfg. Co., Ltd.	CSA 2.00MG	30	30	2.7	6.0
	CSA 4.19MG	30	30	3.0	6.0
	CSA 4.19MGU	30	30	2.7	6.0
	CST 4.19T	Provided	Provided	3.0	6.0
Kyoto Ceramic Co., Ltd.	KBR-2.0MS	100	100	3.0	6.0
	KBR-4.0MS	33	33	3.0	6.0
	KBR-4.19MS	33	33	3.0	6.0
	KBR-4.9152M	33	33	3.0	6.0

RECOMMENDED CRYSTAL OSCILLATOR

Manufacturer	Product Name	External Capacitance (pF)		Oscillation Voltage Range (V)	
		C1	C2	MIN.	MAX.
Kinseki	HC-49/U	22	22	2.7	6.0

Note: Use a crystal oscillator with an equivalent series resistance of 80Ω or less.

DC CHARACTERISTICS (T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V _{IH1}	Other than below		0.7V _{DD}		V _{DD}	V
	V _{IH2}	Ports 0, 1, TIO, 1, RESET		0.8 V _{DD}		V _{DD}	V
	V _{IH3}	Ports 12 to 14	Pull-up resistor	0.7 V _{DD}		V _{DD}	V
			Open drain	0.7 V _{DD}		12	V
	V _{IH4}	X1, X2		V _{DD} -0.5		V _{DD}	V
Low-Level Input Voltage	V _{IL1}	Other than below		0		0.3 V _{DD}	V
	V _{IL2}	Ports 0, 1, TIO, 1, RESET		0		0.2 V _{DD}	V
	V _{IL3}	X1, X2		0		0.4	V
High-Level Output Voltage	V _{OH}	V _{DD} = 4.5 to 6.0 V, I _{OH} = -1 mA		V _{DD} -1.0			V
		I _{OH} = -100 μA		V _{DD} -0.5			V
Low-Level Output Voltage	V _{OL}	V _{DD} = 4.5 to 6.0 V	Ports 0, 2 to 9, I _{OL} = 15 mA		0.35	2.0	V
			Ports 12 to 14, I _{OL} = 10 mA		0.35	2.0	V
		V _{DD} = 4.5 to 6.0 V, I _{OL} = 1.6 mA				0.4	V
		I _{OL} = 400 μA				0.5	V
High-Level Input Leakage Current	I _{LIH1}	V _{IN} = V _{DD}	Other than below			3	μA
	I _{LIH2}		X1, X2			20	μA
	I _{LIH3}	V _{IN} = 12 V	Ports 12 to 14 (open drain)			20	μA
Low-Level Input Leakage Current	I _{LIL1}	V _{IN} = 0 V	Other than X1, X2			-3	μA
	I _{LIL2}		X1, X2			-20	μA
High-Level Output Leakage Current	I _{LOH1}	V _{OUT} = V _{DD}	Other than below			3	μA
	I _{LOH2}	V _{OUT} = 12 V	Ports 12 to 14 (open drain)			20	μA
Low-Level Output Leakage Current	I _{LOL}	V _{OUT} = 0 V				-3	μA
Internal Pull-Up Resistor	R _L	Ports 1, 4 to 9, and 12 to 14	V _{DD} = 5 V±10%	15	40	70	kΩ
				10		80	kΩ
Supply Current*1	I _{DD1}	4.19MHz crystal	V _{DD} = 5 V±10%*2		3	9	mA
			V _{DD} = 3 V±10%*3		0.55	1.5	mA
	I _{DD2}	oscillator C1 = C2 = 22pF	HALT mode V _{DD} = 5 V±10%		600	1800	μA
			V _{DD} = 3 V±10%		200	600	μA
	I _{DD3}	STOP mode, V _{DD} = 3 V±10%			0.1	10	μA

*1: The current flowing into the internal pull-up resistor, power-ON reset circuit (mask option), and comparator circuit is not included.

2: When the high-speed mode is set by setting the processor clock control register (PCC) to 0011.

3: When the low-speed mode is set by setting the PCC to 0000.

CAPACITANCE ($T_a = 25^\circ\text{C}$, $V_{DD} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{IN}	$f = 1\text{ MHz}$ Pins other than those measured are at 0 V			15	pF
Output Capacitance	C_{OUT}				15	pF
Input/Output Capacitance	C_{IO}				15	pF

COMPARATOR CHARACTERISTICS ($T_a = -40$ to $+85^\circ\text{C}$, $V_{DD} = 4.5$ to 6.0 V)

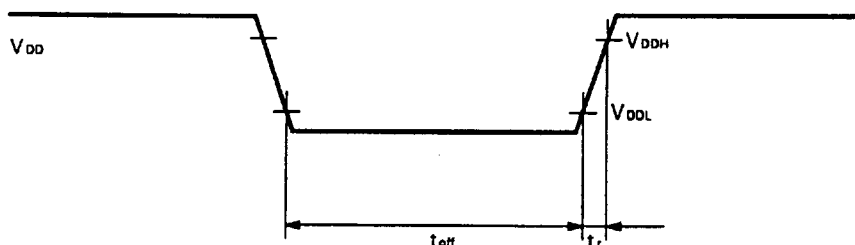
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Comparison Accuracy	V_{ACOMP}				± 100	mV
Threshold Voltage	V_{TH}		0		V_{DD}	V
PTH Input voltage	V_{PTH}		0		V_{DD}	V
Comparator circuit current dissipation		PTHM7 is set to "1"		1		mA

POWER-ON RESET CIRCUIT CHARACTERISTICS (MASK OPTION) ($T_a = -40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power-On Reset High-Level Operating Voltage	V_{DDH}		4.5		6.0	V
Power-On Reset Low-Level Operating Voltage	V_{DDL}		0		0.2	V
Supply Voltage Rise Time	t_r		10		*1	μs
Supply Voltage Off Time	t_{off}		1			s
Power-On Reset Circuit Current Dissipation*2	I_{OPR}	$V_{DD} = 5\text{ V} \pm 10\%$		10	100	μA
		$V_{DD} = 2.5\text{ V}$		2	20	μA

*1: $2^{17}/f_{xx}$ (31.3 ms at $f_{xx} = 4.19\text{ MHz}$)

*2: Current flowing when power-ON reset circuit or power-ON Flag is incorporated.

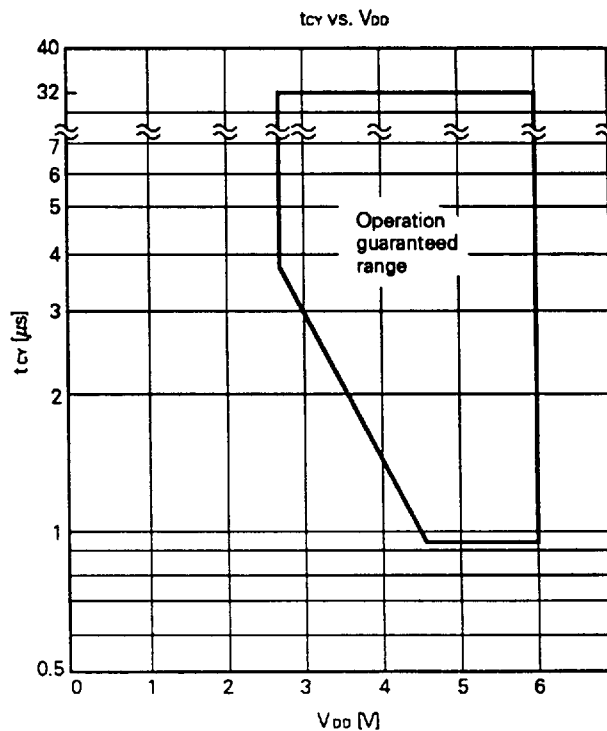


Note: Apply power gradually and smoothly.

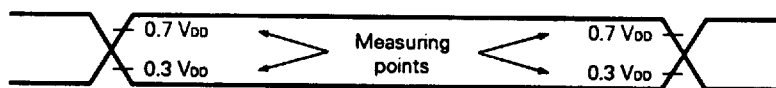
AC CHARACTERISTICS ($T_a = -40$ to $+85^\circ\text{C}$, $V_{DD} = 2.7$ to 6.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU Clock Cycle Time* (Minimum Instruction Execution Time = 1 Machine Cycle)	t _{cy}	$V_{DD} = 4.5$ to 6.0 V	0.95		32	μs
			3.8		32	μs
TIO, TI1 Input Frequency	f _{TI}	$V_{DD} = 4.5$ to 6.0 V	0		1	MHz
			0		275	kHz
TIO, TI1 Input High-/Low-Level Width	t _{TIH} , t _{TIL}	$V_{DD} = 4.5$ to 6.0 V	0.48			μs
			1.8			μs
SCK Cycle Time	t _{SCK}	$V_{DD} = 4.5$ to 6.0 V	Input	0.8		μs
			Output	0.95		μs
			Input	3.2		μs
			Output	3.8		μs
SCK High-/Low-Level Width	t _{SCKH} , t _{SCKL}	$V_{DD} = 4.5$ to 6.0 V	Input	0.4		μs
			Output	t _{SCK} /2-50		ns
			Input	1.6		μs
			Output	t _{SCK} /2-150		ns
SI Setup Time (vs. SCK↑)	t _{SIK}		100			ns
SI Hold Time (vs. SCK↑)	t _{SIL}		400			ns
SCK ↓→ SO Output delay Time	t _{SCKSO}	$V_{DD} = 4.5$ to 6.0 V			300	ns
					1000	ns
INT0 to INT4 High-/Low-Level Width	t _{INTH} , t _{INTL}		5			μs
RESET Low-Level Width	t _{RESL}		5			μs

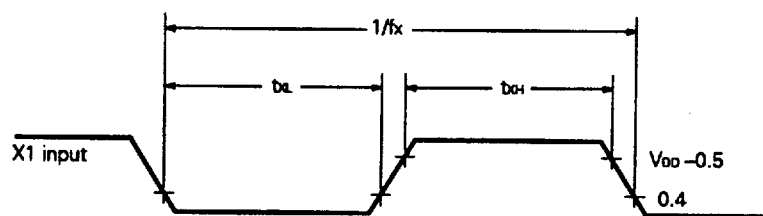
*: The cycle time of the CPU clock (Φ) is determined by the input frequency of the ceramic or crystal oscillator circuit and the set value of the processor clock control register.
The t_{cy} vs. V_{DD} characteristics are as shown on the right.



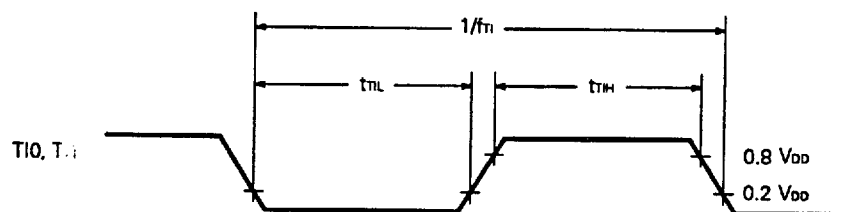
AC TIMING MEASURING POINTS (excluding Ports 0, 1, TI0, TI1, X1, X2, and $\overline{\text{RESET}}$)



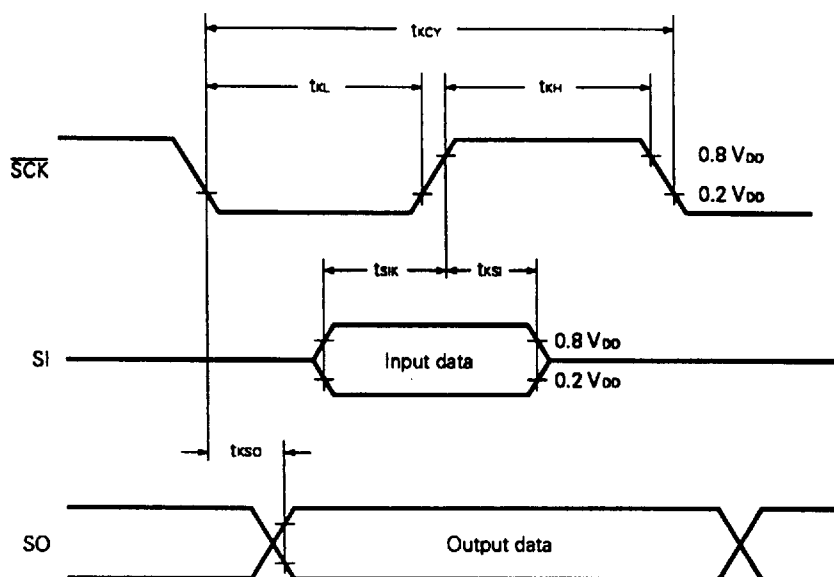
CLOCK TIMING



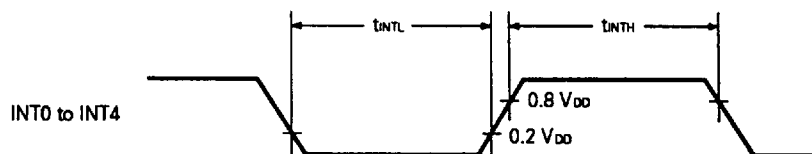
TI INPUT TIMING



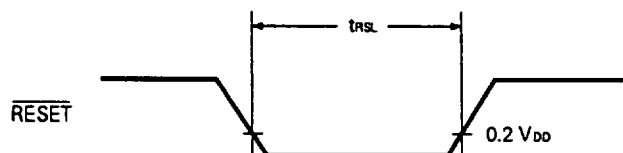
SERIAL TRANSFER TIMING



INTERRUPT INPUT TIMING



RESET INPUT TIMING



LOW-VOLTAGE DATA RETENTION CHARACTERISTICS OF DATA MEMORY IN STOP MODE

(T_a = -40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data Retention Supply Voltage	V _{DDDR}		2.0		6.0	V
Data Retention Supply Current*1	I _{DDDR}	V _{DDDR} = 2.0 V		0.1	10	μA
Release Signal Set Time	t _{SREL}		0			μs
Oscillation Stabilization Wait Time*2	t _{WAIT}	Released by $\overline{\text{RESET}}$		2 ¹⁷ /f _x		ms
		Released by interrupt request		*3		ms

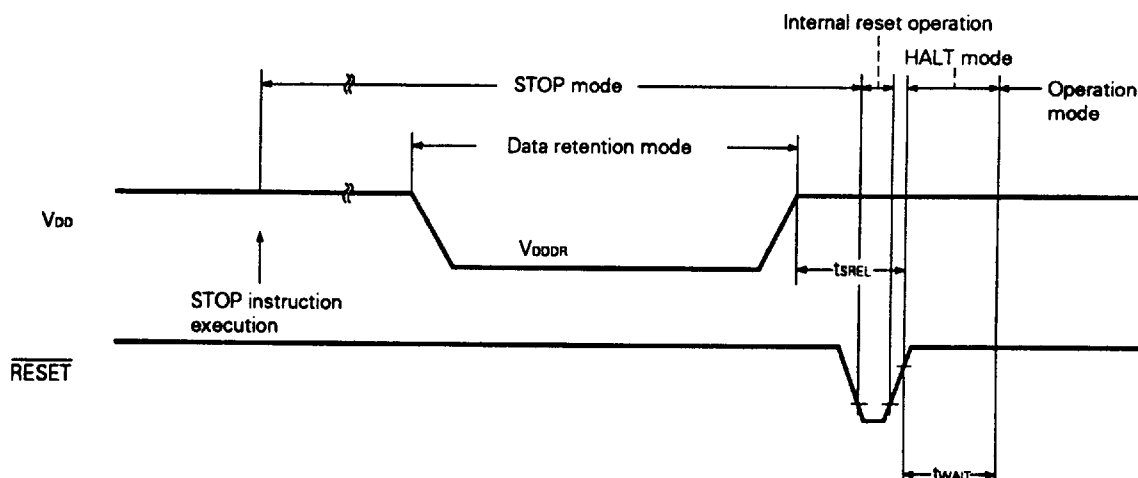
*1: The current flowing through internal pull-up resistor, power-ON reset circuit (mask option), and comparator circuit is not included

2: The oscillation stabilization wait time is the time during which the CPU is stopped to prevent unstable operation when oscillation is started.

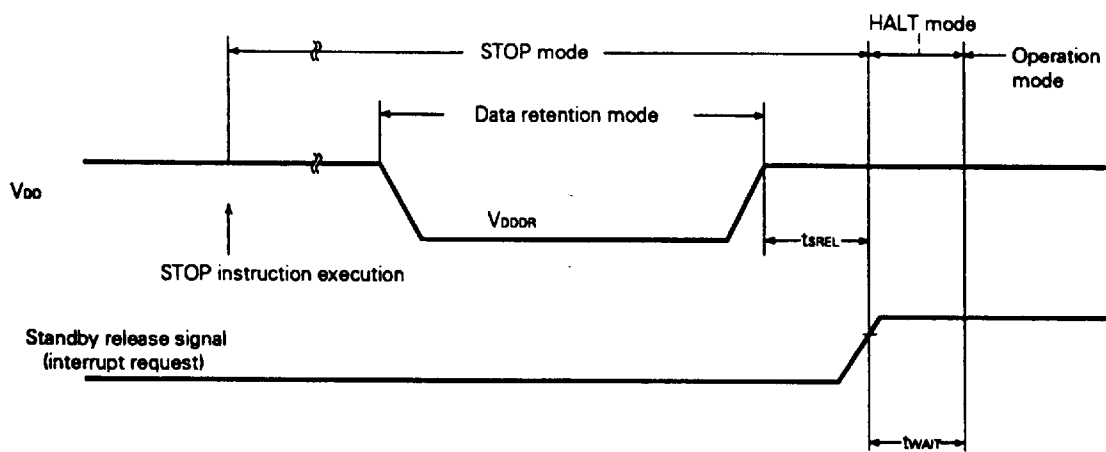
3: Depends on the setting of the basic interval timer mode register (BTM) as follows:

BTM3	BTM2	BTM1	BTM0	Wait time (): f _{xx} = 4.19 MHz
-	0	0	0	2 ²⁰ /f _{xx} (approx. 250 ms)
-	0	1	1	2 ¹⁷ /f _{xx} (approx. 31.3 ms)
-	1	0	1	2 ¹⁸ /f _{xx} (approx. 7.82 ms)
-	1	1	1	2 ¹³ /f _{xx} (approx. 1.95 ms)

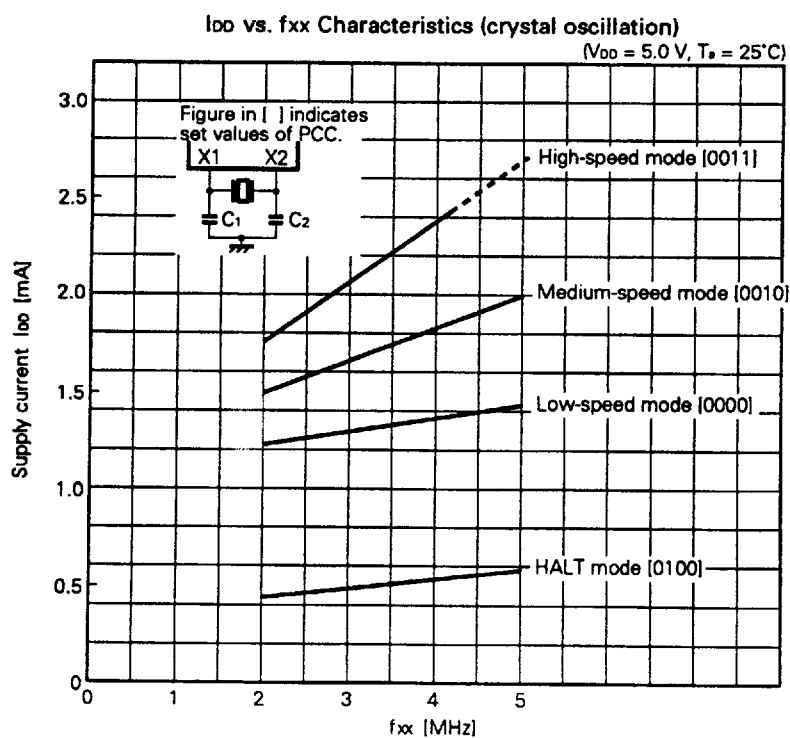
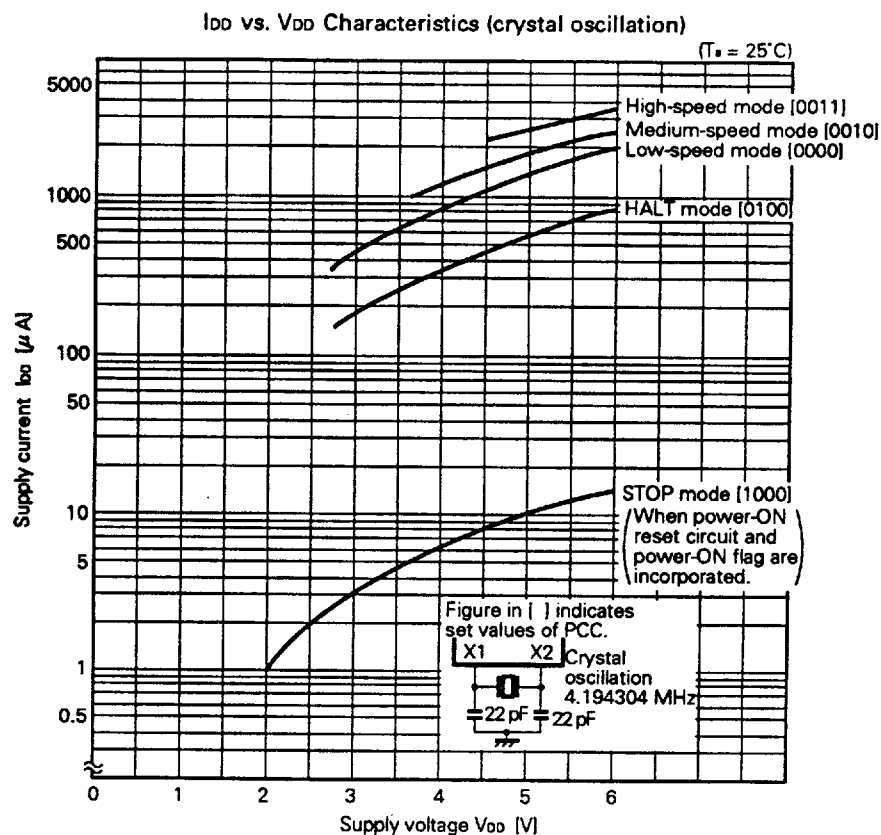
DATA RETENTION TIMING (releasing STOP mode by $\overline{\text{RESET}}$)

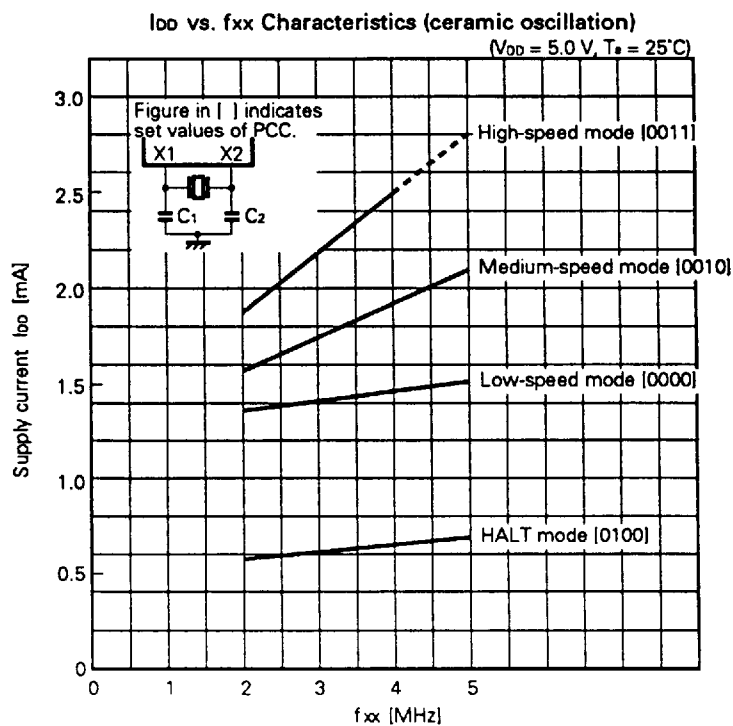
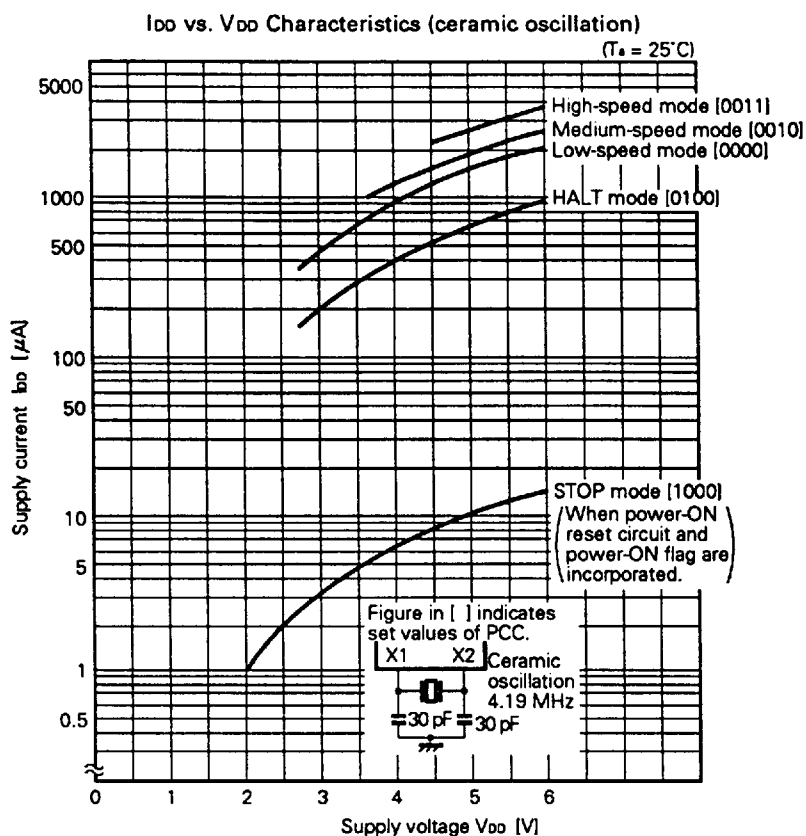


DATA RETENTION TIMING (standby release signal: releasing STOP mode by interrupt)

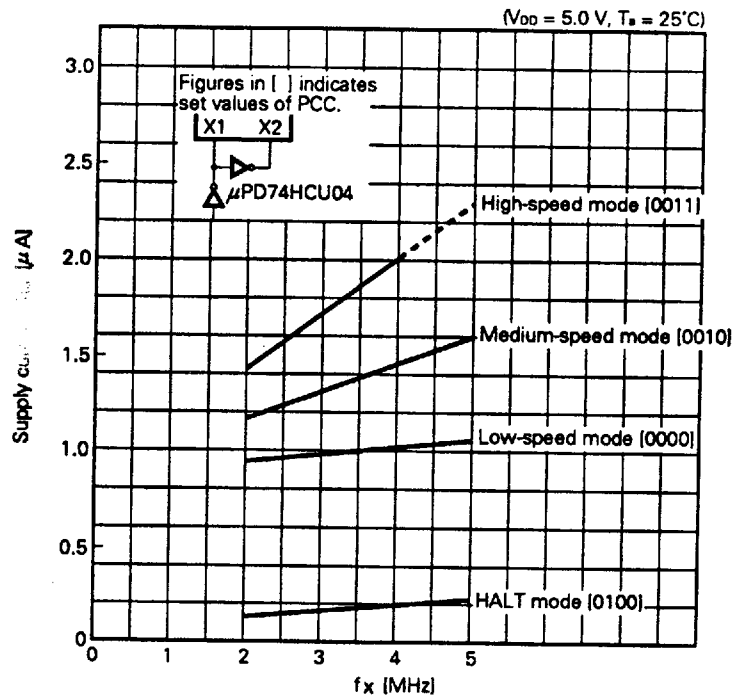


13. CHARACTERISTIC DATA (REFERENCE VALUE)

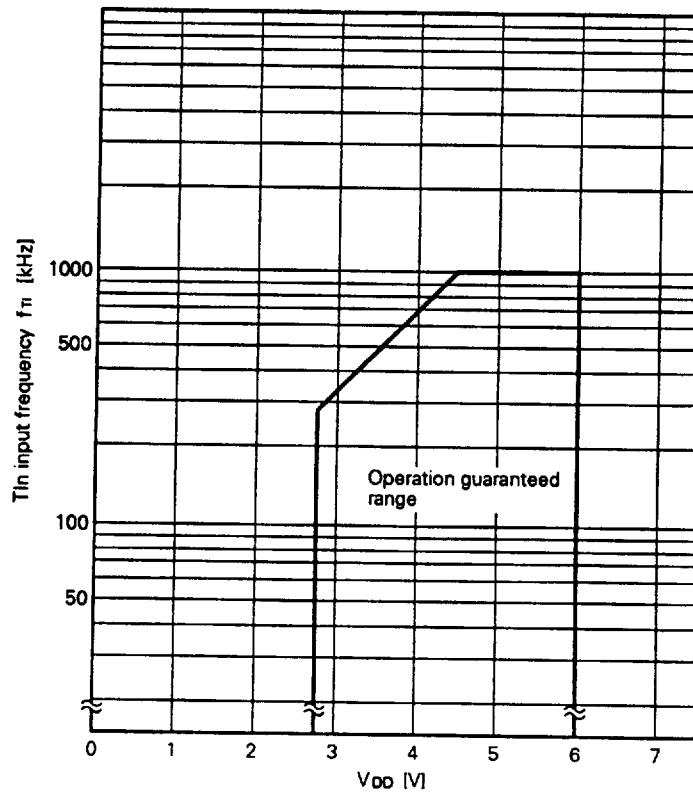




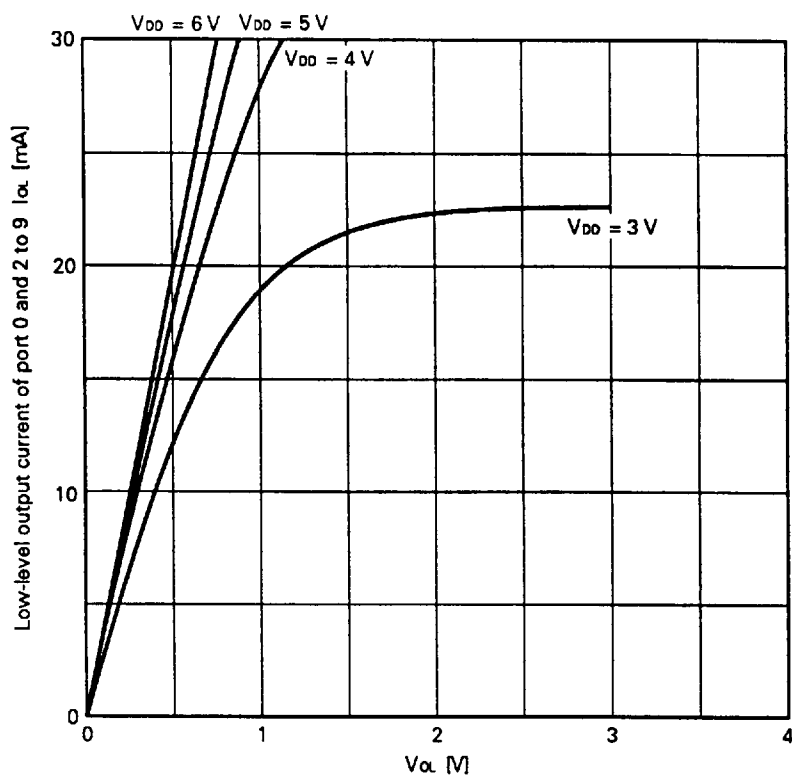
I_{DD} vs. f_x Characteristics (external clock)



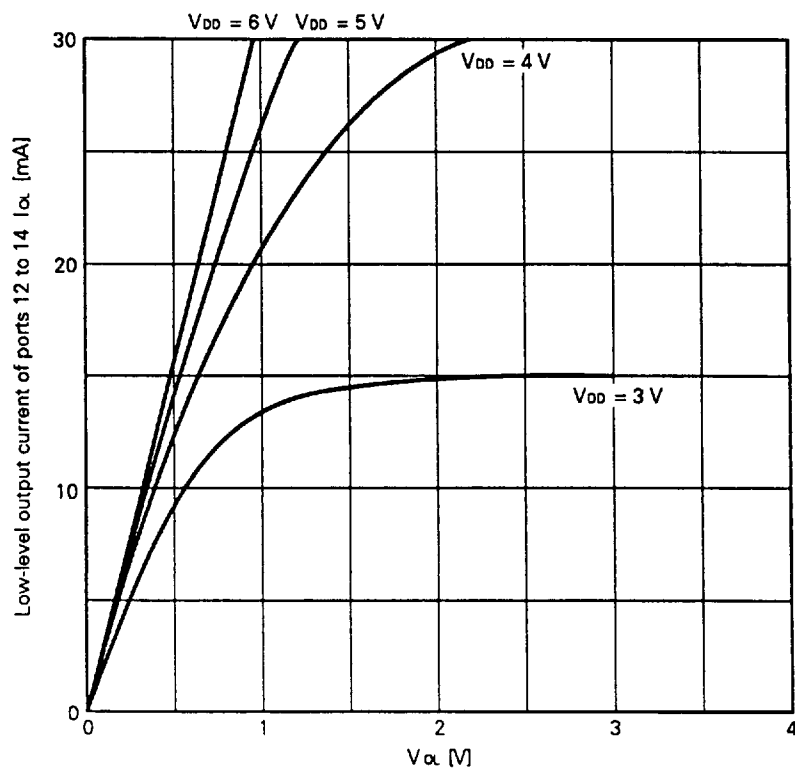
f_{in} vs. V_{DD} Characteristics

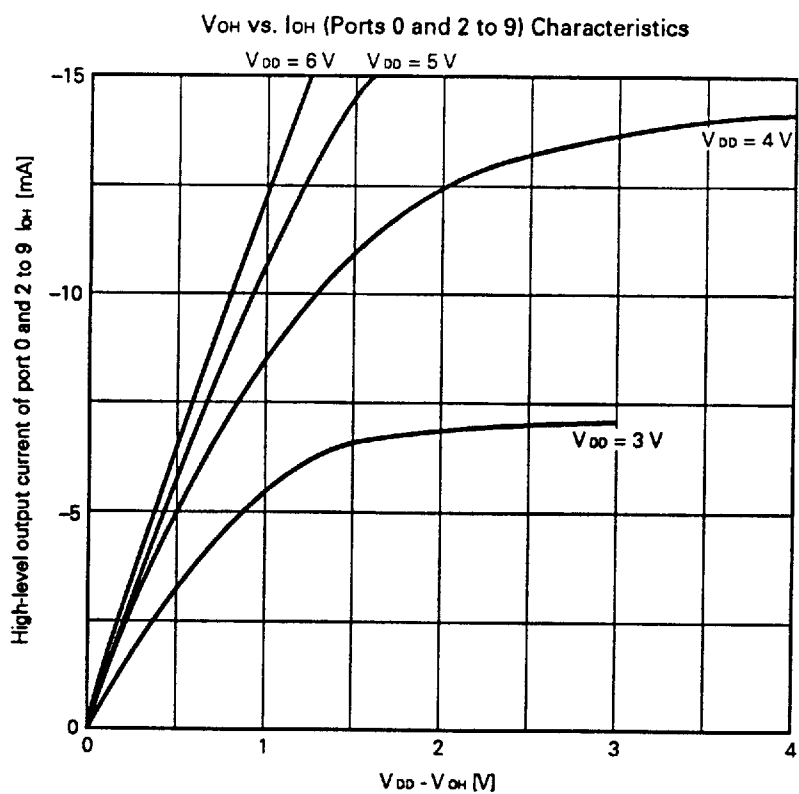


V_{OL} vs. I_{OL} (Ports 0 and 2 to 9) Characteristics



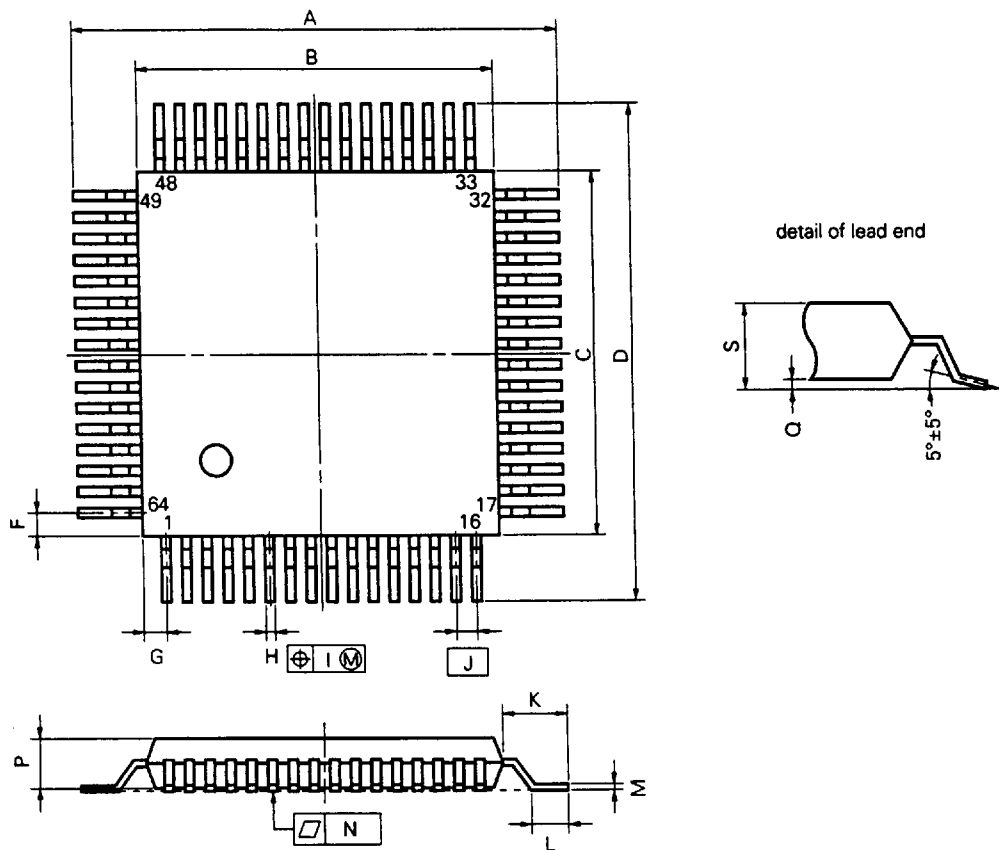
V_{OL} vs. I_{OL} (Ports 12 to 14) Characteristics





14. PACKAGE DRAWINGS

64 PIN PLASTIC QFP (□14)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

P64GC-80-AB8-3

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	0.551 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	0.014 ^{+0.004} _{-0.005}
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

15. RECOMMENDED SOLDERING CONDITIONS

It is recommended that μPD75104A, 75106A, and 75108A be soldered under the following conditions.

For details on the recommended soldering conditions, refer to Information Document "Semiconductor Devices Mounting Manual" (IEI-616).

For other soldering methods and conditions, please consult NEC.

Table 15-1 Soldering Conditions of Surface Mount Type

(1) μPD75108AGC - xxx - AB8: 64-pin plastic QFP (□ 14 mm)

Soldering Method	Soldering Conditions	Symbol for Recommended Condition
Infrared Reflow	Package peak temperature: 230°C, time: 30 seconds max. (210°C min.), number of times: 1	IR30-00-1
VPS	Package peak temperature: 215°C, time: 40 seconds max. (200°C min.), number of times: 1	VP15-00-1
Wave Soldering	Soldering bath temperature: 260°C max., time: 10 seconds max., number of times: 1, pre-heating temperature: 120°C max. (package surface temperature)	WS60-00-1
Pin Partial Heating	Pin temperature: 300°C max., time: 3 seconds max. (per side)	—

(2) μPD75104AGC - xxx - AB8: 64-pin plastic QFP (□ 14 mm)

Soldering Method	Soldering Conditions	Symbol for Recommended Condition
Infrared Reflow	Package peak temperature: 230°C, time: 30 seconds max. (210°C min.), number of times: 1, number of days: 2 days*, (afterwards, 16 hours of prebaking at 125°C is required.)	IR30-162-1
VPS	Package peak temperature: 215°C, time: 40 seconds max. (200°C min.), number of times: 1, number of days: 2 days*, (afterwards, 16 hours of prebaking at 125°C is required.)	VP15-162-1
Wave Soldering	Soldering bath temperature: 260°C max., time: 10 seconds max., number of times: 1, pre-heating temperature: 120°C max. (package surface temperature), number of days: 2 days*, (afterwards, 16 hours of prebaking at 125°C is required.)	WS60-162-1
Pin Partial Heating	Pin temperature: 300°C max., time: 3 seconds max. (per side)	—

*: This means the number of days after unpacking the dry pack. Storage conditions are 25°C and 65% RH max.

Caution: Do not use two or more soldering methods in combination (except the pin partial heating method).

Notice

A model that can be soldered under the more stringent conditions (infrared reflow peak temperature: 235°C, number of times: 2, and an extended number of days) is also available.
For details, consult NEC.

APPENDIX A. FUNCTIONAL DIFFERENCES AMONG THIS SERIES PRODUCTS

Item	μPD75104	μPD75106	μPD75108	μPD75112	μPD75116	μPD75104A	μPD75108A	μPD75108B	μPD75116
Program Memory	- Mask ROM 0000H-0FFFH 4096 x 8 bits	- Mask ROM 0000H-177FH 6016 x 8 bits	- Mask ROM 0000H-177FH 8064 x 8 bits	- Mask ROM 0000H-277FH 12160 x 8 bits	- Mask ROM 0000H-377FH 16256 x 8 bits	- Mask ROM 0000H-0FFFH 4096 x 8 bits	- Mask ROM 0000H-177FH 8064 x 8 bits	- One-time PROM 0000H-177FH 8064 x 8 bits	- One-time PROM 0000H-377FH 16256 x 8 bits
Data Memory	320 x 4 bits { Bank 0: 256 x 4 } { Bank 1: 64 x 4 }	320 x 4 bits { Bank 0: 256 x 4 } { Bank 1: 64 x 4 }	512 x 4 bits { Bank 0: 256 x 4 } { Bank 1: 256 x 4 }	512 x 4 bits { Bank 0: 256 x 4 } { Bank 1: 256 x 4 }	512 x 4 bits { Bank 0: 256 x 4 } { Bank 1: 256 x 4 }	320 x 4 bits { Bank 0: 256 x 4 } { Bank 1: 64 x 4 }	- Mask ROM 0000H-0FFFH 4096 x 8 bits	- Mask ROM 0000H-177FH 8064 x 8 bits	- One-time PROM 0000H-177FH 8064 x 8 bits
Instruction Set	Provided with BR laddr instruction except for μPD75104 and 75104A								
I/O Lines	58								
Total I/O	- CMOS I/O: 32 +12 V withstand open-drain output: 12 (pull-up resistor as mask option) - LED direct drive: 44								
Input	- CMOS I/O: 32 (pull-up resistor as mask option: 24) +12 V withstand open-drain output : 12 (pull-up resistor as mask option) - LED direct drive: 44								
Power-ON Reset Circuit	- CMOS input: 10 - Comparator input: 4								
Power-ON Flag	Not provided								
Operating Voltage Range	2.7 to 6.0 V								
Pin Connections	Depends on package. Only μPD75116 has V _{PP} pin.								
Package	64-pin plastic shrink DIP (750 mil) 64-pin plastic QFP (14 x 20 mm)								

APPENDIX B. DEVELOPMENT TOOLS

The following development support tools are readily available to support development of systems using μPD75108A:

Hardware	IE-75000-R* ¹ IE-75001-R	In-circuit emulator for 75X series
	IE-75000-R-EM* ²	Emulation board for IE-75000-R and IE-75001-R
	EP-75108AGC-R EV-9200GC-64	Emulation probe for μPD75104AGC and 75108AGC. It is provided with a 64-pin conversion socket, EV-9200GC-64
Software	IE Control Program	Host machine
	RA75X Relocatable Assembler	PC-9800 series (MS-DOS™ Ver.3.30 to Ver.5.00A* ³) IBM PC/AT™ (PC DOS™ Ver.3.1)

*1: Maintenance product

2: Not provided with IE-75001-R.

3: Ver.5.00/5.00A has a task swap function, but this function cannot be used with this function.

Remarks: For development tools from other companies, refer to 75X Series Selection Guide (IF-151).