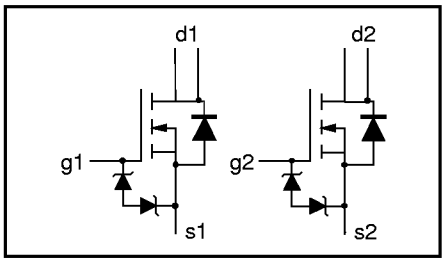
# TrenchMOS™ transistor PHN220

## FEATURES

- 'Trench' technology
- Low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low-profile surface mount package

## SYMBOL




## QUICK REFERENCE DATA

$V_{DSS}$ = 55 V

$I_D$ = 2.6 A

$R_{DS(ON)} \leq 200\ m\Omega$

## GENERAL DESCRIPTION

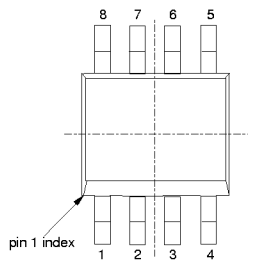
Dual, N-channel, enhancement mode, field-effect power transistors, using '**trench**' technology to achieve very low on-resistance in a low-profile, surface mount package. This device is intended for use in computer disk drives, d.c. to d.c. converters and general purpose switching applications.

The PHN220 is supplied in the SOT96 (SO8) 8-leaded, low profile, surface mounting package.

## PINNING

| PIN | DESCRIPTION |
|---|---|
| 1 | source 1 |
| 2 | gate 1 |
| 3 | source 2 |
| 4 | gate 2 |
| 5-6 | drain 2 |
| 7-8 | drain 1 |

## SOT96 (SO8)




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | - | - | 55 | V |
| $V_{DGR}$ | Drain-gate voltage | $R_{GS}$ = 20 kΩ | - | 55 | V |
| $\pm V_{GS}$ | Gate-source voltage | - | - | 20 | V |
| $I_D$ | Drain current (DC) | $T_{sp}$ = 25 ˚C | - | 2.6 | A |
| | | $T_{sp}$ = 100 ˚C | - | 1.6 | A |
| $I_{DM}$ | Drain current (pulse peak value) | $T_{sp}$ = 25 ˚C | - | 10 | A |
| $P_{tot}$ | Total power dissipation | $T_{sp}$ = 25 ˚C | - | 2.5 | W |
| | | $T_{sp}$ = 100 ˚C | - | 1 | W |
| $T_{stg}$, $T_j$ | Storage & operating temperature | | - 55 | 150 | ˚C |

## ESD LIMITING VALUE

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_C$ | Electrostatic discharge capacitor voltage | Human body model (100 pF, 1.5 kΩ) | - | 2 | kV |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $R_{th\ j\text{-}sp}$ | From junction to solder point | per transistor | 35 | 50 | K/W |
| $R_{th\ j\text{-}amb}$ | From junction to ambient | minimum footprint, FR4 board | 150 | - | K/W |

## ELECTRICAL CHARACTERISTICS

characteristics are per transistor at $T_j$= 25˚C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V; $I_D$ = 0.25 mA | 55 | - | - | V |
| | | $T_j$ = -55˚C | 50 | - | - | V |
| $V_{GS(TO)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$; $I_D$ = 1 mA | 2.0 | 3.0 | 4.0 | V |
| | | $T_j$ = 150˚C | 1.2 | - | - | V |
| | | $T_j$ = -55˚C | - | - | 4.4 | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{DS}$ = 55 V; $V_{GS}$ = 0 V; | - | 0.05 | 10 | µA |
| | | $T_j$ = 150˚C | - | - | 100 | µA |
| $I_{GSS}$ | Gate source leakage current | $V_{GS}$ = ±10 V | - | 0.04 | 1 | µA |
| | | $T_j$ = 150˚C | - | - | 10 | µA |
| $\pm V_{(BR)GSS}$ | Gate source breakdown voltage | $I_G$ = ±1 mA | 16 | - | - | V |
| $R_{DS(ON)}$ | Drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 5 A | - | 150 | 200 | mΩ |
| | | $T_j$ = 150˚C | - | - | 370 | mΩ |
| $g_{fs}$ | Forward transconductance | $V_{DS}$ = 25 V; $I_D$ = 5 A; $T_j$ = 25˚C | 0.5 | 2.5 | - | S |
| $C_{iss}$ | Input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; f = 1 MHz | - | 190 | 240 | pF |
| $C_{oss}$ | Output capacitance | | - | 65 | 80 | pF |
| $C_{rss}$ | Feedback capacitance | | - | 32 | 45 | pF |
| $t_{d\ on}$ | Turn-on delay time | $V_{DD}$ = 30 V; $I_D$ = 5 A; | - | 9 | 14 | ns |
| $t_r$ | Turn-on rise time | $V_{GS}$ = 10 V; $R_G$ = 10 Ω; | - | 28 | 42 | ns |
| $t_{d\ off}$ | Turn-off delay time | | - | 15 | 23 | ns |
| $t_f$ | Turn-off fall time | $T_j$ = 25˚C | - | 8 | 12 | ns |

## REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j$ = -55 to 175˚C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{DR}$ | Continuous reverse drain current | $T_{sp}$ = 25˚C | - | - | 2.6 | A |
| $I_{DRM}$ | Pulsed reverse drain current | $T_{sp}$ = 25˚C | - | - | 10 | A |
| $V_{SD}$ | Diode forward voltage | $I_F$ = 2 A; $V_{GS}$ = 0 V | - | 0.85 | 1.1 | V |
| $t_{rr}$ | Reverse recovery time | $I_F$ = 2 A; -$dI_F$/dt = 100 A/µs; | - | 43 | - | ns |
| $Q_{rr}$ | Reverse recovery charge | $V_{GS}$ = -10 V; $V_R$ = 30 V | - | 0.16 | - | µC |

## AVALANCHE LIMITING VALUE

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $W_{DSS}$ | Drain-source non-repetitive unclamped inductive turn-off energy | $I_D$ = 1.9 A; $V_{DD} \leq$ 25 V; $V_{GS}$ = 10 V; $R_{GS}$ = 50 Ω; $T_{sp}$ = 25 ˚C | - | - | 10 | mJ |

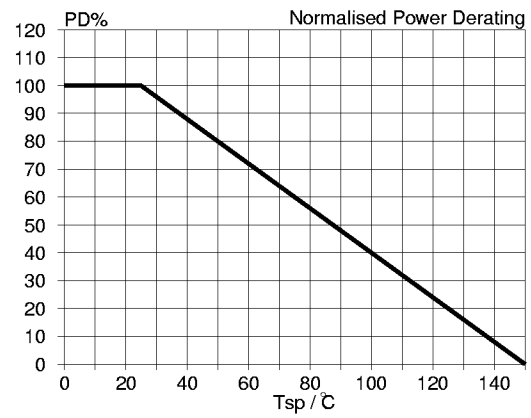



*Fig.1. Normalised power dissipation.*
*PD% = 100·$P_D$/$P_{D\ 25\ °C}$ = f($T_{sp}$)*

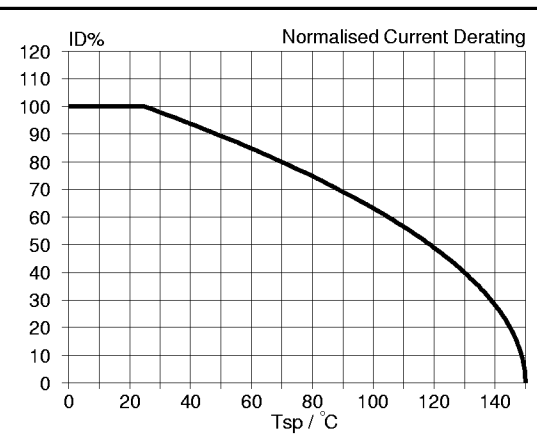



*Fig.2. Normalised continuous drain current.*
*ID% = 100·$I_D$/$I_{D\ 25\ °C}$ = f($T_{sp}$); conditions: $V_{GS}$ ≥ 10 V*

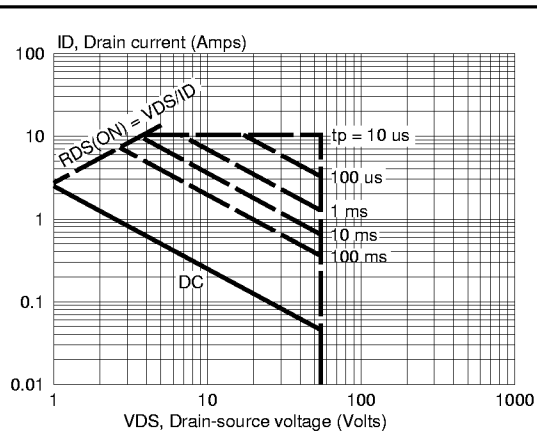



*Fig.3. Safe operating area. $T_{sp}$ = 25 ˚C*
*$I_D$ & $I_{DM}$ = f($V_{DS}$); $I_{DM}$ single pulse; parameter $t_p$*

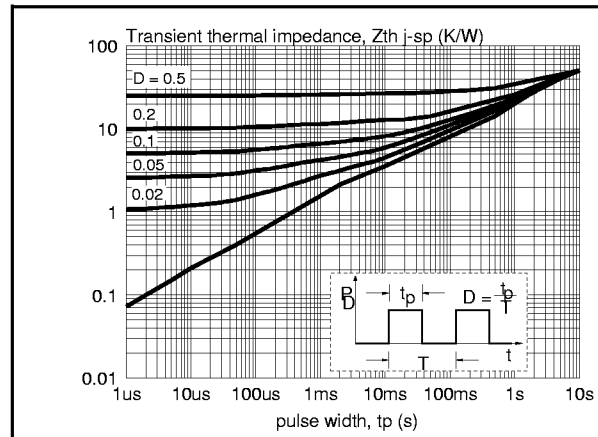



*Fig.4. Transient thermal impedance.*
*$Z_{th\ j\text{-}sp}$ = f(t); parameter D = $t_p$/T*

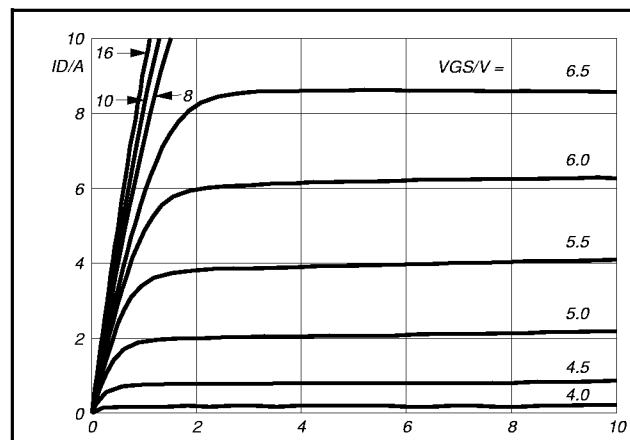



*Fig.5. Typical output characteristics, $T_j$ = 25 ˚C.*
*$I_D$ = f($V_{DS}$); parameter $V_{GS}$*

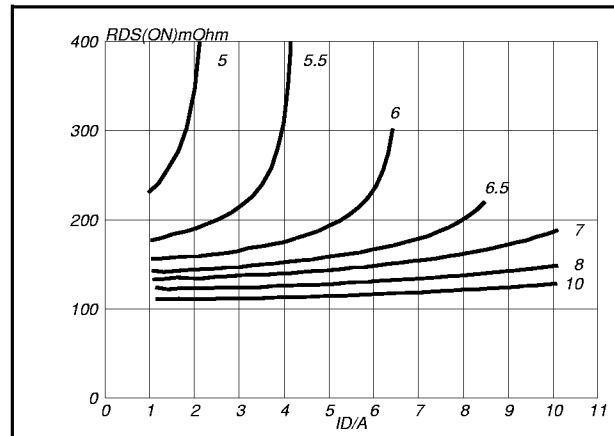



*Fig.6. Typical on-state resistance, $T_j$ = 25 ˚C.*
*$R_{DS(ON)}$ = f($I_D$); parameter $V_{GS}$*

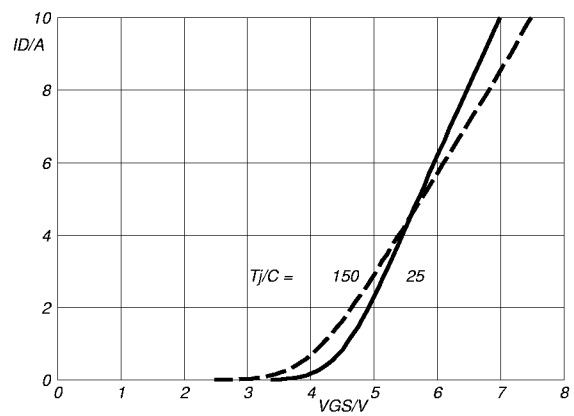



*Fig.7. Typical transfer characteristics.*
*$I_D = f(V_{GS})$ ; conditions: $V_{DS}$ = 25 V; parameter $T_j$*

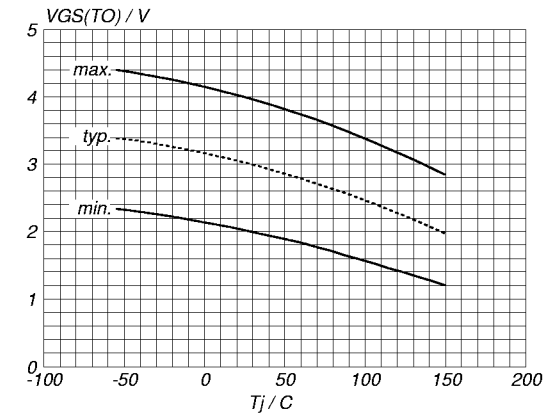



*Fig.10. Gate threshold voltage.*
*$V_{GS(TO)} = f(T_j)$; conditions: $I_D$ = 1 mA; $V_{DS} = V_{GS}$*

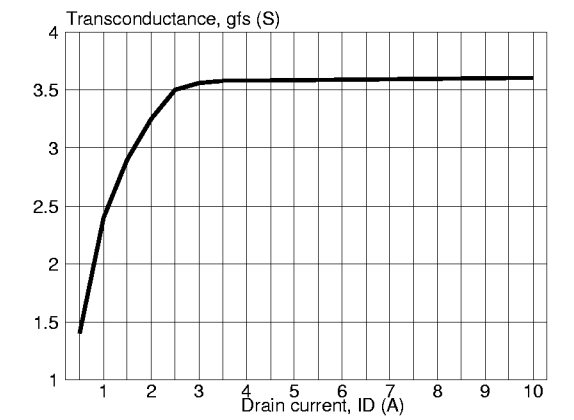



*Fig.8. Typical transconductance, $T_j$ = 25 °C.*
*$g_{fs} = f(I_D)$; conditions: $V_{DS}$ = 25 V*

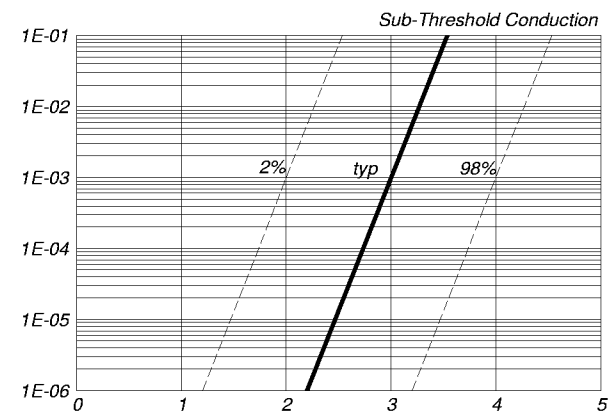



*Fig.11. Sub-threshold drain current.*
*$I_D = f(V_{GS})$; conditions: $T_j$ = 25 °C; $V_{DS} = V_{GS}$*

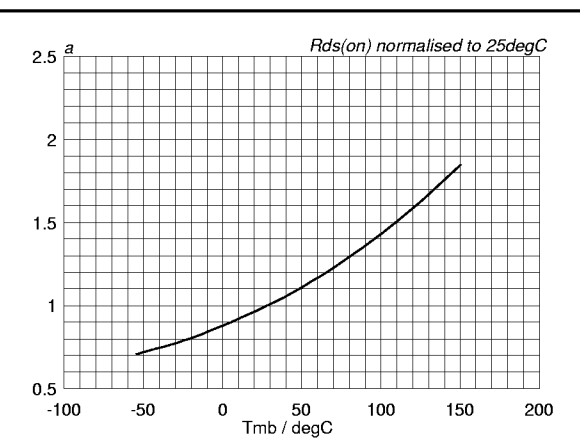



*Fig.9. Normalised drain-source on-state resistance.*
*$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; $I_D$ = 5 A; $V_{GS}$ = 10 V*

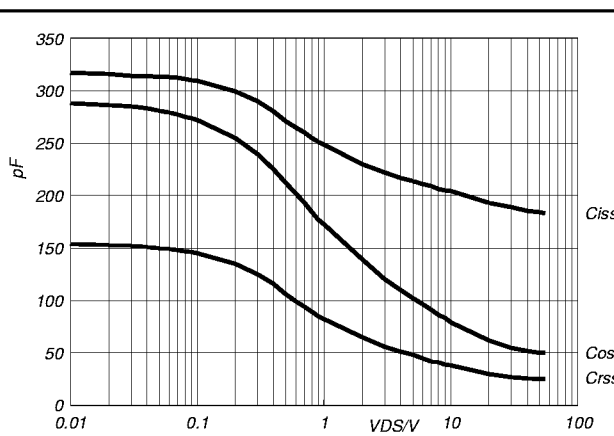



*Fig.12. Typical capacitances, $C_{iss}$, $C_{oss}$, $C_{rss}$.*
*$C = f(V_{DS})$; conditions: $V_{GS}$ = 0 V; f = 1 MHz*

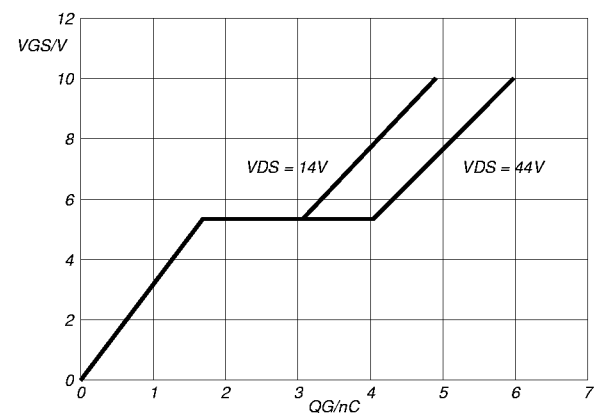



*Fig.13. Typical turn-on gate-charge characteristics.*
*$V_{GS}$ = f($Q_G$); conditions: $I_D$ = 5 A; parameter $V_{DS}$*

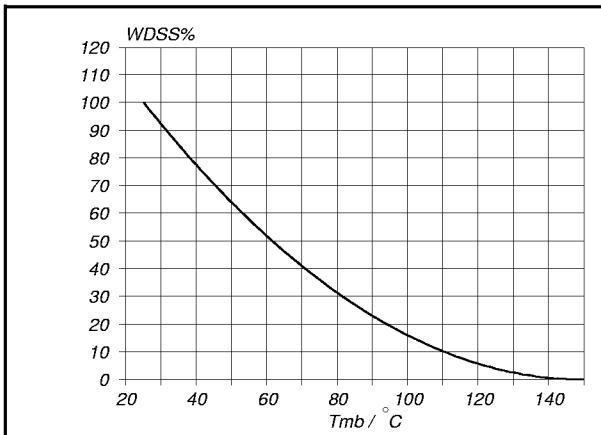



*Fig.15. Normalised avalanche energy rating.*
*$W_{DSS}$% = f($T_{sp}$); conditions: $I_D$ = 1.9 A*

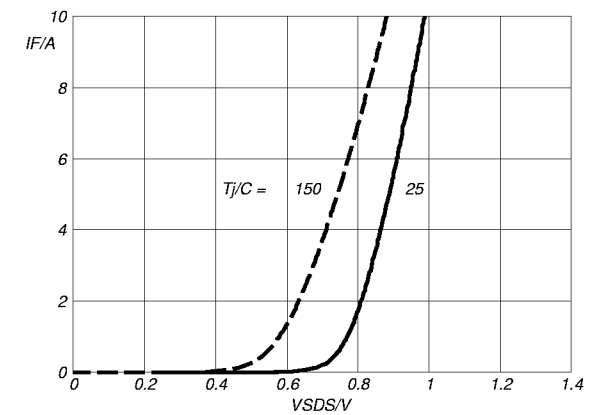



*Fig.14. Typical reverse diode current.*
*$I_F$ = f($V_{SDS}$); conditions: $V_{GS}$ = 0 V; parameter $T_j$*

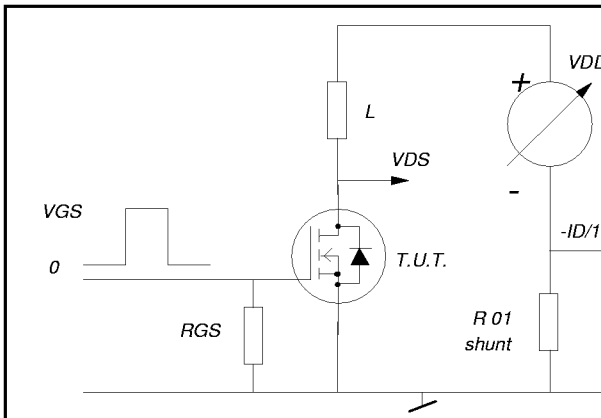



*Fig.16. Avalanche energy test circuit.*

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

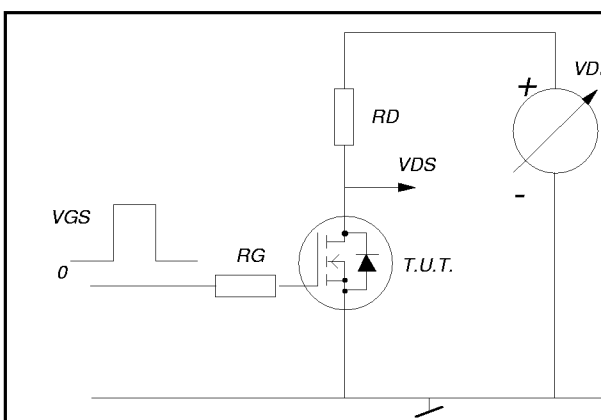



*Fig.17. Switching test circuit.*

## MECHANICAL DATA

*Dimensions in mm*

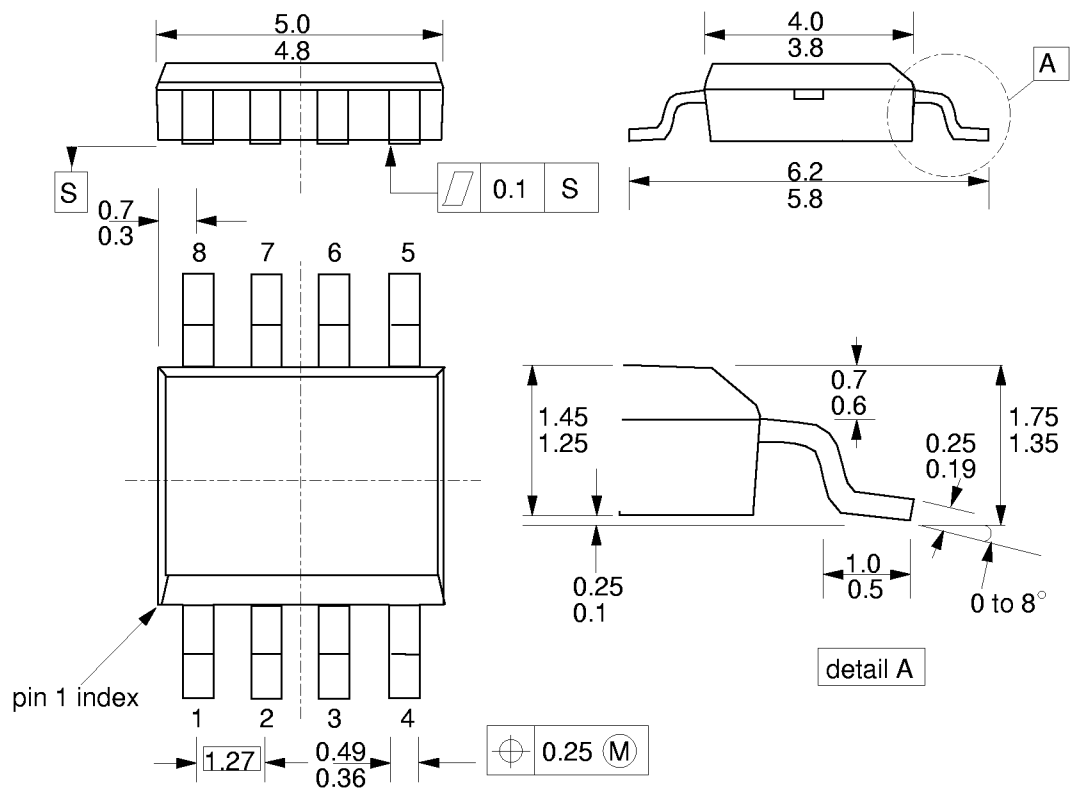



*Fig.18. SOT96 (SO8).*

**Notes**

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".