National Semiconductor

2900 Family/
Bipolar Microprocessor

IDM2909A/11A
Microprogram Sequencer

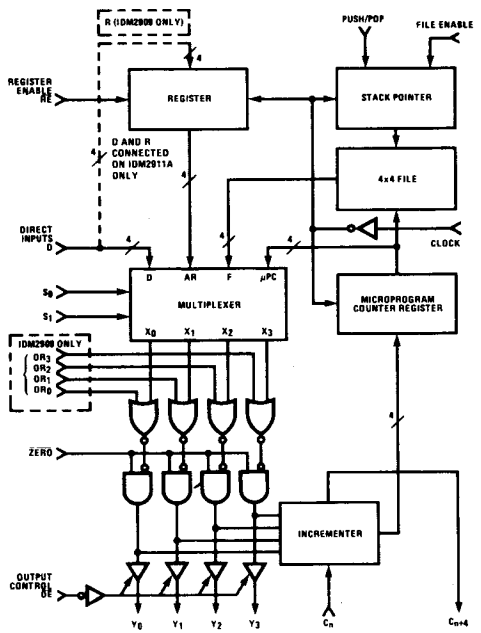
General Description

The IDM2909A is a 4-bit wide address controller that is used to sequence through a series of microinstructions contained in ROM or PROM. Two devices can be interconnected to generate an 8-bit address (256 words), three devices for a 12-bit address (4k words), and so on. For a given device, the 4-bit address field can originate from any one of four sources. These are: (1) direct "D" inputs from an external source, (2) external data from an internal register "R," (3) a push/pop stack that is 4 words deep, and (4) a program counter, which usually contains the last address incremented by "1." Control of the push/pop stack is such that the stack can efficiently execute nested subroutine linkages. Moreover, each of the four TRI-STATE outputs can be ORed with an external input to implement conditional skips or branch instructions; a separate line is used to force the outputs to an "all-zero" state. As shown in the block diagram, the IDM2911A is identical to the IDM2909A, except the four OR inputs are removed and the "D" and "R" inputs are connected. The IDM2909A is housed in a 28-pin dual-in-line package, whereas the IDM2911A is a 20-pin device.

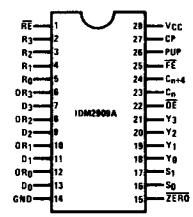
Features and Benefits

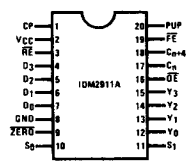
- 4-bit cascadable slice — any number of microwords can be generated.
- Internal address register — provides four address sources.
- Branch input for N-way branches — where "N" is any word in the microcode.
- Cascadable 4-bit microprogram counter.
- 4x4 file with stack pointer and push/pop control — four microsubroutines can be nested.
- Zero input for returning to microcode word "zero."
- Individual OR input for each bit to branch to higher microinstruction (IDM2909A only).
- TRI-STATE outputs.
- All internal registers change state on Low-to-High transition of clock pulse.

Simplified Block Diagram



Connection Diagrams





Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +7.0V
DC Output Current into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Operating Range

P/N	Ambient Temperature	V_{CC}
IDM2909ANC, JC	0°C to +70°C	4.75V to 5.25V
IDM2911ANC, JC	0°C to +70°C	4.75V to 5.25V
IDM2909AJM, JM/883	−55°C to +125°C	4.50V to 5.50V
IDM2911AJM, JM/883	−55°C to +125°C	4.50V to 5.50V

Electrical Characteristics

Commercial T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V

Military T_A = −55°C to +125°C, V_{CC} = 4.50V to 5.50V

Parameter	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output High Voltage	V_{CC} = min, V_{IN} = V_{IH} or V_{IL}	Mil	I_{OH} = −1.0mA	2.4			V
			Com'l	I_{OH} = −2.6mA	2.4			
V_{OL}	Output Low Voltage	V_{CC} = min, V_{IN} = V_{IH} or V_{IL}		I_{OL} = 4.0mA			0.4	V
				I_{OL} = 8.0mA			0.45	
				I_{OL} = 16mA (Note 5)			0.5	
V_{IH}	Input High Level	Guaranteed input logical high voltage for all inputs			2.0			V
V_{IL}	Input Low Level	Guaranteed input logical low voltage for all inputs					0.8	V
V_I	Input Clamp Voltage	V_{CC} = min, I_{IN} = −18mA					−1.5	V
I_{IL}	Input Low Current	V_{CC} = max, V_{IN} = 0.4V					−0.36	mA
I_{IH}	Input High Current	V_{CC} = max, V_{IN} = 2.7V					20	μA
I_I	Input High Current	V_{CC} = max, V_{IN} = 7.0V					0.1	mA
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = max			−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = max (Note 4)				80	130	mA
I_{OZL}	Output Off Current	V_{CC} = max, $\overline{OE}$ = 2.7V		V_{OUT} = 0.4V			−20	μA
I_{OZH}				V_{OUT} = 2.7V			20	

Notes:

1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Apply GND to C_n, R_0, R_1, R_2, R_3, OR_0, OR_1, OR_2, OR_3, D_0, D_1, D_2, and D_3. Other inputs open. All outputs open. Measured after a LOW-to-HIGH clock transition.
5. The 16mA guarantee applies only to Y_0, Y_1, Y_2, and Y_3.

Standard Screening (Conforms to MIL-STD-883 for Class C Parts)

Step	MIL-STD-883 Method	Conditions	Level	
			IDM2909A/2911A NC, JC	IDM2909A/2911A JM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C 24-hour, 150°C	100%	100%
Temperature Cycle	1010	C −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B 10,000 G	100%*	100%
Fine Leak	1014	A 5×10^{-8} atm-cc/cm^3	100%*	100%
Gross Leak	1014	C Fluorocarbon	100%*	100%
Electrical Test Subgroups 1, 7, and 9	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B Parts				
Group A Sample Tests	5005	See below for definitions of subgroups		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 5
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 5

*Not applicable to IDM2909ANC or IDM2911ANC.

Group A Subgroups
(as defined in MIL-STD-883, Method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum Rated Temperature
3	DC	Minimum Rated Temperature
7	Function	25°C
8	Function	Maximum and Minimum Rated Temperature
9	Switching	25°C
10	Switching	Maximum Rated Temperature
11	Switching	Minimum Rated Temperature

Additional Screening for Class B Parts

Step	MIL-STD-883 Method	Conditions	Level
			IDM2909A/11A JM/883
Burn-In	1015	D 125°C 160 hours min.	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

Switching Characteristics Over Operating Range

All parameters are guaranteed worst case over the operating voltage and temperature range for the device type.

IDM2909A/11A JC, NC $T_A = 0°C$ to $+70°C$ $V_{CC} = 4.75V$ to $5.25V$

IDM2909A/11A JM, JM/883 $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.5V$ to $5.5V$)

Table 1. Minimum Clock Requirements

Minimum Clock Low Time	30
Minimum Clock High Time	30

Table 2. Maximum Combinatorial Propagation Delays

Inputs	Outputs	
	Y_i	C_{n+4}
$\overline{OE}$	25	–
$\overline{ZERO}$	30	35
OR_i	20	30
S_0, S_1	30	35
D_i	20	30
C_n	–	18

Table 3. Maximum Delays from Clock to Outputs

Functional Path	Grade	Clock to Y_i	Clock to C_{n+4}
Register ($S_1 S_0$ = LH)	C	40	45
	M	50	55
μ Program Counter ($S_1 S_0$ = LL)	C	40	45
	M	50	55
File ($S_1 S_0$ = HL)	C	45	50
	M	55	60

$C_L \leq 50pF$
(except output disable tests)

Table 4. Setup and Hold Time Requirements

External Inputs	t_s	t_h
$\overline{RE}$	20	0
R_i	15	0
PUSH/POP	20	0
$\overline{FE}$	20	0
C_n	15	0
D_i	20	0
OR_i	20	0
S_0, S_1	30	0
$\overline{ZERO}$	30	0

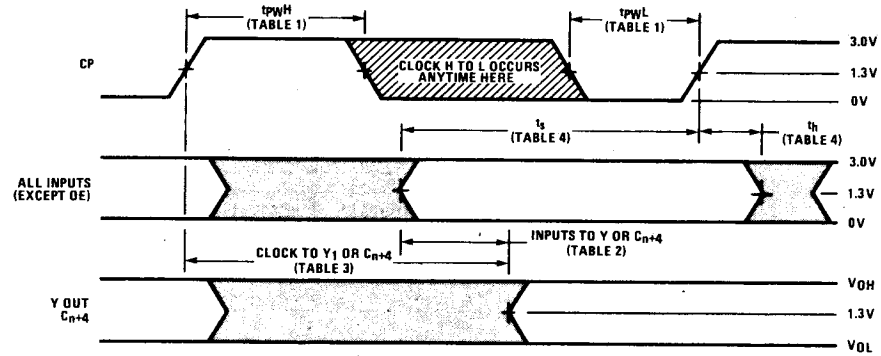


Figure 1. Switching Waveforms (refer to preceding tables for specific values)

Architecture of Microprogram Sequencer

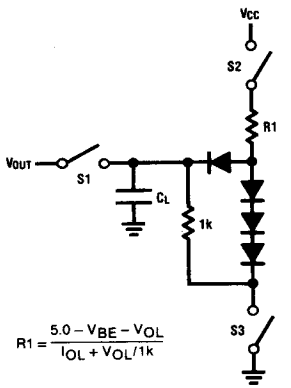
A 4-input multiplexer selects one of four sources for the address of the next microinstruction address; these sources are: the address register, the microprogram counter, direct inputs, and the memory file. The multiplexer is controlled by the S_0/S_1 inputs. As shown in figure 2, the address register consists of four D-type edge-triggered flip-flops with a common clock enable. When the REGISTER ENABLE signal is low, new data is entered on the low-to-high transition of the clock. The "Q" outputs of the address register are available at the input of the multiplexer as a source for the next microinstruction address. The direct inputs (D_0-D_3) can likewise be selected as an address input to the multiplexer.

Both the IDM2909A and the IDM2911A are bipolar microprogram sequencers designed for use in high-speed microprocessors, high-performance computer control units, and other applications where overlap fetch of the microinstruction is required. Each device is cascadable in 4-bit increments such that two devices can address up to 256 words of microprogram memory, three devices up to 4k of memory, and so on. A detailed block diagram of the microprogram sequencer is shown in figure 2.

In the IDM2911A, the 4-bit direct field is also used as an input to the address register, that is, R_0 and D_0 are connected, R_1 and D_1 are connected, and so on. With the "R" and "D" connections made and the OR inputs removed, the IDM2911A can perform an N-way branch, where "N" is any word in the microcode.

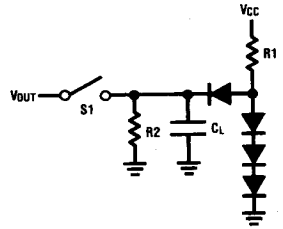
Test Output Load Configurations for IDM2909A/2911A

A. Three-State Outputs



$$R1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1k}$$

B. Normal Outputs



$$R2 = \frac{2.4V}{I_{OH}}$$

$$R1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R2}$$

Note 1: $C_L = 50$ pF includes scope probe, wiring and stray capacitances without device in test fixture.

Note 2: S1, S2, S3 are closed during function tests and all AC tests except output enable tests.

Note 3: S1 and S3 are closed while S2 is open for t_{PZH} test.
S1 and S2 are closed while S3 is open for t_{PZL} test.

Note 4: $C_L = 5.0$ pF for output disable tests.

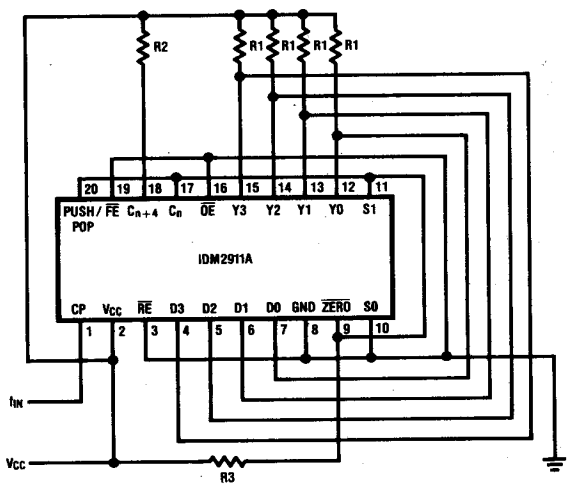
Test Output Loads

Pin # (DIP)	Pin Label	Test Circuit	IDM2909		IDM2909A	
			R1	R2	R1	R2
18-21	Y_{0-3}	A	300	1k	220	1k
24	C_{n+4}	B	470	2.4k	220	2.4k

Pin # (DIP)	Pin Label	Test Circuit	IDM2911		IDM2911A	
			R1	R2	R1	R2
12-15	Y_{0-3}	A	300	1k	220	1k
18	C_{n+4}	B	470	2.4k	220	2.4k

Burn-in Circuit for IDM2911A

Notes:
Max $I_{CC} = 200$ mA
$T_A = +125°C$
Resistors = ±5%
R1 = 390Ω
R2 = 560Ω
R3 = 1 kΩ
$f_{IN} = 100$ kHz, 50% duty cycle, 0V-3V
From clock buffer on each board:
V_{CC} min = 5.0V
V_{CC} max = 5.1V



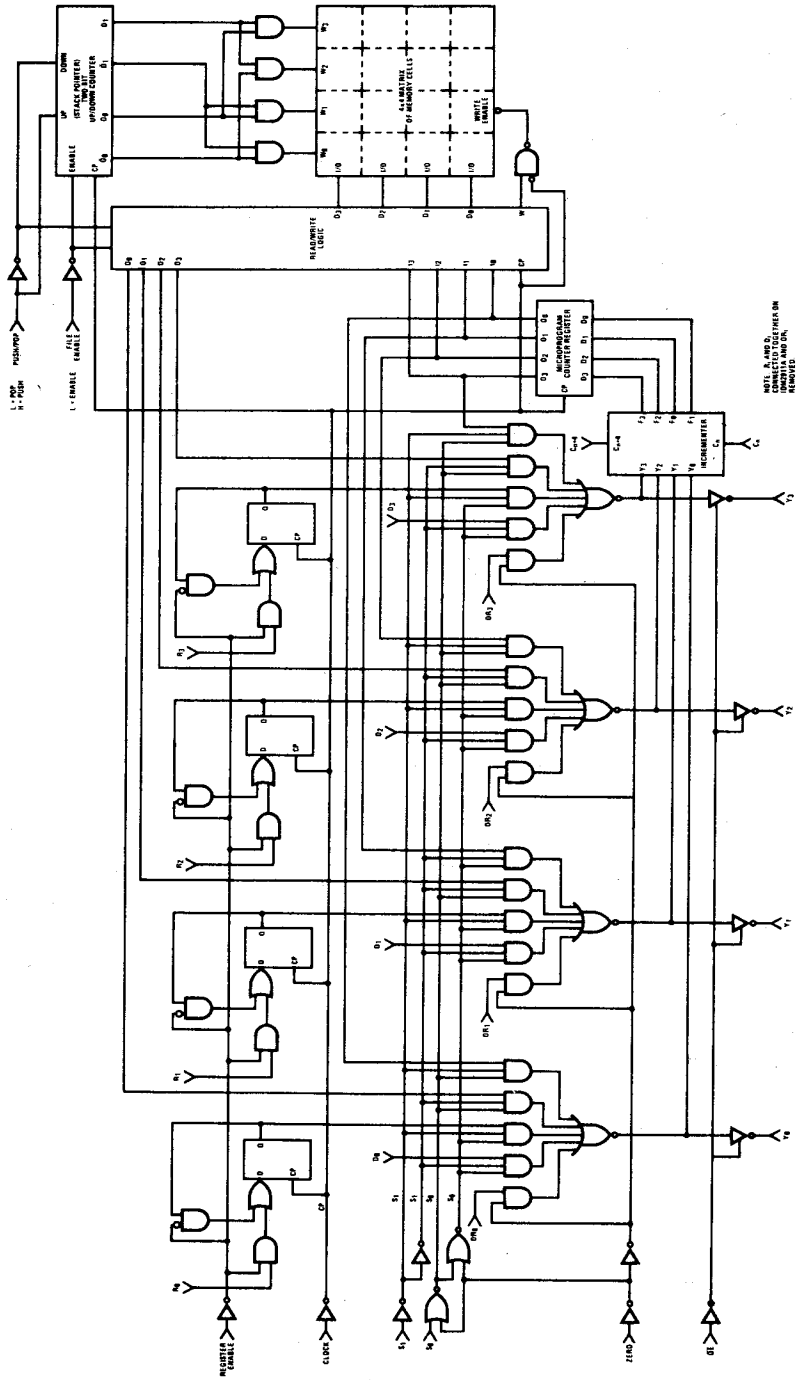


Figure 2. Microprogram Sequencer - Detailed Block Diagram

The microprogram counter consists of a 4-bit incrementer followed by a 4-bit register. The carry-in (C_n) and carry-out (C_{n+4}) features of the incrementer make cascading to larger word lengths easy and straightforward. The microprogram counter can be used in either of two ways. When the least significant bit of C_n is high, the microprogram register (μPC) is loaded on the next clock cycle with the current output word (Y_0-Y_3) plus 1, that is, $Y + 1 \rightarrow \mu PC$; thus, sequential microinstructions are executed. When C_n is low, the "Y" outputs are not incremented; accordingly, the same microinstruction can be repeatedly executed. The last address source available at the input of the multiplexer is the 4-bit/4-word stack file; when executing subroutines, the file provides return address linkage. The 4-by-4 memory matrix contains a stack pointer (SP) that always points to the last word written in the file; thus, stack reference operations (looping) can be performed without a push or pop. The stack pointer operates as an up/down counter with separate PUSH/POP and FILE ENABLE inputs. When the enable signal is low and the other signal is high, the "push" operation is enabled. Under these conditions, the stack pointer is incremented and the file is written with the required return linkage, that is, the next microinstruction address following the subroutine jump that initiated the "push." If both input signals (PUSH/POP and FILE ENABLE) are low, a "pop" operation is implemented. During this clock cycle, the return linkage is used to return from the subroutine; the next low-to-high transition of the clock pulse decrements the stack pointer.

When the FILE ENABLE signal is high, the stack pointer is not incremented or decremented, regardless of whether the PUSH/POP signal is high or low. Linkage of the stack pointer is such that any combination of pushes, pops, or stack references can be implemented; one microinstruction subroutine can be performed. Since the stack is 4 words deep, up to four microsubroutines can be nested. The ZERO input is used to force all four outputs (Y_0-Y_3) of the multiplexer to the zero (logic 0) state. When the zero input is low, all Y-outputs are low, unless overridden by the OUTPUT ENABLE ($\overline{OE}$) signal. Also, each bit of the Y-output word can be ORed at the input such that conditional logic can be enforced; this allows execution of microinstructions to occur in any programmed sequence.

Definition of Terms and Symbols (Figure 2)

Inputs to IDM2909A/11A:

S_0/S_1	Control lines for address-source selection
$\overline{FE}$/PUP	Control lines for push/pop stack
$\overline{RE}$	Enable signal for internal address register
OR_i	Logic OR input for each address output line
$\overline{ZERO}$	Logic AND input for all output lines
$\overline{OE}$	Output Enable; when $\overline{OE}$ is high, the Y-outputs are TRI-STATE (high impedance)
C_n	Carry-in to incrementer
R_i	Inputs to the internal address register
D_i	Direct inputs to the multiplexer
CP	Clock inputs

Outputs from the IDM2909A/11A:

Y_i	Address outputs; address inputs to control memory
C_{n+4}	Carry-out from the incrementer
μPC	Contents of the microprogram counter
REG	Contents of the internal register
STK0/STK3	Contents of the push/pop stack. By definition, the word addressed by the stack pointer in the 4-by-4 file is STK0. Data is pushed onto the stack at STK0 and is subsequently pushed to STK1, STK2, and finally to STK3. When the stack is popped, data is removed in the following order: STK3 → STK2 → STK1, and then to STK0. When a push or pop occurs, only the stack pointer changes — the data is not physically shifted within the stack.
SP	Contents of the stack pointer

Terms and symbols external to the IDM2909A/11A:

A	Control memory address
I(A)	Instruction in control memory at address "A"
μWR	Contents of microword register at output of control memory; this register contains the instruction currently being executed
T_n	Period of timing cycle

Operation of the IDM2909A/11A

Select codes for the multiplexer and the truth tables for output control/stack control are shown in figure 3. The two bits (S_0/S_1) from the microword register (plus additional branching logic) determine the data source for the next microinstruction address. The selected data source appears on the Y-outputs of the multiplexer.

A state table for S_0, S_1, $\overline{FE}$, and PUP is shown in figure 4; these signals define not only the address specified by the Y-outputs, but also the state of all internal registers, following the low-to-high transition of the clock pulse. In figure 4, it is assumed that the microprogram counter initially contains some word "J," word "K" is in the address register, and words R_a through R_d are contained in the 4-word push/pop stack.

The sequence for executing a subroutine using the IDM2909A is illustrated in figure 5. For any given clock cycle, the instruction being executed is contained in the microword register (μWR); the contents of this register also directly (or indirectly) control S_0, S_1, $\overline{FE}$, and PUP. At the appropriate time, the starting address of the subroutine is applied to the "D" inputs of the sequencer. The three left-hand columns of figure 5 show the execution sequence of the instructions and the designated execution cycles. At address "J+2," the sequence-control part of the microinstruction contains the command "Jump To Subroutine A." At time t_2, the "J+2" instruction resides in the μWR and the inputs of the sequencer are set up to execute the "jump," and to save the return address. Address bits for subroutine "A" are taken from the microword register and applied to the D-inputs of the multiplexer; the output appears at the Y-port of the multiplexer.

Address Selection

Octal	S_1	S_0	Source for Y Outputs	Symbol
0	L	L	Microprogram Counter	μPC
1	L	H	Register	REG
2	H	L	Push-Pop Stack	STK0
3	H	H	Direct Inputs	D_i

Output Control

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0S_1

Z = High Impedance

Synchronous Stack Control

$\overline{FE}$	PUP	Push-Pop Stack Change
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't Care

Figure 3. Truth Tables for Multiplexer Control Signals

Cycle	$S_1, S_0, \overline{FE}$, PUP	μPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	Comment	Principal Use
N N+1	0 0 0 0 –	J J+1	K K	R_a R_b	R_b R_c	R_c R_d	R_d R_a	J –	Pop Stack	End Loop
N N+1	0 0 0 1 –	J J+1	K K	R_a J	R_b R_a	R_c R_b	R_d R_c	J –	Push μPC	Set Up Loop
N N+1	0 0 1 X –	J J+1	K K	R_a R_a	R_b R_b	R_c R_c	R_d R_d	J –	Continue	Continue
N N+1	0 1 0 0 –	J K+1	K K	R_a R_b	R_b R_c	R_c R_d	R_d R_a	K –	Pop Stack; Use AR for Address	End Loop
N N+1	0 1 0 1 –	J K+1	K K	R_a J	R_b R_a	R_c R_b	R_d R_c	K –	Push μPC; Jump to Address in AR	JSR AR
N N+1	0 1 1 X –	J K+1	K K	R_a R_a	R_b R_b	R_c R_c	R_d R_d	K –	Jump to Address in AR	JMP AR
N N+1	1 0 0 0 –	J R_a+1	K K	R_a R_b	R_b R_c	R_c R_d	R_d R_a	R_a –	Jump to Address in STK0; Pop Stack	RTS
N N+1	1 0 0 1 –	J R_a+1	K K	R_a J	R_b R_a	R_c R_b	R_d R_c	R_a –	Jump to Address in STK0; Push μPC	
N N+1	1 0 1 X –	J R_a+1	K K	R_a R_a	R_b R_b	R_c R_c	R_d R_d	R_a –	Jump to Address in STK0	Stack Ref (Loop)
N N+1	1 1 0 0 –	J D+1	K K	R_a R_b	R_b R_c	R_c R_d	R_d R_a	D –	Pop Stack; Jump to Address on D	End Loop
N N+1	1 1 0 1 –	J D+1	K K	R_a J	R_b R_a	R_c R_b	R_d R_c	D –	Jump to Address on D; Push μPC	JSR D
N N+1	1 1 1 X –	J D+1	K K	R_a R_a	R_b R_b	R_c R_c	R_d R_d	D –	Jump to Address on D	JMP D

X = Don't Care, 0 = Low, 1 = High, Assume C_n = High
Note: STK0 is the location addressed by the stack pointer.

Figure 4. Output and Internal Next-Cycle Register States for IDM2909A/11A

Control Memory

Execute Cycle	Microprogram	
	Address	Sequencer Instruction
	J–1	–
t_0	J	–
t_1	J+1	–
t_2	J+2	JSR A
t_6	J+3	–
t_7	J+4	–
	–	–
	–	–
	–	–
	–	–
	–	–
t_3	A	I(A)
t_4	A+1	–
t_5	A+2	RTS
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–

Execute Cycle		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9
Clock											
Signals											
IDM2909A Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	J+4	J+5		
	STK0	–	–	–	J+3	J+3	J+3	–	–		
	STK1	–	–	–	–	–	–	–	–		
	STK2	–	–	–	–	–	–	–	–		
	STK3	–	–	–	–	–	–	–	–		
IDM2909A Output	Y	J+1	J+2	A	A+1	A+2	J+3	J+4	J+5		
ROM Output	(Y)	I(J+1)	JSR A	I(A)	I(A+1)	RTS	I(J+3)	I(J+4)	I(J+5)		
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	JSR A	I(A)	I(A+1)	RTS	I(J+3)	I(J+4)		

C_n = High

Figure 5. Execution of Subroutine

Subsequently, the first instruction "I(A)" of the subroutine is accessed and input to μWR. On the next low-to-high transition of the clock, I(A) is loaded into μWR for execution and the return address (J+3) is pushed onto the stack. At t_5, the return instruction is executed. Figure 6 shows a similar instruction sequence where one subroutine is linked to another — the second subroutine consists of only one microinstruction.

Control Memory

Execute Cycle	Microprogram	
	Address	Sequencer Instruction
	J–1	–
t_0	J	–
t_1	J+1	–
t_2	J+2	JSR A
t_9	J+3	–
	–	–
	–	–
	–	–
	–	–
t_3	A	–
t_4	A+1	–
t_5	A+2	JSR B
t_7	A+3	–
t_8	A+4	RTS
	–	–
	–	–
	–	–
	–	–
t_6	B	RTS
	–	–
	–	–

Execute Cycle		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9
Clock											
Signals											
IDM2909A Inputs (from μWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	B+1	A+4	A+5	J+4
	STK0	–	–	–	J+3	J+3	J+3	A+3	J+3	J+3	–
	STK1	–	–	–	–	–	–	J+3	–	–	–
	STK2	–	–	–	–	–	–	–	–	–	–
	STK3	–	–	–	–	–	–	–	–	–	–
IDM2909A Output	Y	J+1	J+2	A	A+1	A+2	B	A+3	A+4	J+3	J+4
ROM Output	(Y)	I(J+1)	JSR A	I(A)	I(A+1)	JSR B	RTS	I(A+3)	RTS	I(J+3)	I(J+4)
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	JSR A	I(A)	I(A+1)	JSR B	RTS	I(A+3)	RTS	I(J+3)

C_n = High

Figure 6. Two Nested Subroutines

Applications Example

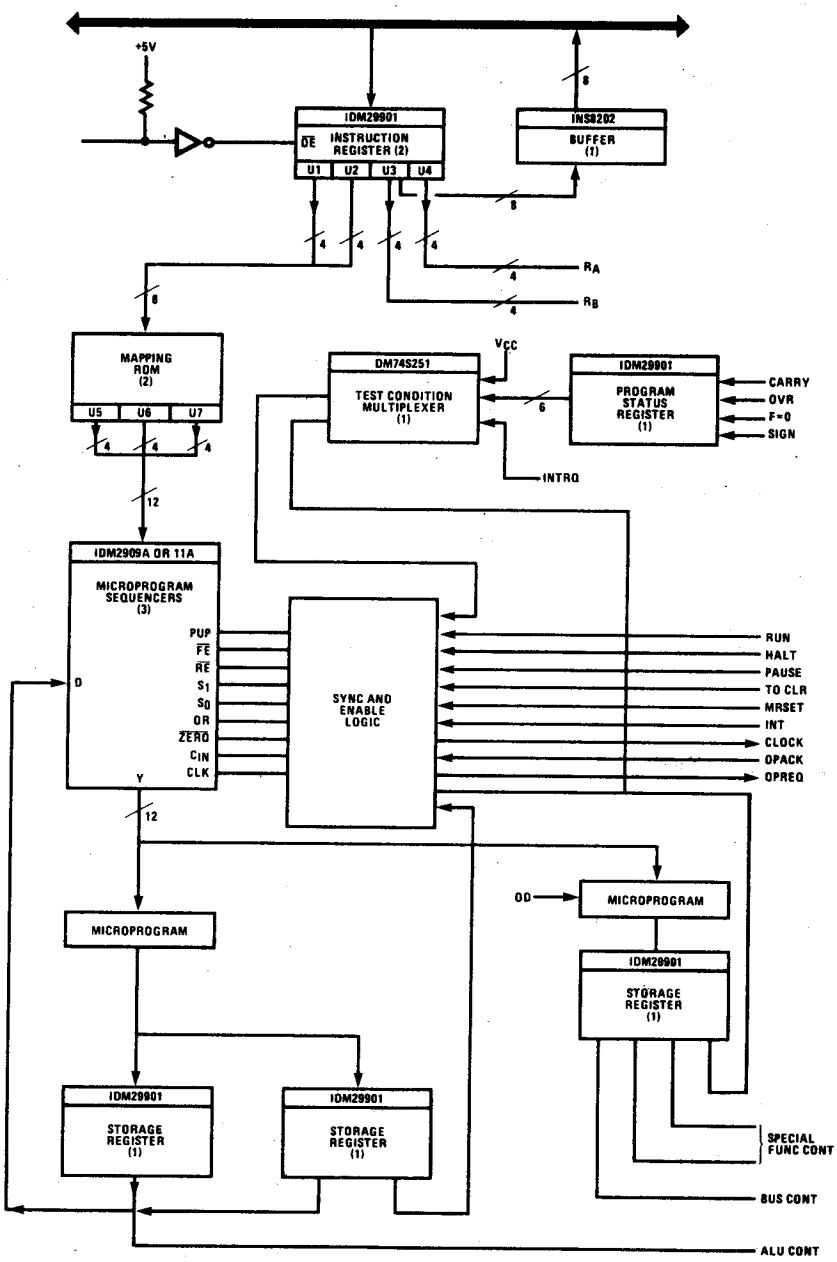


Figure 7. Typical Use of an IDM2909A as a Microprogram Sequencer in a Computer Control Unit