Data Sheet
June 4, 1993

AT&T Microelectronics

AT&T HSM192xD Data Pump Chip Sets

(19,200 bits/s Data/FAX, Parallel Data Mode, ROM Code MJ)

Introduction

The AT&T HSM192xD Data Pump Chip Sets feature new V.32terbo 19,200 bits/s and 16,800 bits/s data and FAX modes, as well as V.32bis and lower-speed modes. These chip sets allow modem designers to build high-speed, fully-featured data/FAX modems with minimal design effort. The HSM192xD Data Pump Chip Sets are high-performance, 2-wire, full-duplex (FDX) modems that operate over either the general switched telephone network (GSTN) or leased lines with the appropriate line terminations.

In addition to the V.32terbo standard, the data pumps conform to CCITT recommendations V.32bis, V.32, V.22bis, V.22, V.23, V.21 and are compatible with the Bell 212A and 103 modems for data mode operation. For FAX operation, the data pumps support Group 3 FAX modulation standards V.17, V.29, V.27ter, and V.21 Channel 2, in addition to the V.17terbo standard. Transmission rates of 300 bits/s to 19,200 bits/s are supported. (See complete list of supported modes at right.)

A key feature in this data pump is a parallel data transfer mode that allows the host controller to pass data directly to/from the data pump without the need for an external USART. When using this feature, the data pump performs all USART functions internally.

The HSM192xD data pumps consist of a ROM-coded DSP16A Digital Signal Processor, an interface device (V32-INTFC), and an AT&T T7525 Linear Codec. Three packaging options are available for applications ranging from PCMCIA card modems to external desktop modems. For ultra-low power applications, versions of the data pumps that operate at 3.3 V are available. The 3.3 V data pumps use an AT&T CSP1027 Linear Codec in place of the T7525 codec.

Features

- Data mode compatibilities:
  - — V.32terbo: 19,200 (TCM), 16,800 (TCM)
  - — CCITT V.32bis: 14,400 (TCM), 12,000 (TCM), 7200 (TCM)
  - — CCITT V.32: 9600 (TCM), 9600 (QAM), 4800 (QAM)
  - — CCITT V.22bis: 2400 (QAM), 1200 (DPSK)
  - — CCITT V.22: 1200 (DPSK), 600 (DPSK)
  - — CCITT V.23: 1200 (FSK), 600 (FSK)
  - — CCITT V.21: 300 (FSK)
  - — Bell 212A: 1200 (DPSK)
  - — Bell 103: 300 (FSK)
- FAX mode compatibilities:
  - — V.17terbo: 19,200 (TCM), 16,800 (TCM)
  - — CCITT V.17: 14,400 (TCM), 12,000 (TCM), 7200 (TCM)
  - — CCITT V.29: 9600 (QAM), 7200 (QAM)
  - — CCITT V.27ter: 4800 (DPSK), 2400 (DPSK)
  - — CCITT V.21 Channel 2: 300 (FSK)
- Non-linear encoding in V.32terbo modes that improves performance over PCM channels and in the presence of harmonic distortion
- Parallel data transfer mode allows operation without the need for an external USART
- Low power consumption (HSM192LD version):
  - — Sleep mode power consumption: 50 mW
  - — Typical active power consumption: 450 mW
- Full-duplex asynchronous inband secondary channel (typically 150 bits/s)
- Voice-thru mode for applications such as PC-based answering machines
- Caller ID receiver designed for actual caller ID signaling frequencies (not V.23 frequencies)
- Transmit and receive baud clocks to support multiplexer applications
- Carrier loss detection for V.32bis and V.32 modes
- Small footprint, surface-mount packaging
- No external RAM or ROM required
- Single 5 V supply (3.3 V versions also available)

User Information

The AT&T HSM192xD Data Pump Chip Sets work with a host microprocessor or other data terminal equipment and a line interface to implement a full duplex modem. Figure MJ-1 shows a block diagram of a system using the chip set. There are many modulation modes (Table MJ-1) that can be selected. The data pump hardware and software configurations can be customized to your particular application. The host microprocessor selects the data pump hardware configuration through the data pump register set. The host controls the software functionality using a simple command set. The register set and command set are presented in subsequent sections.

Hardware Overview

The following sections highlight many features of the AT&T HSM192xD data pump chip sets.

Architecture

The AT&T HSM192xD Data Pump consists of a ROM-coded *WE* DSP16A Digital Signal Processor, an interface device (V32-INTFC2), and an AT&T T7525 Linear Codec (see Figure MJ-2). The DSP16A performs the signal processing and control functions needed to implement the specified standards. The T7525 codec is the analog front-end of the data pump (for 3.3V versions of the data pump, an AT&T CSP1027 codec is substituted for the T7525 codec). The interface device provides V.24, microprocessor bus, and constellation pattern interfaces. No external ROM or RAM is required.

Programmable V.24 Interface

The data and clock paths can be customized for particular applications. The data paths can come from the EIA interface or the host, be clamped, be controlled with CTS or RTS, be tied together for remote digital loop (RDL), or contain test sequences. The clocks can be internal, free-running; external, DTE-slaved using a PLL to lock the transmit timing to XTCLK; clamped; or 3-stated. See V.24 Interface Description, page MJ-45.

Powerup Reset

The data pump powers up in the following mode:

- V.32 mode
- Synchronous
- Transmit level is –10 dBm
- Compromise equalizer enabled at 4 dB
- Receive signal threshold level is –43 dBm
- Data path tied to EIA interface
- Interrupts disabled
- Sleep mode disabled
- V.25 answer sequence enabled

The following options are NOT defaults at powerup, but are recommended in typical applications:

- Long echo canceler length. See C/S RAM Location 0x38.
- Far echo frequency offset compensation. See C/S RAM Location 0x38.
- Synchronous to asynchronous conversion and asynchronous to synchronous conversion. See Host Register 0x2c.

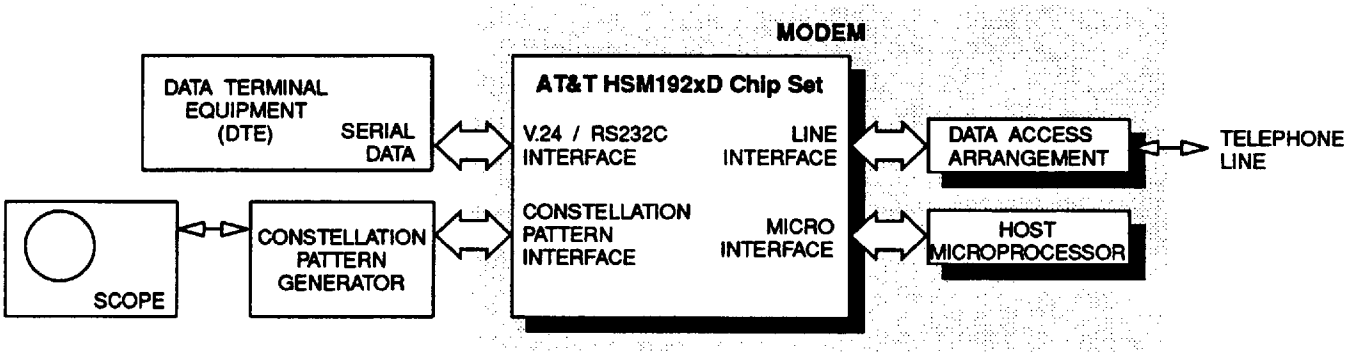


Figure MJ-1. Block Diagram of a Modem Using the AT&T V.32 Chip Set.

User Information (continued)

Sleep Mode

The data pump has the capability to put itself into a low-power mode. When sleep mode is enabled (C/S RAM 0x38), the data pump puts itself into low-power mode after being in idle mode for 4.5 seconds. When in low-power mode, the codec bit clock TCODEC is slowed to 115 kHz, signal TSYNC is disabled, and the sleep mode status bit (register 0x13[7]) is set. The data pump enters idle mode after reset, a disconnect, or "goto idle" command. The data pump automatically wakes up when it receives a ringing signal or a host command. Upon waking up, the codec bit clock is returned to 1.8432 MHz, TSYNC is enabled, the sleep mode status bit (register 0x13[7]) is cleared, and the data pump is ready to accept commands.

Programmable User Clock

The data pump contains a programmable clock that can be used for various system functions; e.g., to drive an external USART. See description of Host Registers 0x12 and 0x13 for more information.

Programmable USART

The data pump provides an internal USART that is used by default for the secondary channel. Alternatively, the USART can be used by the host to inject data into the primary data path to the line or directly to the DTE. The USART contains a two-stage FIFO with the serial channel operating asynchronously. See Programmable USART, page B-1.

External Transmit Timing

The external timing option allows the data pump to be used in leased line synchronous tandem circuit applications. Previous data pumps did not support this application. See External Transmit Timing, page B-6.

Packaging Information

The HSM192xD chip sets are available in the following package options:

- The HSM144DD (DeskTop) version:
  - — DSP16A in 84-pin PLCC
  - — V32-INTFC2 in 68-pin PLCC
  - — T7525 Codec in 28-pin SOJ
- The HSM144LD (LapTop) version:
  - — DSP16A in 84-pin PQFP
  - — V32-INTFC2 in 84-pin PQFP
  - — T7525 in 28-pin SOJ
    (CSP1027 in 44-pin PQFP for 3.3V version)
- The HSM144PD (PCMCIA) version:
  - — DSP16A in 100-pin TQFP
  - — V32-INTFC2 in 100-pin TQFP
  - — T7525 in 28-pin SOTG
    (CSP1027 in 48-pin TQFP for 3.3V version)

The TQFP packages used in the HSM144PD chip set are thin enough to allow two-sided layouts on PCMCIA cards.

Device pin-outs are shown in Appendix A. Package dimension diagrams are shown in Appendix D.

Pin Descriptions

The interface pins for the V.32 chip set are presented in six groups, based on their use:

- Microprocessor Interface
- V.24/EIA-232-D (RS232C) DTE Interface
- Line Interface
- External Data Control Signals
- Constellation Pattern Interface
- Miscellaneous Signals

Appendix A contains complete pin information.

User Information (continued)

Operation Overview

Software Protocol

The data pump contains an easy to use command set which the host controls via the data pump interface device. Commands from the host are sent through the command mailboxes. Data pump responses are read by the host from the response mailboxes. These commands are used to program and control the data pump. (See Host Microprocessor Interface, page MJ-8, and Host Command Set, page MJ-19.)

The host microprocessor also has access to the data pump's Control and Status (C/S) RAM. Many operating parameters are stored in this memory and can be monitored and controlled by the host using specific commands that access this RAM. (See Control and Status RAM, page MJ-28.)

V.32terbo Operation

V.32terbo is a widely-supported modulation standard that extends the V.32bis standard to include two additional data rates, 16,800 bits/s and 19,200 bits/s. V.32terbo modems are compatible with V.32 and V.32bis modems during startup, retrain, and rate renegoatiation. Full duplex extended automode allows automatic rate negotiation at startup between V.32terbo modems and other lower-speed modems.

Table MJ-1. Selectable Configurations

Configuration	Modulation	Sync/ Async	Carrier Frequency (Hz)	Data Rate (bits/s)	Baud (Sym/s)	Bits/Symbol		Constellation Points
						Data	TCM	
V.32terbo 19,200	TCM	Sync/Async	1800	19,200	2400	8	1	512
V.32terbo 16,800	TCM	Sync/Async	1800	16,800	2400	7	1	256
V.32bis 14,400	TCM	Sync/Async	1800	14,400	2400	6	1	128
V.32bis 12,000	TCM	Sync/Async	1800	12,000	2400	5	1	64
V.32bis 7200	TCM	Sync/Async	1800	7200	2400	3	1	16
V.32 9600	TCM	Sync/Async	1800	9600	2400	4	1	32
V.32 9600	QAM	Sync/Async	1800	9600	2400	4	0	16
V.32 4800	QAM	Sync/Async	1800	4800	2400	2	0	4
V.17terbo 19,200	TCM	Sync/Async	1800	19,200	2400	8	1	512
V.17terbo 16,800	TCM	Sync/Async	1800	16,800	2400	7	1	256
V.17 14,400	TCM	Sync/Async	1800	14,400	2400	6	1	128
V.17 12,000	TCM	Sync/Async	1800	12,000	2400	5	1	64
V.17 9600	TCM	Sync/Async	1800	9600	2400	4	1	32
V.17 7200	TCM	Sync/Async	1800	7200	2400	3	1	16
V.29 9600	QAM	Sync/Async	1700	9600	2400	4	0	16
V.29 7200	QAM	Sync/Async	1700	7200	2400	3	0	8
V.27ter 4800	DPSK	Sync/Async	1800	4800	1600	3	0	8
V.27ter 2400	DPSK	Sync/Async	1800	2400	1200	2	0	4
V.22 bis 2400	QAM	Sync/Async	1200/2400	2400	600	4	0	16
V.22 1200	DPSK	Sync/Async	1200/2400	1200	600	2	0	4
V.22 600	DPSK	Sync/Async	1200/2400	600	600	1	0	4
V.23 1200	FSK	Async only	1700/420	1200/75	1200	1	0	—
V.23 600	FSK	Async only	1500/420	600/75	600	1	0	—
V.21 300	FSK	Async only	1080/1750	0—300	300	1	0	—
V.21 Ch. 2 300	FSK	Async only	1750	300	300	1	0	—
Bell 212A	DPSK	Sync/Async	1200/2400	1200	600	2	0	4
Bell 202	FSK	Async only	1700	1200	1200	1	0	—
Bell 103	FSK	Async only	1170/2125	0—300	300	1	0	—

User Information (continued)

Automode Start-up

Automode from V.32 to V.22bis is implemented according to V.32 annex A, and automode to V.23, V.21, Bell103, Bell212A is implemented according to the EIA/TIA draft standard from subcommittee TR-30.1. See C/S RAM Location 0x3b.

Auto-Dialing and Call Progress Control

The functions necessary to perform auto dialing, call progress detection, and auto answering in accordance with North American standards (EIA496A) and CCITT recommendations V.25 bis are provided. The designer must provide a proper telephone line interface and parameter control of the functions included in the data pump to comply fully with these specifications.

These functions include DTMF generation and detection, pulse dialing timing, 3 separate tone generators, 10 separate tone detectors, a programmable ring detector, and two programmable IIR filters. All tones including DTMF are generated within ±1.5%, conforming to Bell System Communications Technical reference publication 47001 dated August 1976. For dialing, programmable duration and interdigit delay are provided. Also, the power level for each tone is programmable. Programmable tone detectors, including DTMF, with adjustable receive threshold level, provide frequency resolution of ±15 Hz and each tone's relative power level. Total in-band energy level is also reported. Programmable make time, break time, and interdigit delay are provided to control pulse dialing.

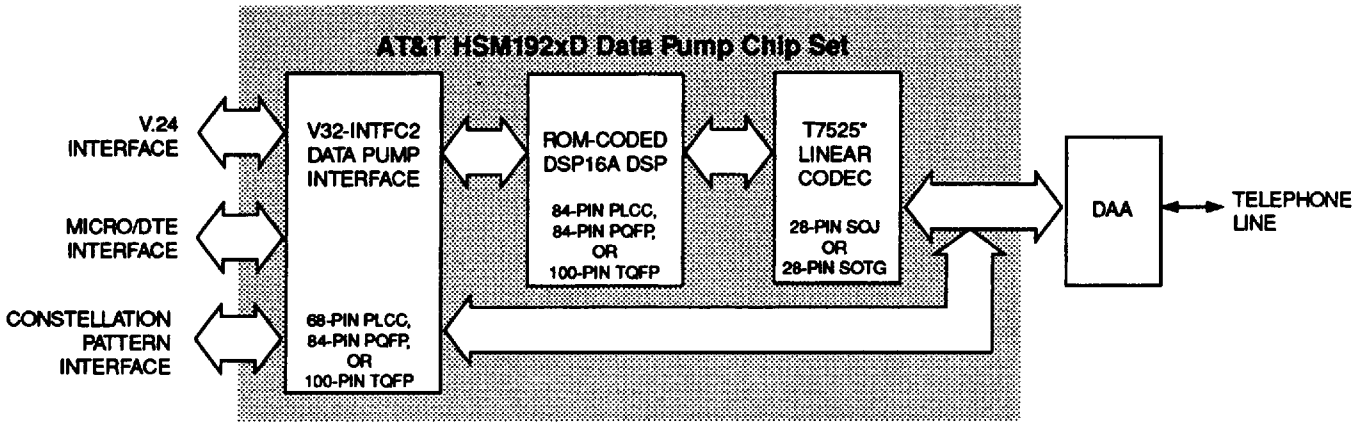
See Control and Status RAM, page MJ-28, for more information on these features.

Ring Detection

The data pump reads the ring detect (RDET) input and controls the ring indication (RI) output. The external ring detect circuit must perform rectification (typically half wave) and voltage detection such that pulses arrive at RDET at the ringing voltage frequency. The data pump performs frequency discrimination and deglitching on the RDET signal so that RI is turned on only when the ringing frequency falls within a user-specified range (C/S RAM locations 0x40 and 0x41).

Programmable IIR Filters

Two programmable 6th order (three 2nd order sections) IIR filters are provided for the host. The host enters the filter coefficients and the minimum energy threshold level for each filter. When the energy of either filter exceeds the minimum energy threshold level set by the host the corresponding bit(s) is set in the operating status word (C/S RAM location 0x3a). At this time, the host can read the actual power level within the band(s) of the filter(s). For a detailed explanation, see Programmable IIR Filters, page B-11.



* In the 3.3 V data pump, the T7525 codec is replaced by a CSP1027 codec in either a 44-pin PQFP or a 48-pin TQFP package.

Figure MJ-2. Block Diagram of the HSM192xD Data Pump

User Information (continued)

Async/Sync, Sync/Async Conversion

Data buffering with basic and extended rates according to CCITT V.14 is provided. Overspeed is automatic on the transmit side and programmable on the receiver side. Transmit and receive character lengths are programmable from 8 to 11 bits. See Host Register 0x2c.

Transmit and Receive Levels

The transmit level is programmable from 0 to –20 dBm with a default value of –10 dBm when measured differentially across codec pins ROP and RON. The receiver has a 40 dB dynamic range. The default range is from –3 dBm to –43 dBm. The receive signal threshold level is programmable from 0 to –45 dBm with a default value of –43 dBm. When the receive signal level drops below this, RD is clamped to marking and RR is forced low (inactive). The receive signal level is the actual value measured at codec pin TGS and is readable at location 0x4a of control and status RAM. See C/S RAM locations 0x03, 0x37, and 0x4a for more information.

Receive Signal Information

Various receive signal information is available to the user. This includes receive signal level, mean square error (mse), and estimates of various channel impairments. See C/S RAM locations 0x4a—0x4d.

Status Information

Extensive data pump status reporting is supported, including modes (dialing, data, etc.), the status of the modem during automode start-up, send and receive data activity, and receive signal parameters.

Echo Canceler

A data driven echo canceler is employed in V.32terbo/V.32bis/V.32 modes. A high-performance AT&T T7525 linear codec allows for a fully digital implementation. Two choices of echo cancelers are provided: 1) a standard version with spans of 8 ms for the near canceler and 10 ms for the far canceler and 2) a longer version with spans of 16 ms for the near canceler and 20 ms for the far canceler. Frequency offset compensation cancels at least 7 Hz of offset and the internal bulk delay line can handle delays as long as 1.2 seconds (600 ms for V.32terbo 19,200 bits/s and 16,800 bits/s modes), with no external RAM or ROM. See C/S RAM locations 0x38 and 0x54—0x56.

Equalizers

An adaptive equalizer is employed in the receiver and a programmable compromise equalizer is employed in the transmitter. The compromise equalizer adjusts the positive slope in the transmit spectrum between 1000 Hz and 2800 Hz. See C/S RAM location 0x04 for more information.

Adaptive Phase Predictor

An advanced adaptive phase predictor is employed to cancel sinusoidal phase jitter with negligible noise enhancement. Up to 3 independent sinusoids with frequencies from 0 to 300 Hz and peak-to-peak phase jitters of 45° or more can be simultaneously canceled.

Remote Digital Loop

The data pump provides support for V.54 remote digital loop (RDL) signaling (referred to as loop 2 by CCITT) and V.22 RDL which is different from V.54. It provides for the generation and detection of all the necessary signals and the host must provide the control logic. For a detailed explanation, see Host Procedures for Implementing Remote Digital Loop, page B-7.

511 Bit Pattern Generator and Detector

The data pump has the capability to generate and receive a 511 pseudorandom bit pattern. An error counter is provided in the detector. See Host Registers 0x23 and 0x2d for more information.

V.32bis Rate Renegotiation

The data pump supports a feature called rate renegotiation that allows two modems that are already connected at a V.32bis rate to quickly switch rates up or down with minimal overhead. Host command 0x2 is used to initiate a V.32bis rate renegotiation. Bit 14 of the operating status word (C/S location 0x3a) indicates that a V.32bis rate renegotiation sequence has been detected.

User Information (continued)

Secondary Channel

The HSM192xD data pump chip set provides a full-duplex, asynchronous, inband, secondary channel that can be used to send and receive diagnostic information without disturbing the primary channel. The secondary channel is available in V.32bis, V.32, V.22bis, and V.22 modes. The channel typically operates at 150 bits/s and causes a minimal increase in the modem's transmit power (approximately 0.2 dB at 150 bits/s). The secondary channel is enabled by setting bit 15 in the options control word (C/S location 0x38).

Voice-Thru Mode

A voice-thru mode is useful for applications such as PC-based answering systems. In this mode, the host passes samples to/from the codec through the data pump. The host can specify 16-bit linear, 8-bit a-law, or 8-bit μ-law data, with the data pump performing any needed conversions. The host can also use the data pump to translate stored data between these same formats in non real-time. Host command 0x17 is used to enter voice-thru mode. For additional information on using this mode, see Using Voice-Thru Mode on page MJ-53.

Transmit and Receive Baud Clocks

Transmit and receive baud clocks are available on pins TBAUD and RBAUD, respectively. These clocks can be used for multiplexer applications. The baud clocks are available for all V.32bis and V.32 rates and for V.22bis 2400 bits/s. The baud rate is 2400 for V.32 and 600 for V.22bis. Regardless of the rate, the clocks are high for one bit period per baud or frame.

Caller ID Receiver

This data pump provides a caller ID receiver function. Caller ID is also referred to as Calling Number Delivery (CND). The data pump's caller ID receiver is designed for the actual signaling frequencies used by the CND service. It is also possible to use V.23 to receive the caller ID signal. However, since V.23 frequencies differ by 100 Hz from those specified for caller ID signaling, using a V.23 receiver provides less than optimal performance.

Caller ID information arrives while the answering equipment is still on-hook, during the silent interval between the first and second ringing pulse. Therefore, the line interface (DAA) must provide a special path from the tip and ring to the analog input (TIN) which can be connected while the modem is on-hook. In addition, a means must be provided to switch TIN between this path and the usual off-hook receive path. The caller ID receive path should be high impedance and capacitively coupled.

On-Line Monitoring

A problem that arises with echo canceling modems is an inability to reliably detect the presence or absence of receive signal energy, due to the behavior of the echo canceler after a disconnect. Thus, the modem may not reliably detect an abrubt termination of a network connection. An echo correlation feature has been added to the data pump to detect this condition. The host controller can use this feature to reliably monitor the presence of the carrier. This feature is active only in V.32 and V.32bis modes.

Host Microprocessor Interface

Communication between the host processor and the data pump is achieved through several means: through directly accessible registers in the V32-INTFC device, through commands and responses exchanged via mailbox registers, and through specific commands that provide access to the DSP's control and status (C/S) RAM. These mechanisms are described in following sections.

The data pump interface device contains a 49-byte address space defined as a host register set (refer to Figure MJ-3). The host processor and the data pump communicate through mailboxes in this register set.

HOST Register Bank (lower bank)			Page
Address	**Mode**	**Description**	
0x00	R/W	UART data register	MJ-9
0x04	W	Command parameter mailboxes	MJ-9
0x05	W		
0x06	W		
0x07	W		
0x08	W		
0x09	W	Command mailbox	MJ-9
0x0A	R	Fast access location mailboxes	MJ-10
0x0B	R		
0x0D	R	Response parameter mailboxes	MJ-10
0x0E	R		
0x0F	R	Response code mailbox	MJ-10
0x12	R/W	User clock register/sleep mode status	MJ-10
0x13	R/W		
0x1E	R	UART Control and Ring indicator register	MJ-11
HOST Register Bank (upper bank)			
0x22	R/W	Clock control register	MJ-11
0x23	R	511 error counter	MJ-11
0x24	R	UART status register	MJ-12
0x25	R	V.54 and V.13 status register	MJ-12
0x28	R/W	Send data, UART, and EIA data set ready control bits	MJ-12
0x29	R/W	V.24 receive data, clear to send, and receiver ready control bits	MJ-13
0x2A	R/W	V.24 send and receive timing control bits	MJ-14
0x2B	R/W	V.24: CTS, DTR, DSR, and RR control and status bits	MJ-14
0x2C	W	Asynchronous control register	MJ-15
0x2D	R/W	V.54, V.13, and 511 control register	MJ-16
0x2E	R/W	Interrupts: setting, resetting, clearing and polling	MJ-17, MJ-18
0x2F	R/W		
0x30	R		

Notes:

In Rockwell compatibility mode, the lower bank is selected by HCS1N and the upper bank is selected by HCS0N.

Register addresses not listed in this table are reserved and should not be accessed.

Figure MJ-3. Host Register Set Overview

Host Microprocessor Interface (continued)

Host Register Set

This section describes, in detail, the host register set.

Host Register: 0x00. UART Data Register

Add	Mode	7	6	5	4	3	2	1	0
00	*W	←			T2NDCHB[7:0] (2nd channel, byte)				First →
	*R	← Last			R2NDCHB[7:0] (2nd Channel, byte)				→

This register is used to transfer data to/from the internal UART, connected either to the primary data path or the secondary channel. Register R2NDCHB is read by the host, and T2NDCHB is written by the host.

R2NDCHB[7:0] Receive Data Register. Read only. Data is read a byte at a time from a buffered serial to parallel shift register. A read from address 0x0 empties the buffer and updates the status flags. The status bit R2ND_DA (register 0x1e[1] or register 0x24[3]) indicates when valid data is available at the output of the buffer. This bit can be polled or used to generate an interrupt by setting its enable, Rx2ND_IE (register 0x1e, bit 5).

T2NDCHB[7:0] Transmit Data Register. Write only. Data is written a byte at a time to a buffered stage shift register. Before writing its data, the host should verify that the transmit status bits are in the proper state to ensure that the input buffer is empty. If both stages are empty, it takes one bit clock for the data to move from the input stage to the output shift register. T2ND_BE (register 0x1e, bit 0) will be set when both stages of the transmit buffer are empty. This bit can be polled or used to generate a UARTI interrupt by setting the enable, Tx2ND_IE (register 0x1e, bit 2). Separate indicators for the two stages are available in register 0x24.

Host Register: 0x04—0x09. Command Mailboxes, from the Host to the DSP

Add	Mode	7	6	5	4	3	2	1	0
04	W	←			Command parameter 5 mailbox				→
05	W	←			Command parameter 4 mailbox				→
06	W	←			Command parameter 3 mailbox				→
07	W	←			Command parameter 2 mailbox				→
08	W	←			Command parameter 1 mailbox				→
09	W	←			Command mailbox				→

Six bytes.
Write only.

Location 0x9 is a trigger byte: a write by the host causes an interrupt at the data pump; a read by the data pump causes an interrupt at the host, when enabled.

Commands from the host to the data pump are passed in mailbox 0x09. Any required parameters must be written into the parameter mailboxes **before** writing the command.

Host Microprocessor Interface (continued)

Host Register: 0x0a—0x0b. Fast Access Mailbox, from the DSP to the Host

Add	Mode	7	6	5	4	3	2	1	0
0A	R	← Fast access mailbox (low byte) →							
0B	R	← Fast access mailbox (high byte) →							

Two bytes.
Read only.

The contents of the data pump control and status (C/S) RAM location specified by the address contained in C/S RAM location 0x3C are automatically copied to these mailboxes periodically. By default, this is the operating status word (C/S RAM location 0x3a). The update period depends on the current operating mode. See Status Information, page MJ-19, for details.

Host Register: 0x0d—0x0f. Response Mailboxes, from DSP to Host

Add	Mode	7	6	5	4	3	2	1	0
0D	R	← Response parameter (low byte) mailbox →							
0E	R	← Response parameter (high byte) mailbox →							
0F	R	← Response code mailbox →							

Three bytes.
Read only.

Location 0xf is a trigger byte: a write by the data pump causes an interrupt at the host; a read by the host causes an interrupt at the data pump. The response code from the requested command is returned in 0x0f. The requested information is returned in 0x0d and 0x0e. The specific return code and format of the returned value(s) are specified in the Host Command Set table.

Host Register: 0x12—0x13. User Clock Registers

This is a programmable clock that can be used for any purpose. It can be programmed to any value between 619 Hz and 5.068 MHz (average frequency with a resolution of 100 ns) as shown below.

Add	Mode	7	6	5	4	3	2	1	0
12	R/W	← CNMDB[1:0] →		← CNUMB[5:0] →					
13	R/W	SLEEPMODE	← CBDIVB[2:0] →			← CNMDB[5:2] →			

Defaults: register 0x12 = 0x80, register 0x13 = 0x0c.

CNUMB[5:0] Customer bit clock numerator. 64-bit resolution for bit clock. CNUMB[5:0]=Nb–1.

CNMDB[5:0] Customer bit clock numerator minus denominator. CNMDB[5:0]=Nb–Db–1. Seven-bit negative number MSB truncated to six bits.

CBDIVB[2:0] Customer bit clock binary divisor. Binary divisor = Kb = CBDIVB[2:0].

$$f_b = USRCLK = \frac{CKI \cdot Nb}{2^{Kb+3} \cdot Db}\ MHz,\ Nb<Db<65,\ Kb<8,\ CKI=40.5504MHz$$

The default values for these registers specify a frequency of 362,057.1429 Hz.

$CNUMB[5:0] = 0 = N_b–1,\ N_b=1$

$CNUMDB[5:0] = 110010 = N_b–D_b–1 = 1–D_b–1 = –D_b \therefore D_b = 001110 = 14$

$CBDIVB[2:0] = 0 = K_b$

$$f_b = \frac{(40.5504MHz)\cdot(1)}{2^3 \cdot 14} = 362{,}057.1429Hz$$

SLEEPMODE: When active, chip set is in low-power mode.

Host Microprocessor Interface (continued)

Host Register: 0x1e. UART Control and Ring Indicator Register

Add	Mode	7	6	5	4	3	2	1	0
1E	W	X	X	Rx2ND_IE	X	X	Tx2ND_IE	X	X
	R	Rx2ND_IQ	Tx2ND_IQ	RI	RDET	Rx2ND_IE	Tx2ND_IE	R2ND_DA	T2ND_BE

Rx2ND_IE — Receive UART interrupt enable. If the UART has data available (R2ND_DA is active) and this bit is active, a UARTI interrupt (register 0x2e) is generated at the host. This bit is 0 by default (interrupt disabled).

Tx2ND_IE — Transmit UART interrupt enable. If the UART output buffer is empty (T2ND_BE is active) and this bit is active, a UARTI interrupt (register 0x2e) is generated at the host. This bit is 0 by default (interrupt disabled).

Read only bits.

Rx2ND_IQ — Receive UART interrupt request. If R2ND_DA and Rx2ND_IE are active, this bit is active and a UARTI interrupt (register 0x2e) is generated at the host.

Tx2ND_IQ — Transmit UART interrupt request. If T2ND_BE and Tx2ND_IE are active, this bit is active and a UARTI interrupt (register 0x2e) is generated at the host.

RI — Ring indicator. This bit is the inverse of the RIN output pin.

RDET — Ring detect. Shows state of RDETN input pin.

R2ND_DA — Receive UART data available. Flag indicating data is available at UART receive FIFO.

T2ND_BE — Transmit UART buffers are empty. Flag indicating both transmit stages of the UART are empty.

Host Register: 0x22. Clock Control Register

Add	Mode	7	6	5	4	3	2	1	0
22	R/W	TSLAV[1:0]		RESERVED					XTCLK

Default: 0x50

When writing to this register, perform a read/modify/write operation, preserving the state of all bits that are not being changed.

TSLAV[1:0] — Transmit slave mode.
00 – Free running.
10 – DTE slaved, PLL to XTCLK is enabled onto transmit timing.

XTCLK — XTCLK signal level.
0 – Non-inverted (default).
1 – Inverted.

Host Register: 0x23. 511 Error Counter

Add	Mode	7	6	5	4	3	2	1	0
23	R	ERR511B[7:0], self-clearing							

Enable 511 bit pattern search by setting register 0x2d[4] to 1. When 511SYNC bit (0x25[5]) is active-low, data in this register is valid. **Note:** bits 0x2d[2:1] are used to enable 511 bit pattern transmit sequence.

ERR511B[7:0] — 511 error counter. Eight bit value that is self cleared after every read by the host.

Host Microprocessor Interface (continued)

Host Register: 0x24. UART Status Bits

Add	Mode	7	6	5	4	3	2	1	0
24	R	T2NDS1	T2NDS0	X	X	R2NDS	X	X	X

Read only bits.

T2NDS1 — When set, input buffer is full. Do not write new data.

T2NDS0 — When set, transmit output shift register is empty.

R2NDS — When set, data is available for the host to read. Buffered output stage is full.

Host Register: 0x25. V.54 and V.13 Status Register

Add	Mode	7	6	5	4	3	2	1	0
25	R	V54DET	V54END	SY511N	◁	X			▷

Read only bits.

V54DET — V54 loop 2 initiation sequence detect. V.54 sequence has been received. The sequence detected depends on the state of R54SCR1 bit (0x2d[7]).

V54END — V54 End. V.54 ending sequence has been received. 37 marks following a V54 sequence.

SY511N — When low, 511 error register is valid.

Host Register: 0x28. Send Data, UART, and EIA Data Set Ready Control Bits

Add	Mode	7	6	5	4	3	2	1	0
28	R/W	◁	MSDCB[4:0]			▷	EURSTD	◁	DSRCB[1:0] ▷

Default = 0x63. Default modes are indicated below with an asterisk.

Refer to Figure MJ-6 (page MJ-48), EIA Data Path Control.

MSDCB[4:0] — Modem send data control bits. Select the following signals for transmission.

MSDCB[4] = 0

MSDCB[3:2]

00 – Enable muxed data as defined by MSDCB[1:0].

10 – Gate muxed data with EIA_RTS.

* 11 – Gate muxed data with EIA_CTS.

MSDCB[1:0]

* 00 – Enable TxD, external EIA data.

01 – Enable PSD (on pin 11) when in nonmultiplexed mode if EURSTD=0, or internal UART data (T2NDCHB[7:0] register 0x0) if EURSTD=1.

10 – Enable PSD (on pin 42) when in multiplexed mode.

11 – Enable MRD, modem receive data, remote loop.

MSDCB[4] = 1

MSDCB[3:2]

00 – Clamp data low.

01 – Clamp data high.

1x – Enable test pattern as defined by SEQ[1:0] and TSCRM1.

MSDCB[1:0]

xx – Don't care.

Host Microprocessor Interface (continued)

EUSRTD — Enable UART Data. The serial path of the UART is gated to the DCE data path. This allows the host to inject data bits directly into the data path without burden to the DSP. When this bit is cleared, the serial data path is gated to the DTE.

DSRCB[1:0] — Data set ready control bits. These bits can be controlled by the host, as well as the data pump. Gate the following register bits to the DSRN pin.

- 00 – DP_DSR AND H_DSR. (AND function of DP_DSR and H_DSR.)
- 01 – H_DSR. DSR written by host at location 0x2b[5].
- 10 – DP_DSR OR H_DSR. (OR function of DP_DSR and H_DSR.)
- * 11 – DP_DSR. DSR written by DSP at location 0x2b[4].

Host Register: 0x29. EIA Receive Data, Clear to Send, and Receiver Ready Control Bits

Add	Mode	7	6	5	4	3	2	1	0
29	R/W	RXDCB[3:0]				CTSCB[1:0]		RRCB[1:0]	

Default = 0x13. Default modes are indicated below with an asterisk.

Refer to Figure MJ-6 (page MJ-48), EIA Data Path Control.

RXDCB[3:0] — EIA receive data control bits. Select the following signals for EIA_RxD.

RXDCB[3] = 0

RXDCB[2]

- * 0 – Enable MRD. Modem receive data.
- 1 – Enable internal UART serial port.

RXDCB[1:0]

- 00 – Enable data all the time.
- * x1 – Gate data with J_RR. Joint DP_RR and V13_RR.
- 1x – Gate data with H_RR. Host receive ready.

RXDCB[3] = 1

RXDCB[2:0]

- 00x – MSD composite transmit signal after all muxing. Internal test mode.
- 01x – Enable PRD.
- 100 – Clamp data low.
- 101 – Clamp data high.
- 11x – Select TxD, direct terminal loopback.

CTSCB[1:0] — Clear to send control bits. Gate the following register bits to CTSN pin.

- * 00 – DP_CTS, 0x2b[0]. (DP_CTS is delayed with respect to RTSN by the number of milliseconds specified in C/S RAM location 0x00.)
- 01 – H_CTS, CTS written by host at register 0x2b[1].
- 10 – RTS input immediate feedback.
- 11 – Clamp CTSN high.

RRCB[1:0] — Receiver ready control bits. Gate the following register bits to RRN pin. (See Figure MJ-4, page MJ-45.)

- 00 – J_RR AND H_RR. (AND function of DP_RR and H_RR.)
- 01 – H_RR. RR written by host at location 0x2B[3].
- 10 – J_RR OR H_RR. (OR function of DP_RR and H_RR.)
- * 11 – J_RR.

Host Microprocessor Interface (continued)

Host Register: 0x2a. EIA Send and Receive Timing Control Bits

Add	Mode	7	6	5	4	3	2	1	0
2A	R/W	◁ STCB[2:0] ▷			STHIZ	◁ RTCB[2:0] ▷			RTHIZ

Default = 0x44. Default modes are indicated below with an asterisk.

Refer to Figure MJ-5 (page MJ-47), V.24 Timing Control.

STCB[2:0] — EIA send timing control bits. Gate and invert the following signals for EIA_STN.
STCB[2] – Inverts the selected clock.
STCB[1:0]
00 – Clamps STN high.
01 – Select XTCLK input.
* 10 – Select TBITCK, transmit bit clock.
11 – Select USRCLK, independent customer clock.

STHIZ — Force STN output into high-impedance mode.

RTCB[2:0] — EIA receive timing control bits. Gate and invert the following signals for EIA_RTN.
RTCB[2] – Inverts the selected clock.
RTCB[1:0]
00 – Clamps RTN high.
01 – Reserved.
* 10 – Select RBITCK, receive bit clock.
11 – Select USRCLK, independent customer clock.

RTHIZ — Force RTN output into high-impedance mode if RTCB[1] = 1.
If RTHIZ=1 and RTCB1=0, XTCLK input clock is gated onto RTN.

Host Register: 0x2b. EIA CTS, RTS, DTR, DSR, and RR Control and Status Bits

Add	Mode	7	6	5	4	3	2	1	0
2B	W	H_RTS	0	H_DSR	X	H_RR	X	H_CTS	X
	R	DTR	X	H_DSR	DP_DSR	H_RR	DP_RR	H_CTS	DP_CTS

Default = 0x00

Refer to Figure MJ-4 (page MJ-45), V.24 Control Signal Logic.

H_RTS — Host request to send. This control bit is OR'd with RTS ($\overline{\text{RTSN}}$) for the purpose of controlling DP_CTS. After start-up is complete, H_RTS can be used to force DP_CTS active, independent of RTSN. This can be important, since MSD is gated with DP_CTS in this chip set. See Figure MJ-6, page MJ-48.

DTR — Data terminal ready input pin.

H_DSR — Host data set ready, allows the host to control the DSRN lead.

DP_DSR — Data pump data set ready, allows the DSP to control the DSRN lead.

H_RR — Host receiver ready, allows the host to control the RR lead.

DP_RR — Data pump receiver ready. State of the data pump RR signal before the V.13 circuitry.

H_CTS — Host clear to send, allows the host to control the CTSN lead.

DP_CTS — Data pump clear to send. State of the data pump CTS signal before the V.13 circuitry.

Host Microprocessor Interface (continued)

Host Register: 0x2c. Asynchronous Control Register

Add	Mode	7	6	5	4	3	2	1	0
2C	W	STAOSP	RSTAE	◁—— RCHRL[1:0] ——▷		0	TATSE	◁—— TCHRL[1:0] ——▷	

Default: 0x00 (synchronous operation). Default modes are indicated below with an asterisk.

For synchronous operation, this register should be written with 0x00. Although FSK modes are asynchronous, this register must be set to 0x00 for all FSK modes.

Write only bits.

STAOSP — Sync to async over speed. When active, the STA circuit on the receiver side will reduce the stop bits by 25% during overspeed conditions. Otherwise, stop bits will be shrunk by only 12.5%. The transmitter automatically adjusts itself.

RSTAE — Receive sync to async enable. Asynchronous operation on the receiver output is enabled with full V.14 compatibility. Must be cleared for FSK modes.

RCHRL[1:0] — Receive character length, including data, parity, start, and one stop bit.
* 00 – Eight bits per character.
01 – Nine bits per character.
10 – Ten bits per character.
11 – Eleven bits per character.

TATSE — Transmit async to sync enable. Asynchronous operation on the transmitter input is enabled with full V.14 compatibility. Must be cleared for FSK modes.

TCHRL[1:0] — Transmit character length, including data, parity, start, and one stop bit.
* 00 – Eight bits per character.
01 – Nine bits per character.
10 – Ten bits per character.
11 – Eleven bits per character.

Host Microprocessor Interface (continued)

Host Register: 0x2d. V.54, V.13, and 511 Control Register

Add	Mode	7	6	5	4	3	2	1	0
2D	R/W	RSCRM1	SV54END	V54CLR	RCVERR	TSCRM1	◁— SEQ[1:0] —▷		V13ENA

Default: 0x0

RSCRM1 — Receive scramble one. Used to select which V.54 sequence detection is enabled:
* 0 – space sequence.
1 – mark sequence.

SV54END — Select V.54 end. Enables search for V.54 ending sequence: 37 continuous marks immediately following a scrambled sequence detection.

V54CLR — V.54 clear. Clear all of the V.54 circuitry, counter, and flags. Must be inactive to operate. A zero-to-one-to-zero sequence clears the status and restarts the search.

RCVERR — Receive error sequence. Enables search for 511 or dotting sequence. For the 511 sequence (SEQ=10), the circuit looks for an error-free pattern as a good seed, locks it in a circular shift register, and then enables the error counter. For the dotting sequence (SEQ=11), the error counter is enabled with no seed locking. In either case, the number of errors is read from register 0x23. Toggle this bit from 0 to 1 to resync the detector circuitry and enable the counter.

TSCRM1 — Transmit scramble one. Transmitted sequence, any of them, will be scrambled with one when activated. This bit must be set when V13 mode (bit 0) is enabled.

SEQ[1:0] — Transmit and receive sequence selection.
* 00 – V.13 sequence. Bit 1 = bit 7 XOR bit 3.
01 – V.54 sequence. Bit 1 = bit 7 XOR bit 4.
10 – 511 sequence. Bit 1 = bit 9 XOR bit 5.
11 – Dotting. Bit 1 = bit 1N.

V13ENA — V.13 enable. Must be active to allow V.13 compatibility mode.

Host Microprocessor Interface (continued)

Host Register: 0x2e, 0x30. Host Interrupt Control/Status Registers

Add	Mode	7	6	5	4	3	2	1	0
2E	W								
	R	UARTI	V13CTSI	V54IQI	CRBNKI	CWBNKI	RTSEDGI	RIEDGI	JRREDGI
30	R								

Although registers 0x2e and 0x2f share the same bit descriptions, the uses of registers 0x2e and 0x30 differ. Following is a description of how each of these registers is used:

- Register 0x2e. Interrupt Mask Control Register (Write)
  On writes, this register is used to mask individual interrupt sources. Only bits that are unmasked (zero) may cause a host interrupt. By default, all interrupt sources are masked (this is equivalent to 0xff having been written to register 0x2e).
- Register 0x2e. Interrupt Mask Status Register (Read)
  On reads, this register indicates which interrupt event caused the interrupt to occur. After the interrupt is serviced, the interrupt status bit must be reset by writing the appropriate value to register 0x2f.
- Register 0x30. Unmasked Interrupt Status Register (Read only)
  On reads, this register indicates all pending interrupt events, regardless of the interrupt mask. This register is typically used when polling. After an event is serviced, the status bit must be reset by writing the appropriate value to register 0x2f.

Bit descriptions:

UARTI	UART interrupt. OR function of the following bits: UARTI = Rx2ND_IQ + Tx2ND_IQ. See register 0x1e for details.
V13CTSI	V.13 CTS interrupt. Active as long as V13_CTS is high in response to active RTS, after the transmission of the ON sequence. Indicates to the host the current status.
V54IQI	V54 interrupt. V54 sequence has been received or end has been detected. The sequence detected depends on the state of RSCRM1 bit (0x2D[7]). If SV54END bit (0x2D[6]) is active, V.54 ending sequence will generate an interrupt.
CRBNKI	Read bank interrupt. Indicates a read operation by the data pump from the trigger byte location of mailbox 0x9.
CWBNKI	Write bank interrupt. Indicates a write operation by the data pump at the trigger byte location of mailbox 0xf.
RTSEDGI	Request to send edge interrupt. Indicates a transition on RTS input. The type of transition is read at 0x2f.
RIEDGI	Ring indicator edge interrupt. Indicates a transition on RI register bit. The type of transition is read at 0x2f.
JRREDGI	Joint receive ready edge interrupt. Indicates a transition on the joint RR status. The type of transition is read at 0x2f. Joint RR = (V13RR + $\overline{\text{V13ENA}}$) · DP_RR.

Host Microprocessor Interface (continued)

Host Register: 0x2f. Host Interrupt Control/Status Register (continued)

Add	Mode	7	6	5	4	3	2	1	0
2F	W	RST_RTSLH	RST_RILH	RST_JRRLH	RST_CRBNK	RST_CWBNK	RST_RTSHL	RST_RIHL	RST_JRRHL
	R	RTSLH	RILH	JRRLH	RTSLVL	JRRLVL	RTSHL	RIHL	JRRHL

This register has two uses:

- Register 0x2f. Interrupt Reset Register (Write)
  This register is used to reset the interrupt status bits.

  RST_i — Interrupt reset. A write to this location selectively clears the interrupt activity conditions specified by a 1 in the corresponding bits to be cleared. Note that there is a selective edge clear even though the interrupt bit is a composite of the two.

  UARTI is cleared by either clearing the active bits or responding to the request by read or write of the UART. V13CTSI cannot be cleared, only disabled, while V54IQI is cleared at the source by setting the V54CLR bit.

- Register 0x2f. Interrupt Status Detail Register (Read)
  This register is used to determine which transition caused the RR, RI, or RTS interrupts.

  RTSLH — Request to send low-to-high transition has occurred. This bit is cleared with RST_RSTLH.

  RILH — Ring indicator low-to-high transition has occurred. This bit is cleared with RST_RILH.

  JRRLH — Joint and V.13 receive ready low-to-high transition has occurred. This bit is cleared with RST_JRRLH.

  RTSLVL — Request to send level. RTS input pin status.

  JRRLVL. — Joint receive ready level. JRR internal status.

  RTSHL — Request to send high-to-low transition has occurred. This bit is cleared with RST_RTSHL.

  RIHL — Ring indicator high-to-low transition has occurred. This bit is cleared with RST_RIHL.

  JRRHL — Joint and V.13 receive ready high-to-low transition has occurred. This bit is cleared with RST_JRRHL.

Host Microprocessor Interface (continued)

Host Command Set

Table MJ-2 lists the host command set. These commands are used by the host to initialize, setup, and alter the data pump configuration. A unique numeric code is assigned to each host command. Mailbox 0x9 is used to pass the command to the DSP. The mailboxes at addresses 0x4 to 0x8 are used to pass any command parameters.

To execute a command, the host first writes the command parameters into locations 0x4—0x8. The specific code for the command is then written into the mailbox at location 0x9. This generates an internal interrupt, and the data pump automatically reads and processes the command. When the data pump reads the host command, the CRBNKI bit in register 0x30 of the data pump is set. Or, if interrupts were enabled by setting bit 4 in register 0x2e, an interrupt would be generated. The time required for the data pump to process a command depends on the current operating mode. Table MJ-3 lists the worst-case command response times for each operating mode.

Responses from Data Pump to Host

Registers 0x0a—0x0f are used by the data pump for responses to host commands. After processing a command that requests information, the data pump returns the requested information, along with a response code. Presently, this includes commands 0x4, 0x5, 0xd, 0x10, and 0x14. The requested information is written to mailboxes 0xd and 0xe. The response code is then written to mailbox 0xf, setting bit CWBNKI in register 0x30. The host can either poll this register or, during initialization, can set up the masking bit in register 0x2e and wait for the interrupt (after an interrupt, register 0x30 is read to determine the cause of the interrupt).

Status Information

The mailboxes at addresses 0x0a—0x0b are used for constant status and parameter reporting to the host. The host can choose the desired information to be reported by the data pump at any time by providing the address of the control and status RAM location that provides the desired information. This address is stored in control and status memory location 0x3c. Periodically, the value of the specified location is loaded into mailboxes 0x0a—0x0b. By default, this is the operating status word (C/S RAM location 0x3a). The period of the status reporting updates is determined by the current operating mode. The update period (worst-case) for each mode corresponds to the worst-case command response time listed in Table MJ-3.

Host Microprocessor Interface (continued)

Table MJ-2. Summary of Host Commands to the Data Pump

Command Code (hex)	Description	Response Code
0x01	Write to control and status DSP RAM.	—
0x02	Initiate V.32bis rate renegotiation	—
0x03	Reserved for future use.	—
0x04	Read from control and status DSP RAM.	1
0x05	Read status word and clear SD and RD status bits.	4
0x06	Reserved for future use.	—
0x07	Generate tones.	—
0x08	Detect tones.	—
0x09	Detect DTMF tones.	—
0x0a	DTMF dialing.	—
0x0b	Pulse dialing.	—
0x0c	Local loop test.	—
0x0d	Read DSP RAM location and then clear.	1
0x0e	Start-up.	—
0x0f	Initiate retrain sequence.	—
0x10	Report firmware version.	5
0x11	Connect to line (off hook).	—
0x12	Disconnect from line (on hook) and return to idle.	—
0x13	Return to idle.	—
0x14	Check DSP program memory.	3
0x80	Parallel data transmit command	—
0xa0	Enter Voice-thru mode	—

Table MJ-3. Worst-Case Command Response Times

Operating Modes	Worst-Case Time
V.32terbo, V.32bis, V.32, V.17	670 µs
V.29	580 µs
V.27ter 4800	850 µs
V.27ter 2400	1 ms
V.21 Ch. 2	3.4 ms
V.22, V.22bis, and Bell 212A	294 µs
V.23, V.21, and Bell 103	146 µs
Idle mode	21 µs
Idle mode (with all tone generators and IIR filters enabled)	105 µs

Host Microprocessor Interface (continued)

Table MJ-4. Host Commands to Data Pump

<table>
<tr><th>Command Code (hex)</th><th>Description</th></tr>
<tr><td>0x01</td><td>Write to control and status DSP RAM location.
This command writes one 16-bit word to the control and status RAM location specified by the address passed in mailboxes 6 and 7. The 16-bit value is passed in mailboxes 4 and 5.
<table>
<tr><th>Mailbox</th><th>Content</th></tr>
<tr><td>0x04</td><td>Least significant byte of value to write.</td></tr>
<tr><td>0x05</td><td>Most significant byte of value to write.</td></tr>
<tr><td>0x06</td><td>Least significant byte of address.</td></tr>
<tr><td>0x07</td><td>Most significant byte of address.</td></tr>
<tr><td>0x08</td><td>Not used.</td></tr>
<tr><td>0x09</td><td>0x01.</td></tr>
</table></td></tr>
<tr><td>0x02</td><td>Initiate V.32bis rate renegotiation. (Valid in V.32bis modes only.)
This command causes the data pump to initiate a rate renegotiation sequence with the far-end modem. This command would typically be used if a receive signal parameter, such as received mean squared error, indicates that the rate should be increased or decreased. Before issuing the command, the V.32 rate selection word (C/S RAM location 0x01) should be set to indicate which rates are to be tried.

When the modem detects a rate renegotiation request from the remote modem, the renegotiation sequence is automatically started. The two modems will agree on the highest mutually acceptable rate.

Note: This command should only be executed if the remote modem supports V.32bis modes. Bits 4 and 8 of the received rate sequence (C/S RAM location 0x35) are set when the remote modem supports V.32bis modes.</td></tr>
<tr><td>0x03</td><td>Reserved for future use.</td></tr>
</table>

Host Microprocessor Interface (continued)

Table MJ-4. Host Commands to Data Pump (continued)

<table>
<tr><th>Command Code (hex)</th><th>Description</th></tr>
<tr><td>0x04</td><td>Read from control and status DSP RAM location.
This command reads one 16-bit word from the control and status RAM location specified by the address passed in mailboxes 6 and 7.
<table>
<tr><th>Mailbox</th><th>Content</th></tr>
<tr><td>0x06</td><td>Least significant byte of address.</td></tr>
<tr><td>0x07</td><td>Most significant byte of address.</td></tr>
<tr><td>0x08</td><td>Not used.</td></tr>
<tr><td>0x09</td><td>0x04.</td></tr>
</table>
The format of the returned value is:
<table>
<tr><th>Mailbox</th><th>Content</th></tr>
<tr><td>0x0d</td><td>Least significant byte of requested location.</td></tr>
<tr><td>0x0e</td><td>Most significant byte of requested location.</td></tr>
<tr><td>0x0f</td><td>0x01.</td></tr>
</table></td></tr>
<tr><td>0x05</td><td>Read status word and clear SD and RD activity.
This command returns the operational status word (location 0x3a) and also clears the SD and RD mark and space status bits (bits 6—9). The status word is returned as:
<table>
<tr><th>Mailbox</th><th>Content</th></tr>
<tr><td>0x0d</td><td>Status word least significant byte.</td></tr>
<tr><td>0x0e</td><td>Status word most significant byte.</td></tr>
<tr><td>0x0f</td><td>0x05.</td></tr>
</table>
This command must be used to read the operational status word if SD and RD activity is being monitored, as command 0x04 does not clear the SD and RD activity bits. Refer to the description for the operating status word (C/S location 0x3a), page MJ-38, for more information about the use of this command.</td></tr>
<tr><td>0x06</td><td>Reserved for future use.</td></tr>
</table>

Host Microprocessor Interface (continued)

Table MJ-4. Host Commands to Data Pump (continued)

<table>
<tr><th>Command Code (hex)</th><th>Description</th></tr>
<tr><td>0x07</td><td>Generate tones (max. 3 frequencies at a time). (Not available in data mode.)
This command causes up to 3 tones to be transmitted at a time. The number of tones is specified in mailbox 0x08. Prior to issuing this command, frequency constants corresponding to the desired tones must be stored in locations 0x05—0x0a, and tone power levels must be stored in locations 0x11—0x13 of the Control and Status RAM. (Refer to page MJ-31 of Control and Status RAM for a definition of these constants.) Check the operating status word (C/S location 0x3a) bit 4 to determine when the tone generation has completed.
<table>
<tr><th>Mailbox</th><th>Content</th></tr>
<tr><td>0x08</td><td>Number of tones.</td></tr>
<tr><td>0x09</td><td>0x07.</td></tr>
</table></td></tr>
<tr><td>0x08</td><td>Detect tones (max. 10 frequencies at a time). (Not available in data mode.)
This command instructs the data pump to look for up to 10 tones. The number of tones is specified in mailbox 0x08. Prior to issuing this command, frequency constants specifying the desired tones must be stored in locations 0x1c—0x25, and the tone detection threshold must be stored in location 0x26 of the control and status RAM. (Refer to page MJ-33 of Control and Status RAM for a definition of these constants.)
<table>
<tr><th>Mailbox</th><th>Content</th></tr>
<tr><td>0x08</td><td>Number of frequencies.</td></tr>
<tr><td>0x09</td><td>0x08.</td></tr>
</table>
Results for this command are available in two locations of control and status RAM. Location 0x27 contains the number of tones detected. Location 0x28 indicates which specific tones were detected. In addition, the relative power levels for each tone are available in locations 0x29—0x32. (Refer to page MJ-35 of Control and Status RAM for a definition of these values.)

This command is also used to activate two programmable 6th-order IIR filters. See Programmable IIR Filters, page B-11, for more information.</td></tr>
</table>

Host Microprocessor Interface (continued)

Table MJ-4. Host Commands to Data Pump (continued)

<table>
<tr><th>Command Code (hex)</th><th>Description</th></tr>
<tr><td>0x09</td><td>Detect DTMF tones. (Not available in data mode.)
This command instructs the DSP to look for each of the 8 DTMF tones (4 high band and 4 low band frequencies). Frequency constants corresponding to the DTMF frequencies are automatically loaded into locations 0x1c—0x25 of the control and status RAM. (Note that previously loaded constants are overwritten.)
As with the detect tones command, results are available in locations 0x27—0x30. (Since there are only 8 DTMF frequencies, locations 0x31 and 0x32 are unused in this case.) For a valid DTMF detection, the number of frequencies detected should be two. See the description of C/S RAM location 0x28, page MJ-34, for the correspondence between tone detected bits and the DTMF frequencies. It is necessary for the host processor to perform a table look-up or other procedure to convert the "tones detected" word to the corresponding DTMF digit.</td></tr>
<tr><td>0x0a</td><td>DTMF dialing. (Not available in data mode.)
This command instructs the data pump to dial the specified DTMF digit. If other than the default DTMF dialing parameters are to be used, they must first be stored in control and status RAM locations 0x11, 0x12, 0x17, and 0x18. Monitor the operating status word (C/S location 0x3a) bit 4 to determine when each tone transmission has completed.
<table>
<tr><th>Mailbox</th><th>Content</th></tr>
<tr><td>0x08</td><td>Digit to be dialed. Following are the values that correspond to the digits:
Digit — Value to place in mailbox 0x08
0—9 — 0x0—0x9 (integer value of digit)
* — 0xa
# — 0xb
A — 0xc
B — 0xd
C — 0xe
D — 0xf</td></tr>
<tr><td>0x09</td><td>0x0a.</td></tr>
</table>
</td></tr>
</table>

Host Microprocessor Interface (continued)

Table MJ-4. Host Commands to Data Pump (continued)

<table>
<tr><th>Command Code (hex)</th><th>Description</th></tr>
<tr><td>0x0b</td><td>Pulse dialing. (Not available in data mode.)
This command instructs the data pump to pulse dial the specified digit. If other than the default pulse dialing parameters are to be used, they must first be stored in control and status RAM locations 0x19—0x1b.
<table>
<tr><th>Mailbox</th><th>Content</th></tr>
<tr><td>0x08</td><td>Digit to be dialed.</td></tr>
<tr><td>0x09</td><td>0x0b.</td></tr>
</table></td></tr>
<tr><td>0x0c</td><td>Local loop test.
This command instructs the data pump to enter a local loop test mode (CCITT V.54 loop 3) at the speed and modulation mode specified by control and status words 1 and 2. The format of the command is:
<table>
<tr><th>Mailbox</th><th>Content</th></tr>
<tr><td>0x08</td><td>0 = use answer carrier.
1 = use originate carrier.</td></tr>
<tr><td>0x09</td><td>0x0c.</td></tr>
</table>
Note: Impairment status information is not relevant during local loop mode.</td></tr>
<tr><td>0x0d</td><td>Read DSP RAM and then clear location.
This command reads a specified DSP RAM location and then clears the location. The format for the command and its response are identical to command 0x4 (Read from control and status RAM). Automatic clearing is useful when reading certain parameters such as peak squared error; however, it should be used with caution.
This command reads one 16-bit word from the control and status RAM location specified by the address passed in mailboxes 6 and 7.
<table>
<tr><th>Mailbox</th><th>Content</th></tr>
<tr><td>0x06</td><td>Least significant byte of address.</td></tr>
<tr><td>0x07</td><td>Most significant byte of address.</td></tr>
<tr><td>0x08</td><td>Not used.</td></tr>
<tr><td>0x09</td><td>0x0d.</td></tr>
</table>
The format of the returned value is:
<table>
<tr><th>Mailbox</th><th>Content</th></tr>
<tr><td>0x0d</td><td>Least significant byte of requested location.</td></tr>
<tr><td>0x0e</td><td>Most significant byte of requested location.</td></tr>
<tr><td>0x0f</td><td>0x01.</td></tr>
</table></td></tr>
</table>

Host Microprocessor Interface (continued)

Table MJ-4. Host Commands to Data Pump (continued)

<table>
<tr><th>Command Code (hex)</th><th>Description</th></tr>
<tr><td>0x0e</td><td>Start-up.
This command causes the data pump to perform either an originate or answer mode start-up at the speed and modulation mode specified by control and status words 1 and 2. The format of this command is:
<table>
<tr><th>Mailbox</th><th>Content</th></tr>
<tr><td>0x08</td><td>0 = answer (in half-duplex, receive).
1 = originate (in half-duplex, transmit).</td></tr>
<tr><td>0x09</td><td>0x0e.</td></tr>
</table>
When performing a 4-wire V.32 start-up, the V.25 answer sequence can be disabled. This is accomplished by setting bit 3 high in the options control register in DSP control and status RAM (location 0x38).
Note: For V.17 modes, the RTS signal controls whether the data pump is configured for transmit or receive.</td></tr>
<tr><td>0x0f</td><td>Initiate retrain sequence. (Valid in V.32 and V.22bis modes only.)
This command causes the data pump to initiate a retrain sequence with the far-end modem. This command would typically be issued if a received signal parameter, such as received mean square error, indicated unacceptable performance.
When the modem detects a retrain request from the remote modem, a retrain is automatically started. Therefore, a retrain command need not be issued in this case.</td></tr>
<tr><td>0x10</td><td>Report firmware version.
This command returns the firmware version of the DSP. This value is returned as:
<table>
<tr><th>Mailbox</th><th>Content</th></tr>
<tr><td>0x0d</td><td>Version number least significant byte.</td></tr>
<tr><td>0x0e</td><td>Version number most significant byte.</td></tr>
<tr><td>0x0f</td><td>0x05.</td></tr>
</table>
For ROM code MJ, the firmware version is 6.5 (mailbox 0x0d returns 5, 0x0e returns 6).</td></tr>
<tr><td>0x11</td><td>Connect to line (off-hook).
This command instructs the data pump to close the line control relay, causing the modem to go off-hook. This command should be issued prior to a start-up, dialing, or detect tones command.</td></tr>
<tr><td>0x12</td><td>Disconnect from line (on-hook).
This command instructs the data pump to open the line control relay, causing the modem to go on-hook and return to idle.</td></tr>
</table>

Host Microprocessor Interface (continued)

Table MJ-4. Host Commands to Data Pump (continued)

Command Code (hex)	Description
0x13	**Return to idle.** This command terminates any ongoing operation and returns to idle.
0x14	**Check DSP program memory.** The command instructs the data pump to perform a checksum test of the DSP program memory. The result is placed in location 0x49 of the control and status RAM. Once the operation is done, a response code of 3 is returned to mailbox 0xf. For data pumps using DSP16A ROM code MJ, the checksum value expected in C/S RAM location 0x49 is 0xA610 **Note:** This command should only be issued while in idle mode.
0x80	**Parallel data transmit command.** (Available only in parallel data transfer mode.) While parallel data transfer mode is active, each data transmit command uses the command code 0x80. See Using Parallel Data Transfer Mode, page MJ-51, for detailed information. **Note:** Parallel data transfer mode is started by setting bit 8 of C/S RAM location 0x3d.
0xa0	**Enter Voice-thru mode.** (Not available in data mode.) This command instructs the data pump to enter the voice-thru mode. See Using Voice-Thru Mode, page MJ-53, for detailed information. Prior to issuing this command, the following parameters should be specified.

Mailbox	Content
0x02	Mode (can be one of the following): 0 – Voice-Thru Mode — 16-bit linear samples 4 – Voice-Thru Mode — μ-law samples 7 – Voice-Thru Mode — a-law samples
0x03	Sampling rate value A. *
0x04	Sampling rate value B. *
0x05	Transmit (playback) level. See Table MJ-11, page MJ-54. If this parameter is zero, the default value is used.
0x06	Receive (record) level. See Table MJ-11, page MJ-54. If this parameter is zero, the default value is used.
0x07	Translation mode option bit. 0 – This parameter must be set to zero.
0x08	Not used.
0x09	0xA0

* If either sampling rate parameter is zero, the default rate of 8 kHz is used.

Note: While voice-thru mode is active, each data transmit command also uses the command code 0xa0, although in this case the parameters differ. See Table MJ-13, page MJ-55, in the Using Voice-Thru Mode section.

To exit voice-thru mode, issue the return to idle command (0x13).

Host Microprocessor Interface (continued)

Control and Status RAM Locations

The host can control and monitor the operation of the data pump (the DSP in particular) by means of the control and status words in DSP RAM defined in this section. The control words are used by the host to set operational parameters and select options. Table MJ-5 summarizes the control and status RAM locations, and the following sections describe each location in more detail. Control and status RAM locations are accessed by the host using commands 0x01 and 0x04.

All options and parameters in control and status RAM are defaulted at reset. Nondefault values required by the host must be written following each reset. In addition, certain locations must be written prior to issuing a related command.

Table MJ-5. Control and Status RAM Locations

Address (hex)	Description	Default	R/W	Fmt†	Page
0x00	RTS-CTS delay (ms)	0	R/W	16:0	MJ-29
0x01	V.32 rate selection (default: 9600 coded)	0x89e0	R/W	—	MJ-29
0x02	Low-speed rate selection	0	R/W	—	MJ-30
0x03	Transmit level (dBm)	–10 dBm	R/W	16:0	MJ-31
0x04	Transmit compromise equalization (dB)	4	R/W	16:0	MJ-31
0x05—0x0a *	Frequency constants for tone generation	—	R/W	2:14	MJ-31
0x0c	V.17 Rate Selection Word	0	R/W	—	MJ-31
0x11 *	DTMF high-frequency power/power for tone 1 (dBm)	–10 dBm	R/W	16:0	MJ-32
0x12 *	DTMF low-frequency power/power for tone 2 (dBm)	–12 dBm	R/W	16:0	MJ-32
0x13 *	Transmit power level for tone 3 (dBm)	–10 dBm	R/W	16:0	MJ-32
0x17	Tone duration: DTMF dialing and tone generation (ms)	70 ms	R/W	16:0	MJ-32
0x18	Interdigit delay for DTMF dialing (ms)	70 ms	R/W	16:0	MJ-32
0x19	Make time for pulse dialing (ms)	36 ms	R/W	16:0	MJ-32
0x1a	Break time for pulse dialing (ms)	64 ms	R/W	16:0	MJ-32
0x1b	Interdigit delay for pulse dialing (ms)	750 ms	R/W	16:0	MJ-32
0x1c—0x25 *	Frequency constants for tone detection	—	R/W	2:14	MJ-33
0x26 *	Receive threshold for DTMF and tone detection (dBm)	–43 dBm	R/W	16:0	MJ-33
0x27	Number of tones detected	—	R	16:0	MJ-33
0x28	Detected DTMF and programmable tones	—	R	—	MJ-34
0x29—0x32	Detected tone (relative) power levels	—	R	16:0	MJ-35
0x35	Received rate sequence (V.32 only)	—	R	—	MJ-35
0x36	Current line speed	—	R	—	MJ-35
0x37	Receiver signal threshold level (dBm)	–43 dBm	R/W	16:0	MJ-35
0x38	Options control register	0	R/W	—	MJ-36
0x39	FAX options word	0x00	R/W	—	MJ-37
0x3a	Operating status	—	R/W	—	MJ-38
0x3b	Automode status / FAX status word	—	R	—	MJ-39
0x3c	Address for fast status to mailboxes A and B	0x3a	R/W	—	MJ-40

* Locations marked with an asterisk are modified by the data pump during a start-up sequence. It is necessary to rewrite any required non-default values to these locations after returning to idle mode from data mode and prior to issuing a related command.

† The format string *n:m* indicates that the value should be interpreted as having an implied decimal point between bits *n* and *m*. This is known as Q*m*. For example, 2:14 (or Q14) indicates 14 bits to the right of the implied decimal point. A value in Q*m* is stored as the actual value multipled by 2^m. For example, the value decimal value –1.175235 would be encoded as 0xb4c9 in Q14 and the decimal value 10.5 would be encoded as 0x0a80 in Q8.

Host Microprocessor Interface (continued)

Table MJ-5. Control and Status RAM Locations (Continued)

Address (Hex)	Description	Default	R/W	Fmt	Page
0x3d	HDLC options control word		R/W	—	MJ-41
0x3e	Total in-band energy level for tone detectors (dBm)	—	R	8:8	MJ-41
0x3f	Transmit mute	0	R/W	na	MJ-41
0x40	Ring detect period lower limit (default: 68 Hz)	18	R/W	16:0	MJ-41
0x41	Ring detect period high limit (default: 15 Hz)	80	R/W	16:0	MJ-42
0x42	Answer mode silent interval duration (default: 2 seconds)	4800	R/W	16:0	MJ-42
0x43	Number valid/invalid ringing cycles to enable/disable RI	5	R/W	16:0	MJ-42
0x44	Echo correlator level	—	R/W	16:0	MJ-42
0x48	Carrier drop out timeout (default: 2 seconds)	–4800	R/W	16:0	MJ-42
0x49	Program memory checksum	—	R	16:0	MJ-43
0x4a	Receive signal level (dBm)	—	R/W	8:8	MJ-43
0x4b	Receive signal squared error	—	R/W	16:0	MJ-43
0x4c	Receive signal mean squared error	—	R/W	16:0	MJ-43
0x4d	Receive signal peak squared error (dBm)	—	R/W	8:8	MJ-44
0x4e	RMSE scale factor	0	R/W	16:0	MJ-44
0x51	RMSE averaging time constant	0	R/W	16:0	MJ-44
0x54	Round trip delay. V.32 mode only. (ms)	—	R/W	16:0	MJ-44
0x55	Near echo level. V.32 mode only. (dBm)	—	R/W	8:8	MJ-44
0x56	Far echo level. V.32 mode only. (dBm)	—	R/W	8:8	MJ-44
0x760	IIR filter 1 threshold level (dBm)	—	R/W	16:0	B-11
0x761	IIR filter 2 threshold level (dBm)	—	R/W	16:0	B-11
0x764—0x773	IIR filter 1 coefficients	—	R/W	2:14	B-11
0x774—0x783	IIR filter 2 coefficients	—	R/W	2:14	B-11
0x784	IIR filter 1 detected power level (dBm)	—	R/W	16:0	B-11
0x785	IIR filter 2 detected power level (dBm)	—	R/W	16:0	B-11

C/S RAM Location: 0x00. RTS-CTS Delay

This word selects the delay from the time that RTS turns on until CTS is turned on. The units are milliseconds (ms). The default value is 0, and the valid range is from 0 to 4500 ms. Since this value is used at start-up, it must be set before the startup command is issued.

C/S RAM Location: 0x01. V.32 Rate Selection

This word selects the desired V.32 operating rate. The table gives the rate selection word values for each rate corresponding to a single-speed operation. To enable multiple rates, OR together the values shown in the table for each of the desired rates. For example, to allow all possible V.32terbo rates, a value of 0xfff0 should be used. A clear down (disconnect) is called for by using the value shown in the table (0x8880) and then issuing a retrain command (0x0f).

Automode operation (according to V.32bis Annex A) is selected by setting at least one valid V.32 rate (other than clear down) as well as at least one V.22bis (or V.22) bit in the low-speed rate selection word. The actual operating speed will be negotiated with the remote modem during start-up and will be the highest mutually agreeable speed. Extended automode to FSK and Bell 212A according to EIA/TIA Draft Standard TR 30.1/90-06 will occur when, in addition to at least one V.32 rate and at least one V.22/V.22bis rate, any of the FSK or the Bell 212A bits are set. Extended automode will only automode to the rates that are set in the low-speed rate selection word.

If this word is modified after the initial connection, future retrains and rate renegotiations will use the new value.

Host Microprocessor Interface (continued)

The default value of 0x89e0 corresponds to V.32 9600 bits/s with possible fallbacks of 9600 uncoded and 4800 uncoded. If no V.32 rates are desired, this register should be written with 0x0000.

Bit 4 and 8 together indicate a V.32bis mode; bit 4 and 8 together with either bit 13 or 14 indicate V.32terbo; bit 8 alone (i.e., with bit 4 clear) indicates trellis coding

Word Bits																Description
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	V.32 4800 bits/s
1	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0	V.32 9600 bits/s
1	0	0	0	1	0	0	1	1	1	0	0	0	0	0	0	V.32 trellis coded 9600 bits/s
1	0	0	0	1	0	0	1	1	0	1	1	0	0	0	0	V.32bis 4800 bits/s
1	0	0	0	1	0	1	1	1	0	0	1	0	0	0	0	V.32bis 7200 bits/s
1	0	0	0	1	0	0	1	1	1	0	1	0	0	0	0	V.32bis 9600 bits/s
1	0	0	0	1	1	0	1	1	0	0	1	0	0	0	0	V.32bis 12,000 bits/s
1	0	0	1	1	0	0	1	1	0	0	1	0	0	0	0	V.32bis 14,400 bits/s
1	0	1	0	1	0	0	1	1	0	0	1	0	0	0	0	V.32terbo 16,800 bits/s
1	1	0	0	1	0	0	1	1	0	0	1	0	0	0	0	V.32terbo 19,200 bits/s
1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	Clear down sequence

C/S RAM Location: 0x02. Low-Speed Rate Selection

This word selects the low speed modulation type: V.22bis with choices of 2400, 1200, or 600 bits/s; FSK with choices of V.21, V.23 (600 or 1200), and Bell 103.

Bit	Description	
0	V.22bis 2400 bits/s	Low-speed data modes
1	V.22 1200 bits/s	
2	V.22 600 bits/s	
3	Bell 202 1200 bits/s (caller ID)	
4	Bell 103 0—300 bits/s	
5	V.21 0—300 bits/s	
6	V.23 600 bits/s	
7	V.23 1200 bits/s	
8	V.29 9600 bits/s	FAX modes
9	V.29 7200 bits/s	
10	V.27ter 4800 bits/s	
11	V.27ter 2400 bits/s	
12	V.21 Ch. 2 300 bits/s	

Notes:

1. Since V.22 defines no fallback procedure, only 1 speed can be chosen at a time when using V.22 modes.
2. Bell 212A is selected by setting bit 1 (V.22 1200 bits/s) and bit 0 in host options register 0x38 (2225 Hz answer tone). If only Bell 212A mode is desired (no automode), the V.25 answer sequence must be disabled (CS location 0x39[3]=1).
3. When both V.23 bits are set, automode will only automode to V.23 1200 bits/s. Therefore, V.23 600 bits/s has to be the only V.23 bit set to automode this rate. Also, V.23 in automode assumes that bit 4 of host options register 0x38 is 0. Therefore, if automode switches to V.23 and the receiver is receiving errors, then either the speed is incorrect or the V.23 mode is incorrect. And, since the automode status register indicates

Host Microprocessor Interface (continued)

that it is, in fact, communicating with a V.23 modem, different combinations of V.23 speed and mode followed by start-up commands can be used to determine the correct configuration if the far-end V.23 configuration is unknown.

C/S RAM Location: 0x03. Transmit Level

This word controls the transmit output level for all modes except DTMF dialing and tone generation (there are separate words for this). The units are dBm measured differentially across codec pins ROP and RON. The valid range is 0 to 20 dBm with an implied minus sign. For example, to get a level which is –10 dBm, a value of 0xa should be entered. This control is accurate to ±1 dB.

C/S RAM Location: 0x04. Transmit Compromise Equalization

This location specifies the positive slope in the transmit spectrum in dB between 1000 Hz and 2800 Hz when in V.32 modes. The range is 0 to +15 dB. The default is +4 dB.

C/S RAM Location: 0x05—0x0a. Frequency Constants for Tone Generation

These locations determine the tone frequencies generated by the DSP in response to a transmit tone command. Up to 3 tones may be generated at a time. For each tone, two frequency constants must be stored. For tone 1, location 0x5 contains $\sin(\theta_1)$ and 0x6 contains $\cos(\theta_1)$ where $\theta_1 = \frac{2\pi f_1}{7200}$ and f_1 is the frequency of tone 1. The sin and cos values must be scaled by a factor of 2^{14} or 16,384 (this is binary fraction format Q14) with the binary point immediately to the right of bit 14.

For example, to generate 1800 Hz, the sine value would be 1.0. After scaling, this value becomes $1.0 \cdot 16384 = 16384$ in Q14 format. For additional frequencies, sin and cos values are stored in consecutive locations beginning at address 0x7.

Note: These values must be loaded immediately prior to issuing a "generate tone" command, as they are overwritten by the data pump during a startup sequence.

Address (hex)	Description
0x05	$\sin(k_1)$ for tone 1
0x06	$\cos(k_1)$ for tone 1
0x07	$\sin(k_2)$ for tone 2
0x08	$\cos(k_2)$ for tone 2
0x09	$\sin(k_3)$ for tone 3
0x0a	$\cos(k_3)$ for tone 3

$k_i = \frac{2\pi f_i}{7200}$

f_i = frequency of tone i

C/S RAM Location: 0x0c. V.17 Rate Selection Word

This location is used to select the V.17 rate. There is no rate negotiation in V.17 mode, therefore only one rate must be selected by the host processor and it must be the same at both modems. Only one bit may be active at a time.

Note: This location must be set to zero when using modes other than V.17.

Host Microprocessor Interface (continued)

Bit	V.17 Rate
0	7200 bits/s
1	9600 bits/s
2	1200 bits/s
3	14400 bits/s
4	16800 bits/s
5	19200 bits/s

C/S RAM Location: 0x11. DTMF High-Frequency Power Level and Power Level for Tone 1

This value specifies the transmit power level for the DTMF high-frequency tone and also for tone 1 when a transmit tone command is issued. The units are dBm (see Transmit Level — 0x03). The default is –10 dBm.

C/S RAM Location: 0x12. DTMF Low-Frequency Power Level and Power Level for Tone 2

This value specifies the transmit power level for the DTMF low-frequency tone and also for tone 2 when a transmit tone command is issued. The units are dBm (see Transmit Level — 0x03). The default is –12 dBm.

C/S RAM Location: 0x13. Transmit Power Level for Tone 3

This location determines the transmit power level for tone 3. The units are dBm (see Transmit Level – 0x03). The default is –10 dBm.

C/S RAM Location: 0x17. Tone Duration for DTMF Dialing and Tone Generation

This value determines the duration in ms for each DTMF digit. The valid range is 0 to 4500 ms. The default is 70 ms. This value is also used by the generate tone command. For a continuous tone, the value should be set to 0.

C/S RAM Location: 0x18. Interdigit Delay for DTMF Dialing

This value determines the duration of the silent interval between DTMF digits. The units are milliseconds (ms). The valid range is 0 to 4500 ms. The default is 70 ms.

C/S RAM Location: 0x19. Make Time for Pulse Dialing

This value determines how long the relay remains closed while pulsing for pulse dialing. The units are milliseconds (ms). The valid range is 0 to 4500 ms. The default is 36 ms.

C/S RAM Location: 0x1a. Break Time for Pulse Dialing

This value determines how long the relay remains open while pulsing for pulse dialing. The units are milliseconds (ms). The valid range is 0 to 4500 ms. The default is 64 ms.

C/S RAM Location: 0x1b. Interdigit Delay for Pulse Dialing

This value determines the amount of delay between digits when pulse dialing. The units are milliseconds (ms). The valid range is 0 to 4500 ms. The default is 750 ms.

Host Microprocessor Interface (continued)

C/S RAM Location: 0x1c—0x25. Frequency Constants for Tone Detection

These locations determine the frequencies detected by the DSP in response to a detect tone command. Up to 10 frequencies may be searched for at a time. For each frequency, one constant must be stored. For frequency 1, location 0x1c contains $\cos(\theta_1)$ where $\theta_1 = \frac{2\pi f_1}{f_s}$ radians and f_1 is the frequency of the tone. The cos value must be scaled by a factor of 2^{14} or 16,384 (this is binary fraction format Q14) with the binary point immediately to the right of bit 14. For additional frequencies, cos values are stored in consecutive locations beginning at address 0x1d.

Address (hex)	Description
0x1c	$\cos(k_1)$ for tone 1
0x1d	$\cos(k_2)$ for tone 2
0x1e	$\cos(k_3)$ for tone 3
0x1f	$\cos(k_4)$ for tone 4
0x20	$\cos(k_5)$ for tone 5
0x21	$\cos(k_6)$ for tone 6
0x22	$\cos(k_7)$ for tone 7
0x23	$\cos(k_8)$ for tone 8
0x24	$\cos(k_9)$ for tone 9
0x25	$\cos(k_{10})$ for tone 10

$k_i = \frac{2\pi f_i}{7200}$

f_i = frequency of tone i

C/S RAM Location: 0x26. Receive Threshold for DTMF and Tone Detection

The units are dBm. The default value is –43 dBm. The valid range is 0 to 45 dBm with an implied minus sign.

C/S RAM Location: 0x27. Number of Tones Detected

This location contains the number of tones whose power has exceeded the tone detection threshold when a detect tones or detect DTMF command is issued.

Host Microprocessor Interface (continued)

C/S RAM Location: 0x28. Detected tones

This location indicates which tones have been detected following a detect tone or detect DTMF command. A one indicates a detection. The bits in this word are defined as follows:

Bit	Description	
	For Detect DTMF Command	For Detect Tone Command
0	DTMF high frequency 1 (1209 Hz)	Tone 1
1	DTMF high frequency 2 (1336 Hz)	Tone 2
2	DTMF high frequency 3 (1477 Hz)	Tone 3
3	DTMF high frequency 4 (1633 Hz)	Tone 4
4	DTMF low frequency 1 (697 Hz)	Tone 5
5	DTMF low frequency 2 (770 Hz)	Tone 6
6	DTMF low frequency 3 (852 Hz)	Tone 7
7	DTMF low frequency 4 (941 Hz)	Tone 8
8	—	Tone 9
9	—	Tone 10

When detecting DTMF signals, the values of the detected tones word corresponding to each DTMF digit are defined by the following tables. The table on the left shows the specific values for each DTMF digit. The table on the right relates the high and low frequencies to the actual DTMF digits and the hex values used to encode the digits.

Digit	Detected Tones Word
0	0x82
1	0x11
2	0x12
3	0x14
4	0x21
5	0x22
6	0x24
7	0x41
8	0x42
9	0x44
*	0x81
#	0x84
A	0x18
B	0x28
C	0x48
D	0x88

		High Frequency (Hz)/(Bit)			
		1209 (0)	1336 (1)	1477 (2)	1633 (3)
Low Frequency/ (Bit)	697 (4)	1	2	3	A
	770 (5)	4	5	6	B
	852 (6)	7	8	9	C
	941 (7)	*	0	#	D

Once a tone is present at the receiver, it takes up to 45 ms to detect the tone initially. When valid tone(s) are detected, the appropriate bit(s) in register 0x28 are set. Every 30 ms thereafter, each bit is updated with either a 1 if the tone is still present or a 0 if the tone has ended.

Host Microprocessor Interface (continued)

C/S RAM Location: 0x29—0x32. Detected Tone Relative Power Levels

These locations contain the relative power in 16-bit integer representation of each of the tones which are being looked for. Due to the internal AGC, there is no direct relationship between the actual received signal level and the detected tone relative power levels. These values can only be used for relative comparisons.

For example, three tone detectors can be set up 10 Hz apart and the detected tone power levels can be used to determine if the center tone was derived by the side tones (lower power level with respect to the side tones) or by itself (higher level than the side tones). This technique can be used to measure frequency offset and twist.

C/S RAM Location: 0x35. Received Rate Sequence

This location contains the first rate sequence received from the remote modem during the most recent V.32 startup or retrain. Therefore, it is likely to indicate the rates available at the remote modem, and not just the final negotiated speed. It is defined the same as register 0x1.

C/S RAM Location: 0x36. Current Line Operating Speed

This location gives the actual operating speed when in data mode (i.e., once start-up has completed) and when in a local loop test mode.

Value (hex)	Speed (bits/s)
0x0	0—300
0x1	600
0x2	1200
0x3	2400
0x4	4800
0x5	7200
0x6	9600
0x7	12000
0x8	14400
0x9	16800
0xA	19200

C/S RAM Location: 0x37. Receiver Signal Threshold Level

This location sets the off-to-on signal threshold (within ±1 dB) for all modulation modes. If the received signal falls 2—4 dB below this level, RD will be clamped to marking and the data pump RR bit will be low. The units are dBm. The valid range is 0 to 45 dBm with an offset of –6 dB and an implied minus sign. The default value is –43 dB, which corresponds to a level of –49 dBm at the codec.

Host Microprocessor Interface (continued)

C/S RAM Location: 0x38. Options Control Word

This register contains options which control the operation of the modem. The default value of each option is 0.

Bit	Description
0	**V.22 answer tone.** 0 = unscrambled marks 1 = 2225 Hz (212A compatible)
1	**V.22 550 Hz guard tone.** (Applies only to European countries.) 0 = disabled, 1 = enabled
2	**V.22 1800 Hz guard tone.** (Applies only to European countries.) 0 = disabled, 1 = enabled
3	**V.25 answer sequence in all modes.** 0 = enabled 1 = disabled (in V.32 mode, disable for 4-wire operation).
4	**V.23 mode.** 0 = originate modem transmits at 75 bits/s and receives at 600 or 1200 bits/s, answer modem transmits at 600/1200 bits/s and receives at 75 bits/s. 1 = answer modem transmits at 75 bits/s and receives at 600 or 1200 bits/s, originate modem transmits at 600/1200 bits/s and receives at 75 bits/s
5	**Transmit slave timing.** This option causes the modem's transmit timing to be slaved to the receive timing. This option must be enabled during V.54 remote digital loop. See Remote Digital Loop, page B-7. 0 = disabled, 1 = enabled
6	Reserved for future use
7	Reserved for future use
8	**Far echo canceler frequency offset compensation** (V.32 mode only). When no Δf is present, clearing this bit results in a faster start-up time (standard canceler length only). 0 = disabled, 1 = enabled
9	**Echo canceler length.** 0 = standard canceler 1 = long canceler (use only if round-trip delay is greater than 36.833 ms)
10	**Sleep mode.** 0 = disabled, 1 = enabled
11	**Scrambler/Descrambler.** V.32 and V.22 modes only. See Scrambler/Descrambler, page B-10. 0 = enabled, 1 = disabled
12	**Unscrambled binary ones (USB1) for V.22 RDL.** See Remote Digital Loop, page B-7. 0 = disabled, 1 = enabled
13	**External transmit timing.** See External Transmit Timing, page B-6. 0 = disabled, 1 = enabled
14	**Input clock frequency.** This option selects the data pump input oscillator or crystal frequency. 0 = 40.5504 MHz input clock (default) 1 = 20.2752 MHz input clock
15	**Secondary Channel.** See Secondary Channel Operation, page B-1. 0 = disabled, 1 = enabled

Host Microprocessor Interface (continued)

C/S RAM Location: 0x39. FAX Options Word

This word is used to control certain options applying to FAX modes, including V.21 channel 2 detection and echo protection tone generation. Each bit is described below.

Note: Bits 8 and 9 control compatibility options that also apply to data modes.

Bit	Description
0	**Transmit echo protection tone (EPT) @ 1700 Hz.** 0 = disabled (default) 1 = enabled Note: This option is not supported in V.17 mode.
1	**Transmit echo protection tone (EPT) @ 1800 Hz.** 0 = disabled (default) 1 = enabled
2	**Detect group 2 tones**, i.e., 462, 1100, and 2100 Hz (V.21 receive only).
3	**Fast train enable.** 0 = long train (default) 1 = fast (short) train This option is used by both the transmitter and the receiver to determine if the next train will be long or short. Note that a long train must always be done first in a given direction; afterwards, all remaining trains in that direction may be either long or short. Note that if a short train fails due to poor line conditions, the next train must be long.
8	**SD clamp option.** (This bit applies to both data and FAX modes.) 0 = SD clamped when data pump CTS is low (default) 1 = SD clamped only during start-up and retrain This allows the controller firmware to select when SD is clamped to marking.
9	**V.32bis nonstandard compatibility option.** (This bit applies to both data and FAX modes.) 0 = ignore V.32bis rate sequence bit 4 (default) 1 = do not allow V.32bis rates if bit 4 of the rate sequence is not set This option allows the data pump to start up with V.32bis modems that violate the V.32bis recommendation, by not setting rate sequence bit 4. If this option bit is 0, the data pump ignores bit 4 of the V.32bis rate sequence word.
10—11	**DP_RTS source.** Specifies the source for the DP_RTS logic. See Figure MJ-4, page MJ-45. 00 = DP_RTS is EIA_RTS or H_RTS. (default) 01 = DP_RTS is EIA_RTS. 10 = DP_RTS is H_RTS. 11 = reserved. Specify EIA_RTS as the source for DP_RTS to control the RTS logic via the hardware signal. To operate the RTS logic using the host controller, specify H_RTS as the source for DP_RTS. The default option of EIA_RTS or H_RTS is the manner in which earlier ROM codes operated; use this option for backward compatibility.
12	**Codec type select.** Specifies whether a T7525 codec or a CSP1027 codec is being used. 0 = T7525 codec. (default) 1 = CSP1027 codec.

Host Microprocessor Interface (continued)

C/S RAM Location: 0x3a. Operating Status Word

This location contains status information which is likely to be needed by the host processor on a regular basis. By default, this location is written periodically to mailboxes 0x0a—0x0b. See C/S RAM location 0x3c. The following table summarizes the contents.

Bit	Description
0	**Clear down sequence detected** (V.32 only). This bit is set when a clear down sequence has been detected and when a clear down command is received. The bit is cleared when the next start-up command is received.
1	**Retrain sequence detected.** Set when a retrain sequence is detected and is cleared at the end of the retrain procedure.
2	**Startup in progress.** Set at the beginning of a start-up or retrain procedure and is cleared at the end.
3	**Data mode.** Set once start-up or retrain handshaking has completed and is cleared either at the beginning of a retrain or when a disconnect occurs.
4	**Dialing not ready.** This bit is set while dialing or generating tones to let the host processor know when the DSP has completed the operation. A zero indicates that the DSP is ready, and a 1, that the DSP is not finished.
5	**Ring detect valid.** This bit indicates the presence of a valid ringing signal as specified by the ring period limits in words 0x40 and 0x41.
6*	**Send data (SD) mark status activity indicator.** When set, this bit indicates that at least one mark has occurred in the send data input since the last time the status word was read using command 5. (Command 5 returns the status word and clears the SD and RD mark and space status bits.)
7*	**Send data (SD) space status activity indicator.** When set, this bit indicates that at least one space has occurred in the send data input since the last time the status word was read using command 5. This bit, together with bit 6, indicates the presence or absence of SD activity. If both bits are set, at least one change of state in the SD input has occurred. If only one bit is set, the input was constant (no activity) in either the mark or space condition since the last time that status was read.
8*	**Receive data (RD) mark status activity indicator.** When set, this bit indicates that at least one mark has occurred in the receive data output since the last time the status word was read using command 5.
9*	**Receive data (RD) space activity indicator.** When set, this bit indicates that at least one space has occurred in the receive data output since the last time the status word was read using command 5. This bit, together with bit 8, indicates the presence or absence of RD activity.
10	**V.22 remote digital loop (RDL) request detected.** When set, this bit indicates that the V.22 RDL request signal has been received from the remote modem.
11	**Mean squared error OR echo correlator status.** This status bit is set when either the mean squared error level passes a programmable threshold (CS RAM 0xb) or the echo correlator exceeds the fixed threshold of 900. See On-Line Monitoring, page MJ-57.
12	**Energy detected in IIR filter 1.** When set, indicates the presence of energy above the threshold level specified. See Programmable IIR Filters, page B-11.
13	**Energy detected in IIR filter 2.** When set, indicates the presence of energy above the threshold level specified. See Programmable IIR Filters, page B-11.
14	**V.32bis rate renegotiation sequence detected.** When set, this bit indicates that a V.32bis rate renegotiaion sequence has been detected. This bit remains set after the renegotiation has been completed. The host may clear this bit by performing a read/modify/write operation on this word.

* Host command 5 must be used to read these bits.

Host Microprocessor Interface (continued)

C/S RAM Location: 0x3b. Automode Status Reporting (Data Modes Only)

When in data mode, this location contains information about the current mode of the data pump. This information is useful for determining the mode in use after an automode start-up. The following table lists the values that will be present in this location during various modes of operation. See Automode Operation, page B-twelve, for more information on intermediate states.

Mode	Value (Originate)	Value (Answer)
V.32	0x02 or 0x08	0x82 or 0x87
V.22bis	0x13	0x88
V.22 or Bell 212A	0x11	0x89
V.23	0x09	0x86
V.21	0x10	0x85
Bell 103	0x12	0x90

C/S RAM Location: 0x3b. FAX Status Word (V.29, V.27ter, and V.21 Ch 2 FAX Modes Only)

This word is used to report the current status of the transmitter and receiver during FAX operation. The high byte and low bytes are defined separately. The values that may appear in the low byte of the FAX status word differ for transmit and receive modes. Here is a complete list of possible values:

Word Bits								Mode	Description
7	6	5	4	3	2	1	0		
0	0	0	0	0	0	0	1	Receive only	Silence
0	0	1	1	0	0	1	0		Detection of AB sequence
0	1	1	1	0	0	1	1		Detection of CD sequence
0	1	1	1	0	1	0	0		Scrambled ones
1	1	1	1	0	1	0	1		Facsimile data mode
0	0	0	1	0	0	0	1	Transmit only	Transmit Silence
0	0	0	1	0	0	1	0		Transmit AB sequence
0	0	0	1	0	0	1	1		Transmit CD sequence
0	0	0	1	0	1	0	0		Transmit scrambled ones
0	0	0	1	0	1	0	1		Facsimile data mode
0	0	1	1	0	1	1	1		Transmit EPT at selected frequency

Host Microprocessor Interface (continued)

The high byte of the FAX status word indicates the current FAX speed, training type, and EPT detection.

The format of this word is:

Bits:	15—13	12	11	10—8
Field:	STD	FB	V21D	EPT/TD

where:

STD — FAX standard
FB — Fallback
V21D — V.21 detected
EPT/DT — EPT or tone detected

Word Bits								Description
15	14	13	12	11	10	9	8	
0	0	0	0	0	0	0	0	V.29 9600 bits/s
0	0	0	1	0	0	0	0	V.29 7200 bits/s
0	0	1	0	0	0	0	0	V.27ter 4800 bits/s
0	0	1	1	0	0	0	0	V.27ter 2400 bits/s
0	0	0	0	1	0	0	0	V.29 9600 bits/s. Detected V21
0	0	0	1	1	0	0	0	V.29 7200 bits/s. Detected V21
0	0	1	0	1	0	0	0	V.27ter 4800 bits/s. Detected V21
0	0	1	1	1	0	0	0	V.27ter 2400 bits/s. Detected V21
0	0	0	0	0	0	1	0	V.29 9600 bits/s. EPT @ 1700 Hz
0	0	0	1	0	0	1	0	V.29 7200 bits/s. EPT @ 1700 Hz
0	0	1	0	0	1	0	0	V.27ter 4800 bits/s. EPT @ 1800 Hz
0	0	1	1	0	1	0	0	V.27ter 2400 bits/s. EPT @ 1800 Hz
0	0	0	0	0	1	0	0	V.29 9600 bits/s. EPT @ 1800 Hz
0	0	0	1	0	1	0	0	V.29 7200 bits/s. EPT @ 1800 Hz
0	0	1	0	0	0	1	0	V.27ter 4800 bits/s. EPT @ 1700 Hz
0	0	1	1	0	0	1	0	V.27ter 2400 bits/s. EPT @ 1700 Hz
0	1	0	0	0	0	0	0	V.21 ch2 300 bits/s
0	1	0	0	0	0	0	1	V.21 ch2 300 bits/s. Detected 462 Hz
0	1	0	0	0	0	1	0	V.21 ch2 300 bits/s. Detected 1100 Hz
0	1	0	0	0	1	0	0	V.21 ch2 300 bits/s. Detected 2100 Hz
1	0	0	0	0	0	0	0	V.17 mode
1	0	0	0	0	1	0	0	V.17 mode. EPT @ 1800 Hz
1	0	0	0	1	0	0	0	V.17 mode. Detected V.21

C/S RAM Location: 0x3c. Address for Fast Status to Mailboxes A and B

This location contains the address of one 16-bit control and status RAM location which is copied periodically to host mailboxes 0xA and 0xB. (The update period depends on the current operating mode. See Status Information, page MJ-19, for details.) Mailboxes 0xA and 0xB contain the low byte and high byte, respectively, of the RAM location's contents. The default is the operational status word RAM location 0x3a.

Host Microprocessor Interface (continued)

C/S RAM Location: 0x3d. HDLC Options Control Word

This word is used to monitor and control parallel data mode and Voice-Thru mode. Bits 0—8 are used to control the parallel data mode. Bit 15 provides a status indicating whether Voice mode is currently in use. Bit 14 is used during Voice mode to enable or disable the transmit data paths.

Bit	R/W	Description
0	R/W	**Stop Bits.** Number of stop bits per character. 0 = 1 bit 1 = 2 bits
1—2	R/W	**Data Bits.** Number of data bits per character. 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits
6—7	R/W	**Mode.** 00 = reserved 01 = reserved 10 = asynchronous mode 11 = reserved
8	R/W	**Parallel data mode enable.** 0 = disabled 1 = enabled Note: Bits 0—7 are ignored when parallel data mode is disabled. In this case, asynchronous mode is controlled through host register 0x2c.
9—13	R	**Reserved.** Do not alter the state of these bits. When writing to this register, perform a read/modify/write operation, altering the values of only those bits necessary.
14	R/W	**Transmit data enable.** When set, transmit data is passed through to the codec for output. When cleared, nothing is output by the codec. Note: Since there is no echo cancellation in use while Voice-thru mode is active, it is recommended that transmit data only be enabled while actually transmitting.
15	R	**Voice-thru mode status.** When set, the data pump is in Voice-thru mode. This bit is zero in all other modes.

C/S RAM Location: 0x3e. Total In-Band Energy Level

This is the level of the total in-band energy. Units are dB relative to a codec input level of –6 dBm. The upper byte represents integer dB and the lower byte fractional dB. For a level 10.5 dB below the maximum (i.e., –16.5 dBm), a value of 0xa80 is returned. The minus sign is implied. This parameter is accurate to ±1 dB and is only valid when detecting tones or DTMF digits before a start-up.

C/S RAM Location: 0x3f. Transmit Mute

When this location is set to a value of 1, the transmit output in V.32 and V.22bis modes is muted (symbols are set to 0). When set to 0 (default), the transmitter operates normally.

C/S RAM Location: 0x40. Ring Detect Period Lower Limit

Location 0x40 contains the lower limit of the ring detect period which corresponds to the upper limit of the ring detect frequency. The units are 0.833 ms. For example, for 68 Hz, the period is 14.7 ms. Therefore, the value written to RAM location 0x40 would be $\frac{14.7}{.833\ ms} = 0x12$. This is also the default value.

Host Microprocessor Interface (continued)

To allow deglitching, RI is not set until a programmable number of valid ringing cycles (within the user-supplied upper and lower limits) are detected (C/S RAM location 0x43). The overall frequency range is 0 to 200 Hz.

Ring detect frequency resolution varies with frequency. The following formula gives the resolution as a function of frequency:

$$\Delta f = f\left(1 - \frac{1}{1 + T_s f}\right)$$

where

f is the frequency of interest,
Δf is the frequency resolution,
T_s is the sampling period, and
$T_s = \frac{1}{1200\ Hz} = .833\ ms.$

For example, here are the corresponding values of Δf for several frequencies:

f (Hz)	Δf (Hz)
15	.18
40	1.28
65	3.3

C/S RAM Location: 0x41. Ring Detect Period Upper Limit

This location contains the upper limit of the ring detect period which corresponds to the lower limit of the ring detect frequency. The units are 0.833 ms. For example, for 15 Hz, the period is 66 ms. Therefore, the value written to RAM location 0x41 would be $\frac{66}{.833\ ms} = 0x50$. This is also the default value.

C/S RAM Location: 0x42. Answer Mode Silent Interval Duration

This location determines the duration of the answer mode silent interval. The units are multiples of .416 ms (1/2400). The default is 4800 which corresponds to 2 seconds. Typically, this value should either be left at the default setting or set to 0 in the event that the host processor is to perform the timing.

C/S RAM Location: 0x43. Ring Detect Cycle Counter

Number of valid/invalid ringing cycles to enable/disable RI. The default value of 5 was found to provide very good deglitching. A smaller value should only be used in a country where the ringing pulse duration is less than $5 \cdot \frac{1}{f}$, where f is the ringing frequency.

C/S RAM Location: 0x44. Echo Correlator Level

The echo correlator compares the signal at the input to the receiver with an estimate of the near and far transmit echo. The output of the echo correlator is read at this location. A value larger than 900 indicates that correlation is detected. This condition also causes status bit 11 of the Operating Status Word (C/S RAM 0x3a) to be set. See On-Line Monitoring, page MJ-57, for additional information.

C/S RAM Location: 0x48. Drop Out Timeout

This parameter determines how long the modem will attempt to bridge a carrier drop out when in V.32 and V.32bis data modes or when in V.27, V.29, or V.17 FAX modes. The value depends on the symbol rate (SR) which is mode dependent.

Host Microprocessor Interface (continued)

Mode	Symbol Rate (SR)
V.32, V.32bis, V.17, V.29	2400
V.27 4800 bits/s	1600
V.27 2400 bits/s	1200

The number must be negative and is expressed as:

$$value = -D \cdot SR$$

where D is the desired delay in seconds. The default value is –4800 (0xed40) which corresponds to 2 seconds for all modes except V.27. In the FAX modes, the receiver will return to the FAX idle state once a carrier drop out exceeds the duration of this timeout.

C/S RAM Location: 0x49. Program Memory Checksum

This location contains the checksum computed in response to a "check DSP program memory" command.

C/S RAM Location: 0x4a. Receive Signal Level

This location gives the measured level of the receive signal in data mode for all modulation modes. Units are dB relative to a codec input level of –6 dBm. The upper byte represents integer dB and the lower byte fractional dB. For a level 10.5 dB below the maximum (i.e., –16.5 dBm), a value of 0x0a80 is returned. The minus sign is implied. The receive signal level is accurate to ±2 dB.

C/S RAM Location: 0x4b. Receive Error Squared

This location provides the square of the error between the received constellation point and the decision point. The value is updated each baud interval. This parameter is valid in V.32, V.22bis, and V.22 modes.

C/S RAM Location: 0x4c. Receive Mean Square Error

This location provides an average of the squared error between the received constellation point and the decision point. This parameter can be used to estimate the signal to noise ratio (SNR) and the probable bit error rate when the channel impairment is white noise. For other impairments, the estimate is somewhat more uncertain. This parameter is valid in V.32terbo, V.32bis, V32, V.22bis, and V.22 modes.

In order to provide more useful information when using V.32terbo modes, the MSE calculation algorithm has been enhanced in this version of the data pump, by providing a host programmable scale factor and averaging time constant. The default values for each of these parameters causes the MSE to be calculated as in previous releases of the data pump.

The scale factor, stored in C/S RAM location 0x4c, can be set as follows:

Value	Result
0	Normal (default)
–1	×2 — Scale by factor of 2.
–2	×4 — Scale by factor of 4.

Host Microprocessor Interface (continued)

The averaging time constant, stored in C/S RAM location 0x51 can be set as follows:

Value	Time Constant (τ) *
0	†
–1	0.2 s (500 baud)
–2	0.4 s (1000 baud)
–3	0.8 s (2000 baud)
–4	1.6 s (3000 baud)

* The times in seconds listed here assume a baud rate of 2400.

† This case is used only for compatibility with earlier releases.

When the time constant is set to 0, the MSE value is computed using single precision to maintain compatibility with earlier data pump releases. For other values, double precision is used. Double precision should always be used for V.32terbo modes. It is also suggested for lower-speed rates, although for existing designs this will require new fall-back and fall-forward MSE thresholds to be established. After a change in line conditions, the value of MSE approaches a new value over a period of 3τ.

C/S RAM Location: 0x4d. Receive Peak Squared Error

This location provides the peak of the squared error between the received constellation point and the decision point since the last time that this location was read and cleared. The peak value is cleared immediately following each read of this location using command 0x0d. This parameter is valid in V.32, V.22bis, and V.22 modes.

C/S RAM Location: 0x4e. RMSE Scale Factor

This location holds a scale factor used in calculating the receive mean squared error. See description of C/S RAM location 0x4c. Valid values for this location are 0, –1, or –2. The default value is 0.

C/S RAM Location: 0x51. RMSE Time Constant

This location holds an averaging time constant used in calculating the receive mean squared error. See description of C/S RAM location 0x4c. Valid values for this location are 0, –1, –2, –3, or –4. The default value is 0.

C/S RAM Location: 0x54. Round Trip Delay

This location contains the measured round trip delay which is used by the far echo canceler. Units are ms. This parameter is valid in V.32 modes only.

C/S RAM Location: 0x55. Near Echo Level

This location contains the measured level of the near echo. Units are dBm. This parameter is valid in V.32 modes only and is accurate to ±1 dB.

C/S RAM Location: 0x56. Far Echo Level

This location contains the measured level of the far echo. Units are dBm. This parameter is valid in V.32 modes only and is accurate to ±1 dB.

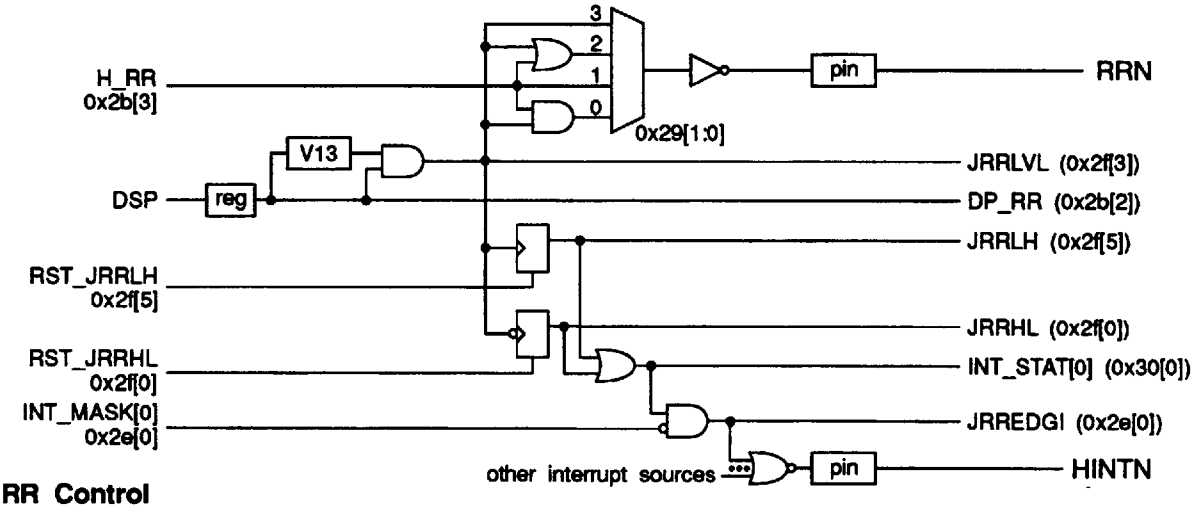
Design Information

V.24 Interface Description

The data pump contains a group of 11 pins that make up a V.24 compatible interface. These pins provide the timing (STN, RTN, XTCLK), control (RTSN, CTSN, DSRN, DTRN, RIN, RRN), and data (TXD, RXD) signals required for implementing the V.24 compatible interface. Signal names ending in *N*, e.g., RTSN, are defined as active-low. Most EIA control and timing signals are active-low at the data pump I/O pins. In the following sections, the internal, active-high versions of these signals are discussed (to differentiate, the *N* is left off the signal names). Figures MJ-4, MJ-5, and MJ-6 depict how these signals are used by the data pump and also how their functions can be controlled by the host processor.

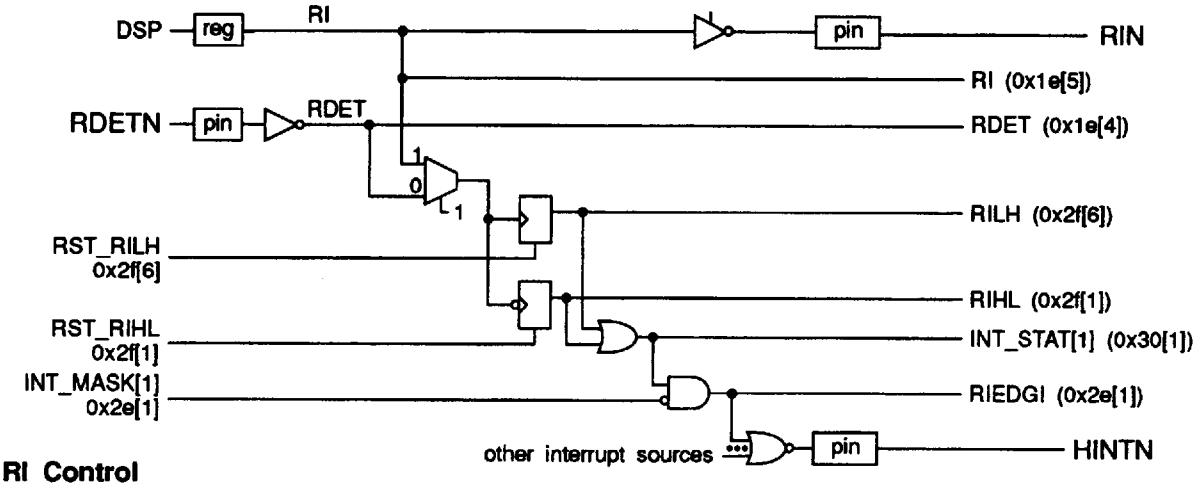
Control Signals

The data pump allows the host a great deal of flexibility in using the V.24 control signals. Figure MJ-4 illustrates this control. Asserting RTS (Request To Send) will cause the data pump to assert CTS (Clear To Send) once start-up has completed. By default, the data pump will assert CTS some period after the RTS signal is asserted.



A. RR Control

B. DTR Control



C. RI Control

Figure MJ-4. V.24 Control Signal Logic

Design Information (continued)

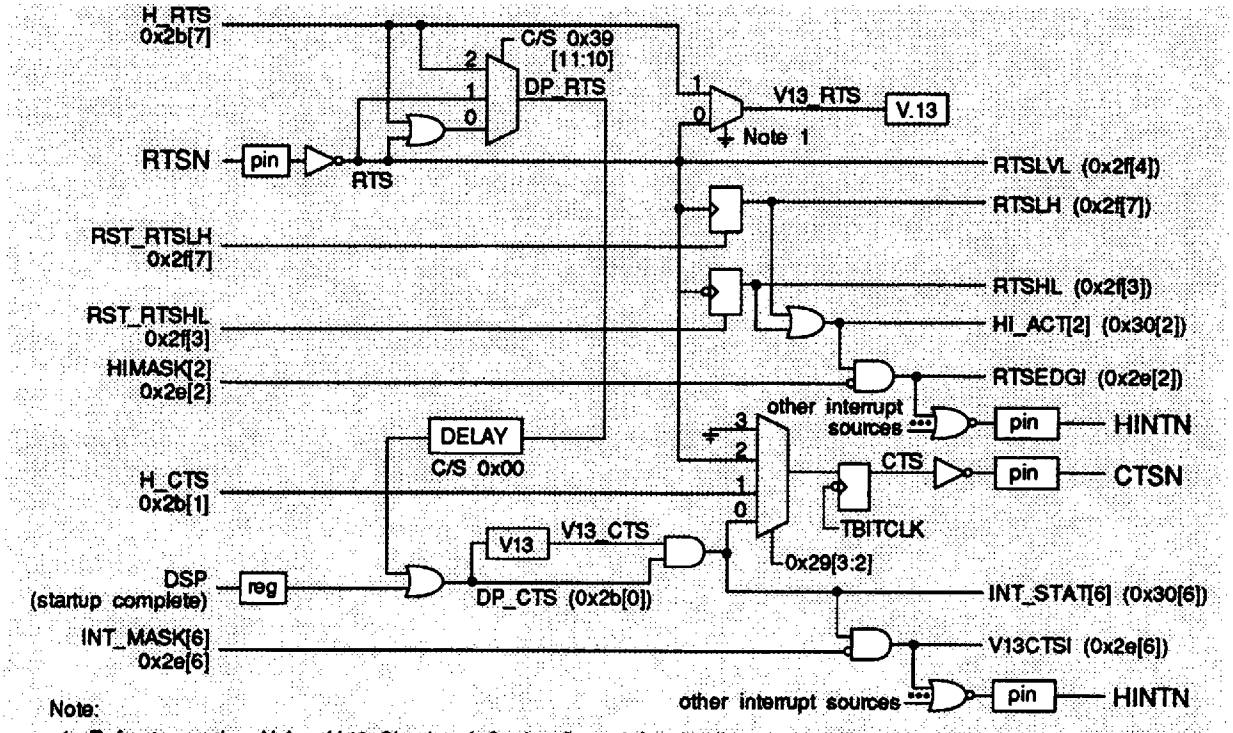
This period is defined by Control and Status RAM location 0x00. The host may optionally gate RTS directly to CTS, control CTS through the host interface (register 0x2b), or tie CTS high. This control is accomplished through register 0x29. CTS, by default, is used by the data pump to gate transmit data (see Data Signals section for more options).

DSR (Data Set Ready) indicates that the modem is ready to transfer data. The data pump, by default, sets DSR at the appropriate times as defined by each modem standard. The host may optionally control it through the H_DSR (Host DSR) bit of register 0x2b, or allow it to be an AND or OR function of H_DSR and the data pump's DSR (DP_DSR).

DTR (Data Terminal Ready) is simply latched in register 0x2B. It is not used in any other way by the data pump, but its status can be used by the host to initiate its own defined event such as a disconnect.

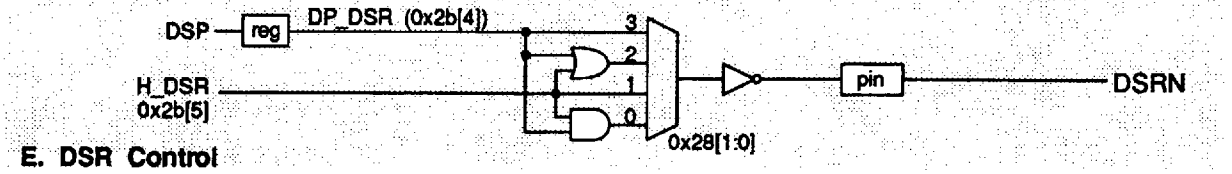
RI (Ring Indicator) is controlled by the data pump, and indicates that valid ring has been detected. Its value may also be read at bit 5 of register 1E. This is the same indication that can be monitored in bit 5 of C/S RAM location 0x3a. This indicates the presence of a valid ringing signal as specified by the ring period limits in C/S RAM locations 0x40 and 0x41.

RR (Receiver Ready) indicates, by default, that the data pump has detected carrier. It is asserted after start-up and will go off during retrain. The host may modify this functionality by selecting one of the other options available in register 0x29 (RRCB). The host may select to control RR directly through H_RR (Host RR) of register 0x2B, or allow it to be an AND or OR function of H_RR and the data pump's RR (DP_RR).



Note:
1. Refer to section Using V.13 Simulated Carrier Control for details on controlling this MUX.

D. RTS and CTS Control



E. DSR Control

Figure MJ-4. V.24 Control Signal Logic (continued)

Design Information (continued)

Timing Signals

The host's control of the timing signals is illustrated in Figure MJ-5. The data pump provides two synchronous clocks, RTN (Receive Timing) and STN (Send Timing), for USART timing. RTN and STN, by default, represent the data pump generated RBITCK (Receive Bit Clock) and TBITCK (Transmit Bit Clock). Optionally, the host may gate XTCLK (External Clock) or USRCLK (User Clock) onto either STN or RTN. These signals may also be individually inverted or forced to high impedance. This control is defined in register 0x2A. XTCLK would be provided by the V.24 input, while USRCLK is generated by the data pump and may be programmed using registers 0x12 and 0x13.

Data Signals

Figure MJ-6 illustrates the V.24 data path. In the standard (default) mode of operation, the data pump's MRD (Modem Receive data) is gated with DP_RR (carrier detect) to yield RXD (Receive Data). The host may enable the sync to async converter using register 0x2C. Other basic options include clamping RxD high or low, or gating TXD to RXD as part of local digital loop. These options are enabled using register 0x29.

TXD operates in much the same way. It is normally (by default) gated directly to the data pump's MSD (Modem Send Data). It may be passed through the async to sync converter using register 0x2C, and, by default, MSD is gated with CTS before being transmitted. It may optionally be gated with RTS or be enabled all the time using register 0x28, field MSDCB. As part of remote digital loop support, the host can direct the data pump to connect MRD to MSD using the MSDCB field.

Additional data sources and destinations are available for increased flexibility and functionality. A simple UART is available which can be gated either to the MSD path or to RXD. This gives the host the ability to directly interface to either the DCE (remote modem) or DTE (V.24 interface). This is done using MSDCB of register 0x28 and RxDCB of register 0x29.

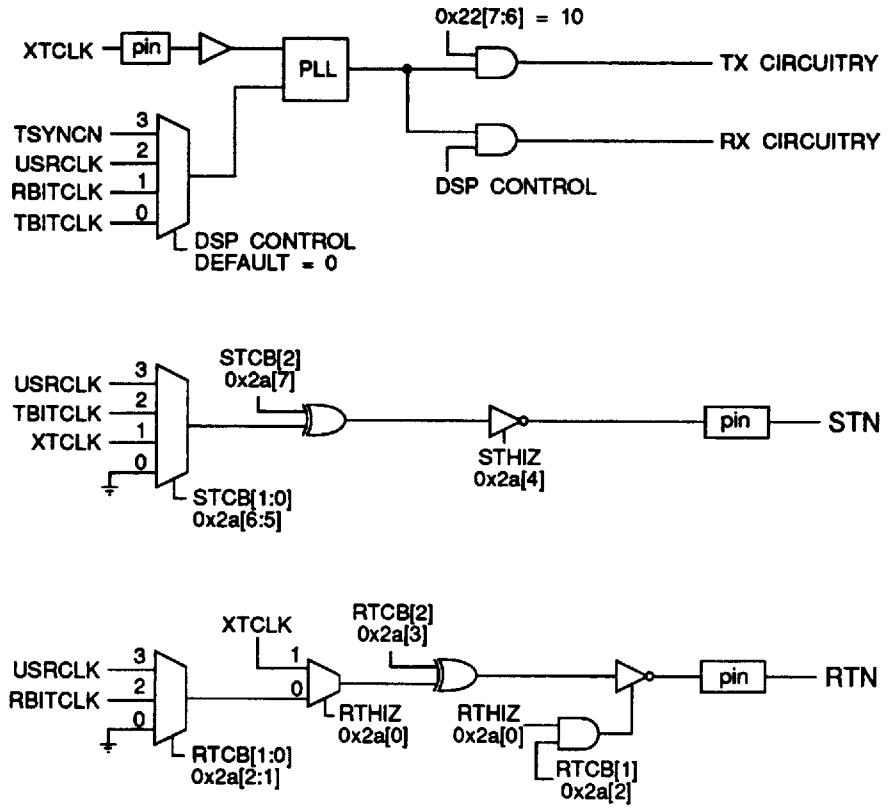


Figure MJ-5. V.24 Timing Control

Design Information (continued)

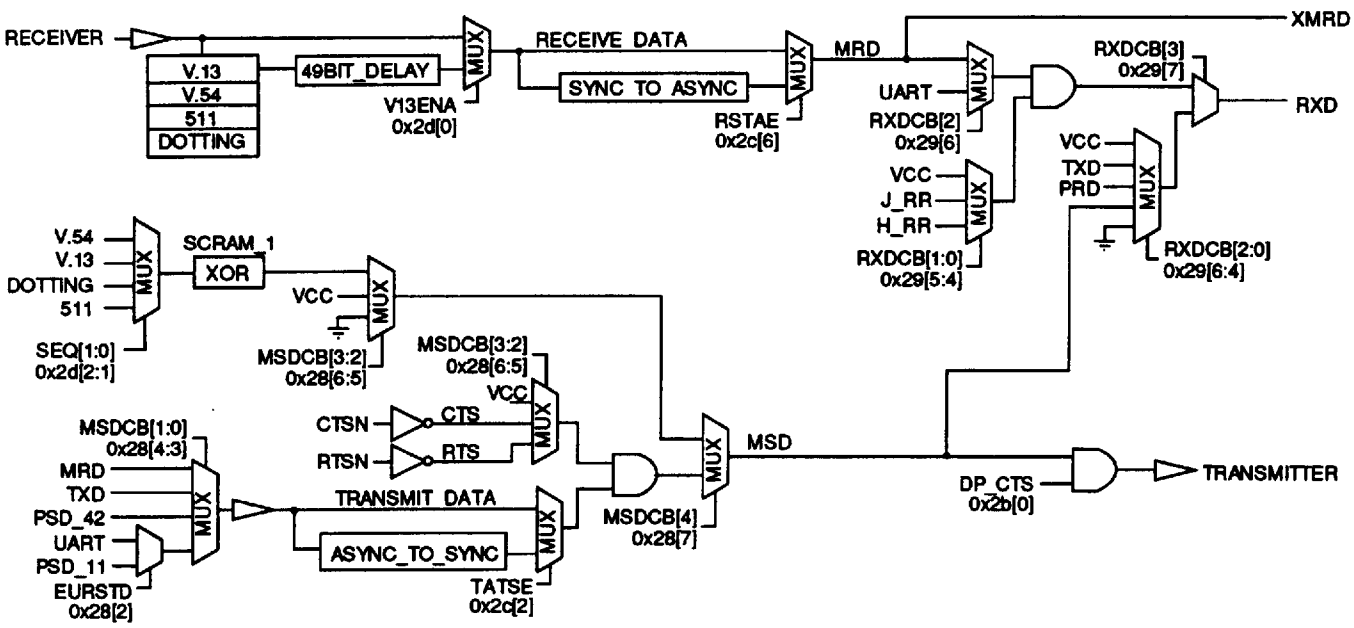


Figure MJ-6. EIA Data Path Control

V.42 Signals

The data pump provides three additional signals that are used to support V.42 mode. The V.42 data path is illustrated in Figure MJ-7. In this configuration, the DTE's TXD comes into RXDA of the host's channel A USART. It is processed and transmitted out TXDB of the host's channel B USART onto PSD. PSD can be gated onto MSD (using the MSDCB field of register 0x28) for transmission. In this case, the host has the ability to switch between PSD (when in V.42 mode) or TXD (when in a synchronous mode) without external glue logic. For the receive path, XMRD (external MRD) can be tied to RXDB of the host's channel B USART for processing. The processed data is transmitted out of TXDA of the host's channel A USART onto the data pump's PRD (Processor Receive Data). PRD can then be gated directly onto RXD using the RXDCB field of register 0x29. Again, the host may choose between MRD and PRD as RXD without any external logic.

Accessing the PSD and PRD Signals

In the multiplexed bus mode, the PSD and PRD signals are available on V32-INTFC pins 42 and 43, respectively, of the 68-pin PLCC package and pins 50 and 51, respectively, of the 84-pin PQFP package. To enable PSD, set host register 0x28 bits MSDCB[1:0] to 10. To enable PRD, set host register 0x29 bits RXDCB[3:0] to 101x.

In nonmultiplexed bus modes, PSD and PRD are shared with DSPCKI (default) and RI (default), respectively. These signals are present on pins 11 and 52, respectively, of the 68-pin PLCC package and pins 15 and 64, respectively, of the 84-pin PQFP package. To enable PSD, set host register 0x28 bits MSDCB[1:0] to 01. The procedure for enabling PRD (with RI no longer available) and RBITCLK depends of the configuration of the data pump.

Design Information (continued)

The following configurations are possible:

Bus Mode	Clock Option	
	1X Clock	2X Clock
Nonmux'd, general	0x59	0x49
Nonmux'd, Motorola	0x79	0x69
Nonmux'd, Rockwell	0x99	0x09

To enable PRD, perform the following steps:

1. Write value from above list to register 0x06.
2. Write 0x00 to register 0x07.
3. Write 0x2c to register 0x08.
4. Write 0x3 to register 0x09.
5. Wait for CRBNKI to indicate that the data pump has read the command. Clear CRBNKI.

Finally, set host register 0x29 bits RXDCB[3:0] to 101x and PRD will be enabled.

Note: When using PRD on pin 52 of the PLCC package or pin 64 of the PQFP package, a 50 Ω resistor should be placed in series between the PRD input and the source driving the PRD signal. This is necessary, since before issuing the above command, this pin is an output (RIN).

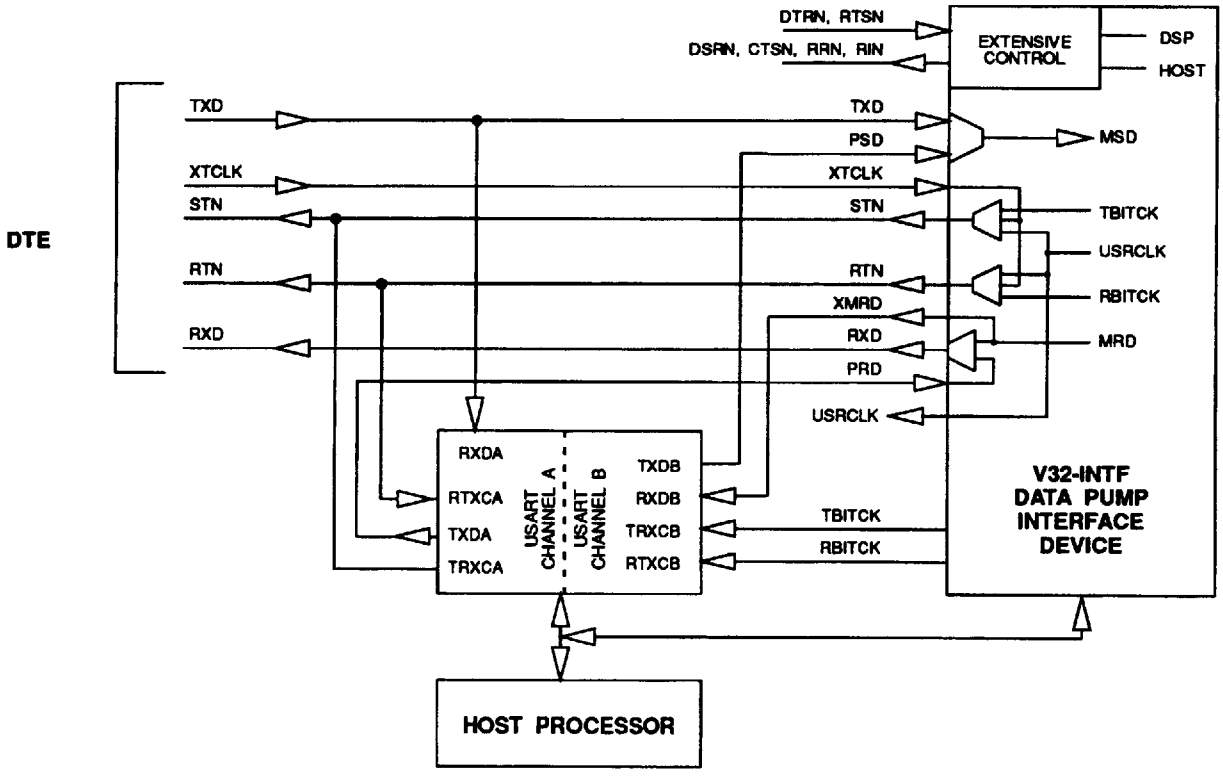


Figure MJ-7. V.42 Data and Timing Configuration

Design Information (continued)

Using FAX Modes

The use of the various FAX modes is discussed in the following sections.

V.29, V.27ter, and V.21 Channel 2 FAX Modes

The following sections describe the use of the receiver and transmitter in these FAX modes. For V.17 mode operation, refer to the following section.

Receiver Control

There are many parameters that affect the operation of the receiver. Most are used the same as when operating in a data mode (V.32, etc). The general procedure is to set those parameters that specify the mode and control the general operation of the modem, and then issue a start-up command (in receive mode).

The parameters that must be set before issuing the start-up command are the rate selection word and the receive signal threshold level. Parameters controlling optional features, such as Group 2 tone reception, should also be set before issuing the start-up command. Note that each of these parameters has a default value that may be acceptable for some applications.

During high-speed FAX reception (i.e., V.29, V.27ter), the receiver is continuously looking for a V.21 signal. The FAX status word reflects the results of this detection. During V.21 channel 2 reception, the modem can be set to detect Group 2 tones at 462 Hz, 1100 Hz, and 2100 Hz. To enable this option, set bit 2 of the FAX options word. The FAX status word will indicate any detected tones.

Transmitter Control

There are many parameters that affect the operation of the transmitter. Most are used the same as when operating in a data mode (V.32, etc). The general procedure is to set those parameters that specify the mode and control the general operation of the modem, and then issue a start-up command (in transmit mode).

The parameters that must be set before issuing the start-up command are the rate selection word and the transmit level. If echo protection tones (EPT) are to be transmitted, this option should be selected in the FAX options word before issuing the start-up command. Note that each of these parameters has a specific default value that may be acceptable for some applications.

In order for the transmitter to operate, either the H_RTS bit of register 0x2b or the RTS pin of the V.24 interface must be active. The FAX status word indicates the current status of the transmitter during operation.

V.17 FAX Mode

For other FAX modes (i.e., V.29, V.27, and V.21), a parameter is included with the start-up command that indicates whether transmit or receive mode is desired. This parameter is ignored for start-ups in V.17 mode. In V.17 mode, the data pump monitors DP_RTS and received carrier and enters the appropriate mode depending on which is active. Therefore, in order to switch the direction of transmission (turn the line around), it is necessary only to lower DP_RTS at one end and raise DP_RTS at the other end.

Note: Previous ROM codes (prior to ME) required that the EIA RTS pin be inactive while operating as a receiver in V.17 FAX modes. The MG ROM code includes two new control bits in C/S RAM location 0x39 that allow the source of the internal data pump RTS signal (DP_RTS) to be selected from the following choices:

- the EIA_RTS pin
- the H_RTS control bit
- OR function of the EIA_RTS pin and the H_RTS control bit (default selection)

Refer to the description of C/S RAM location 0x39 on page MJ-37 for detailed information.

C/S RAM location 0x0c is used to select the V.17 rate. There is no rate negotiation within V.17 mode. Therefore, one rate must be selected by the host processor and it must be selected the same at both modems.

Design Information (continued)

Using Parallel Data Transfer Mode

Note: Parallel data transfer mode is available only in V.23, V.21, and Bell 103 modes. For all other modes, including V.21 ch 2 FAX mode, the internal USART should be used.

Parallel data mode and asynchronous operation are controlled using C/S RAM location 0x3d. Parallel data transfers are performed using the host mailboxes and one previously unused host register. The use of these registers allows up to six bytes to be transferred at a time in each direction.

Transmit Data

A transmit data transfer from the host processor to the data pump is initiated using a command from the host processor. The format of the command is shown below. Byte 1 is transmitted first and bit 0 of each byte is transmitted first in time.

Table MJ-6. Transmit Data Command Format

Host Register	Description
0x2	Transmit byte 1
0x3	Transmit byte 2
0x4	Transmit byte 3
0x5	Transmit byte 4
0x6	Transmit byte 5
0x7	Transmit byte 6
0x9	Transmit data command byte

In the transmit command byte, bit 7 is set to distinguish this command from all other commands. This allows other bits in the command byte to be used to convey information. Up to six bytes may be transferred. The actual number of bytes is set in the Tx byte count field of the transmit command byte, defined below.

Prior to issuing a transmit data command, the host must wait for the transmit data buffer ready (TDBR) flag to be set (register 0x1f, bit 7). When set, this flag indicates that the internal transmit data buffer is ready to accept up to 6 additional bytes. Once the host processor sees TDBR set, it must clear the bit before issuing a transmit data command. Bit 3 of host register 0x1f is a transmit buffer under run indicator. When set, it indicates that the host processor did not provide transmit data at a sufficient rate and that the internal buffer emptied. When this occurs, marking is transmitted. The under run flag is cleared by the data pump once the data pump receives the next transmit data command.

Table MJ-7. Transmit Data Command Byte

Bit	Definition
7—4	Must be set to 0x8
3	Reserved (set to 0).
2—0	Tx byte count. (0—6)

Transmit Data Interrupt

If desired, an interrupt can be generated when a TDBR condition occurs. This condition shares an interrupt status bit with UART receive (Rx2ND_IQ) and UART transmit (Tx2ND_IQ). Enabling the TDBR interrupt is a two step process. First, a mask value must be written to the interrupt mask control register (0x2e) to enable the combined UART/TDBR interrupt. The mask value written contains 0's for those interrupts to be enabled and 1's for those to be disabled. To enable the TDBR interrupt, clear bit 7 of register 0x2e. Second, the TDBR condition must be enabled as a source for this interrupt. To do this, set bit 4 of register 0x1f.

Once an interrupt occurs, the host must first read register 0x2e to determine the source of the interrupt. Bit 7 of register 0x1f should be cleared prior to issuing the transmit data command. After processing the interrupt, bit 7 of register 0x2e must be also cleared by the host. Figure MJ-8 depicts this decision process.

Receive Data

Receive data transfers from the data pump to the host are initiated by the data pump. Up to six bytes will be transferred at a time.

Once the data pump has data to transfer, it waits for the host to read the previous data or command response from the mail boxes and then writes the data. This is an unsolicited transfer, since the host does not explicitly request the data with a command. All six mailbox locations are used for data, so registers 0xa and 0xb do not contain fast access information during a receive data transfer. This is explained below. Status relating to asynchronous mode is written to register 0x17.

Design Information (continued)

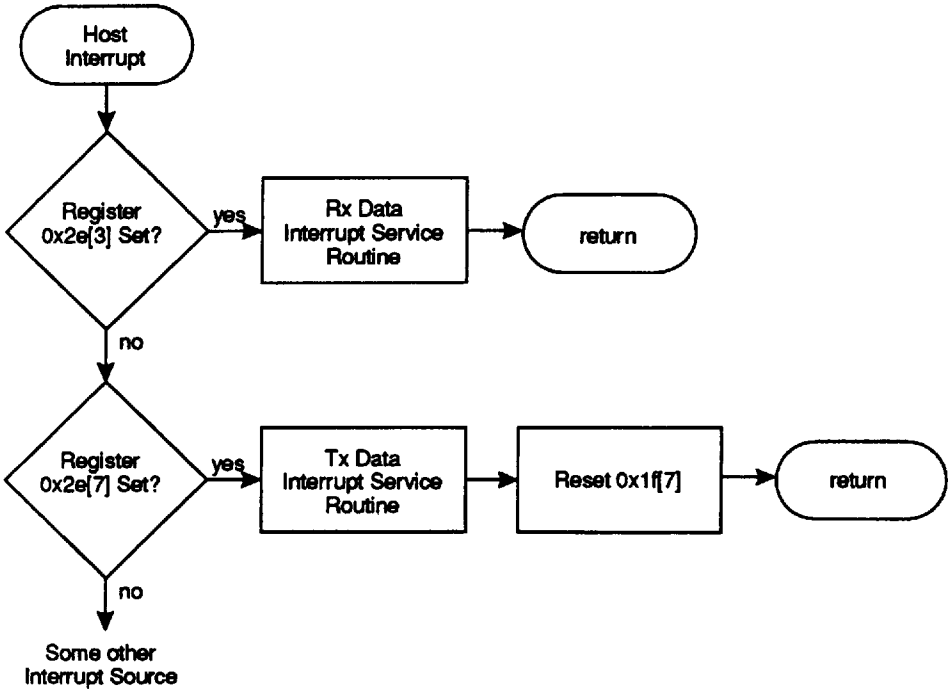


Figure MJ-8. Host Interrupt Processing

While in parallel data transfer mode, it is necessary for the data pump to be able to receive and respond to other commands, such as "read DSP RAM." Since the location 0xf normally contains the response code for commands, a mechanism is needed for the host to distinguish between an unsolicited receive data transfer and a command response. Bit 7 of register 0x17 indicates the type of data contained in registers 0xa—0xf. A value of 0 indicates that fast access information is in registers 0xa and 0xb and that registers 0xc—0xf may contain a command response. A value of 1 indicates a receive data transfer.

Bit 0 of host register 0x1f is a receive data over run indicator. When set, it indicates that the host did not read the receive data at a sufficient rate, allowing the internal receive buffer to overflow. Once the host sees that the receive data over run indicator is set, the host must clear this bit in order to detect another over run.

An interrupt can be generated whenever the data pump writes to register 0xf. Therefore, receive data transfers and command responses can generate an interrupt. This interrupt is enabled by setting bit 3 of host register 0x2e.

Table MJ-8. Receive Data Format

Host Register	Description
0xa	Receive byte 1
0xb	Receive byte 2
0xc	Receive byte 3
0xd	Receive byte 4
0xe	Receive byte 5
0xf	Receive byte 6
0x17	Status

Table MJ-9. Receive Data Format

Bit	Definition
7	Indicates the type of data contained in registers 0xa—0xf. 0 = fast access/command response 1 = receive data transfer
2—0	Receive byte count (0—6)

Design Information (continued)

Using Voice-Thru Mode

Voice-Thru mode allows for receiving, transmitting, and storage of audio data. This is particularly useful for applications such as PC-based answering machines and voice-mail systems. Audio samples are transmitted and/or received in real time through the data pump. The data can be μ-law, a-law, or 16-bit linear samples. The data pump translates the data between the format requested by the host and the 16-bit linear format needed at the codec.

Table MJ-10. Real-Time Voice-Thru Modes

Data Format	Sampling Rate	Bits/Sample
Linear PCM	variable	16
μ-Law PCM	variable	8
a-Law PCM	variable	8

The data pump processes the voice data in frames of 160 samples and double-buffers frames in both the transmit and receive paths. Double-buffering allows the data pump to operate on one frame (in each direction) while the host transfers data to/from the data pump.

The frame period is the time required to transmit and receive a frame of data on the line. This period also determines the amount of time available for the host to transfer each frame to/from the data pump. The frame period is calculated by dividing the frame size (160) by the sampling rate (variable). For a typical case using an 8 kHz sampling rate, the frame period is 20 ms. In this case, the host has 20 ms in which to read the last received frame from the data pump and write the next frame to be transmitted to the data pump. The timing of data transfers during each frame period is not critical.

The host passes data to/from the data pump using the parallel data transfer mode. Status information is available for each frame received or transmitted.

While in voice-thru mode, tone generation and detection and DTMF generation and detection may be used. See Table MJ-12 for a complete list of commands that can be used while voice-thru mode is in use.

Entering Voice-Thru Mode

Voice-thru mode is started by issuing host command 0xa0 with the appropriate arguments (see Host Command 0xa0, page MJ-27). One of the arguments specifies linear, a-law, or μ-law data.

Other arguments set the sampling rate and the initial record and playback levels. Additional information on setting the sampling rate is provided in the following section.

The return to idle command (code 0x13) is used to exit voice-thru mode.

Setting the Sampling Rate

The sampling rate to be used during voice-thru mode is specified by supplying two values in mailboxes 3 and 4 before issuing the voice-thru command. By default, the sampling rate used is 8 KHz. If either mailbox 3 or 4 contains a zero, the default sampling rate is used.

Following is the format for the Sampling Rate Value A (mailbox 3) and the Sampling Rate Value B (mailbox 4):

	7	6	5	4	3	2	1	0
Value A →	×2	X	X	SNUMB[4:0]				
Value B →	0	0	0	SNMDB[4:0]				

Following are the descriptions of the fields in the Sampling Rate Value control words:

×2 — Multiplies the sample rate calculated by SNUMB and SNMDB by 2.

SNUMB — Sample Clock Numerator. SNUMB = NS–1

SNMDB — Sample Clock Numerator minus Denominator. SNMDB= NS–DS–1 This value should be negative, larger than 6 bits, and truncated to five bits.

The following equation describes how these values are used to calculate the sampling rate.

$$fs = \text{Sampling Frequency} = 9{,}900 \cdot \frac{Ns}{Ds} \text{ Hz}$$

$$Ns < Ds < 33$$

For example, to achieve a sampling rate of 7200 bits/s, values are chosen for NS and DS of 8 and 11, respectively. Values A and B then become:

SNUMB = NS–1 = 8–1 = 7
SNMDB = NS–DS–1 = 8–11–1 = –4

Value A = 0x07
Value B = 0x1c

Design Information (continued)

Voice-Thru Mode Control/Status Information

The HDLC Options Control Word (C/S RAM location 0x3d) provides two bits used to monitor and control voice-thru mode. Bit 15 provides a status bit indicating whether voice mode is currently in use. Bit 14 is used to enable the transmit data path. Since there is no echo cancellation in use while voice-thru mode is active, it is recommended that transmit data only be enabled while actually transmitting.

Record and Playback Levels

The initial record and playback levels to be used while in voice-thru mode are specified as arguments to the voice-thru mode command. These levels are then stored in C/S RAM and can be changed while voice mode is active. The following table lists the C/S RAM locations, valid entries, and the corresponding gains for these two control words.

Table MJ-11. Voice-Thru Mode Play/Record

Parameter	C/S Addr.	Valid Entries	Resulting Gain
Playback level	0x03	0—43	+18 to –25 dB
Record level	0x4a	0—43	+18 to –25 dB

Valid Commands While in Voice Mode

Table MJ-12 lists the host commands that can be used while voice-thru mode is active.

Table MJ-12. Valid Commands in Voice-Thru

Command (hex)	Description
0x01	Write to DSP RAM
0x04	Read from DSP RAM
0x07	Generate tones
0x08	Detect tones
0x09	Detect DTMF tones (8 kHz sampling rate only when in GSM/Voice mode)
0x0d	Read RAM and clear location
0x13	goto idle (exit GSM/Voice mode)

Receiving Data

Receive data is read by the host from data pump registers 0xa—0xf. (The following section describes the precise format of the data.). The data pump double buffers the received data, so that the host has a frame period in which to read the current frame from the data pump while the data pump is receiving the next frame. The timing of reads within the frame period are not critical.

When the data pump has a frame of data ready for the host to read, it first checks to see that the host has read any previous information from the mailboxes, then writes the current data (maximum six bytes at a time) to the mailboxes. The receive data status word (passed in register 0x17) indicates the number of bytes being passed and an end-of-frame (EOF) status bit. When the EOF status bit is set, it indicates that the current data represents the last data of that frame. At this point, registers 0xe, 0xf, and 0x16 are used to pass status information regarding the frame just received (see next section).

The host must read all data in the current frame before the data pump has received the next frame. If the host fails to do so, an overflow error flag is set (register 0x1f, bit 0). The host must reset this bit after an error occurs.

An interrupt can be generated whenever the data pump writes to register 0xf. Therefore, receive data transfers and command responses can generate an interrupt. This interrupt is enabled by setting bit 3 of register 0x2e.

Receive Data Format (data pump to host)

Receive data is read by the host six bytes at a time from the data pump mailboxes. Status information is also provided with each six-byte set of data and after each 160-sample frame. Table MJ-13 shows the locations where this information is read from in the data pump register set.

The Receive Data Status Word read from register 0x17 contains two pieces of information: the number of bytes and an end-of frame (EOF) status bit. Following is the format of this word.

Bits	Description
7—4	Receive Data Transfer. 0xA = Voice-mode receive data transfer
3	End of Frame. 1 = end of frame (EOF)
2—0	Receive byte count. A value of 0—6

Design Information (continued)

Table MJ-13. Host Register Uses During Voice-Thru Mode

Host Register	Resgister Use in Normal Operation	Register Use During Voice-Thru Mode	
		μ-law or a-law data	16-bit linear data
0x02	Not used.	Transmit sample 1	Transmit sample 1, lower byte
0x03	Not used.	Transmit sample 2	Transmit sample 1, upper byte
0x04	Command parameter mailboxes	Transmit sample 3	Transmit sample 2, lower byte
0x05		Transmit sample 4	Transmit sample 2, upper byte
0x06		Transmit sample 5	Transmit sample 3, lower byte
0x07		Transmit sample 6	Transmit sample 3, upper byte
0x08		Not used.	Not used.
0x09	Command mailbox	Transmit Data Command	Transmit Data Command
0x0a	Fast access location mailboxes	Receive sample 1	Receive sample 1, lower byte
0x0b		Receive sample 2	Receive sample 1, upper byte
0x0c	Not used.	Receive sample 3	Receive sample 2, lower byte
0x0d	Response parameter mailboxes	Receive sample 4	Receive sample 2, upper byte
0x0e		Receive sample 5	Receive sample 3, lower byte
0x0f	Response code mailbox	Receive sample 6 *	Receive sample 3, upper byte *
0x16	Not used.	Not used. *	Not used. *
0x17	Not used.	Receive Data Status Word	Receive Data Status Word

* If End-Of-Frame (EOF) flag is set in Receive Data Status Word, this location holds status information.

A 160-sample frame of 8-bit data requires 26 6-byte transfers and a final 4-byte transfer; a 160-sample frame of 16-bit data requires 53 6-byte transfers and a final 2-byte transfer.

As noted above, when the EOF status bit is set in the Receive Data Status Word, the values passed in registers 0xe, 0xf, and 0x16 have special significance. The following table lists the values passed in these locations.

Register	Mode	Description (when EOF = 1)
0x0e	R	Inband energy level in dB (upper byte of tone energy)
0x0f	R	Tone detection (lower byte of tone found word)
0x16	R	Frame status

Transmitting Data

Data to be transmitted is passed from the host to the data pump via mailboxes 0x2—0x9. (The precise format of the data is described below). The data pump double buffers the transmit data, so that the host has a 20 ms window in which to write the next frame to the data pump while the data pump is transmitting the current frame. The timing of writes within the 20 ms window are not critical.

Before writing data to be transmitted, the host must first wait for the transmit data buffer ready (TDBR) flag to be set (register 0x1f, bit 7). The data pump sets this flag at the beginning of each frame. The host must clear this flag after sending the end of the frame. The host must also signal the end of each frame by setting the EOF bit in the transmit data command passed with the data.

If the transmit data buffer is not filled before the end of the current frame, an underrun error flag is set (register 0x1f, bit 3). The host must reset this bit after an error occurs.

Transmit Data Format (host to data pump)

Transmit data is passed from the host to the data pump six bytes at a time. The host must keep track of 160-sample frames and indicate the end of each frame in the data stream. Table MJ-13 shows the mailboxes used by the host to pass voice-thru mode data to the data pump.

The Transmit Data Command passed in register 0x9 contains two pieces of information: the number of bytes and an end-of frame (EOF) status bit. The data to be passed should be written to the mailboxes prior to writing the Transmit Data

Design Information (continued)

Command. Following is the format of the Transmit Data Command word:

Bits	Description
7—4	**Transmit Data Indicator.** 0xA = Transmit data indicator (specifies a voice-thru mode data transfer)
3	**End of Frame.** 1 = end of frame (EOF) 0 = not end of frame
2—0	**Byte count.** (0—6) 000 — 0 bytes 001 — 1 byte 010 — 2 bytes 011 — 3 bytes 100 — 4 bytes 101 — 5 bytes 110 — 6 bytes

Transmit Data Interrupt

If desired, an interrupt can be generated when a TDBR condition occurs. This condition shares an interrupt status bit with UART receive (Rx2ND_IQ) and UART transmit (Tx2ND_IQ). Enabling the TDBR interrupt is a two step process. First, a mask value must be written to the interrupt mask control register (0x2e) to enable the combined UART/TDBR interrupt. The mask value written contains 0's for those interrupts to be enabled and 1's for those to be disabled. To enable the TDBR interrupt, clear bit 7 of register 0x2e. Second, the TDBR condition must be enabled as a source for this interrupt. To do this, set bit 4 of register 0x1f.

Once an interrupt occurs, the host must first read register 0x2e to determine the source of the interrupt. If bit 7 is set and the UART is being used, registers 0x1e and 0x1f must then be read to determine the actual source. After processing the interrupt, bit 7 of register 0x2e must be cleared by the host. Figure MJ-9 depicts this decision process.

Typical Usage Example

Figure MJ-10 shows the flowchart for a simple case where the data pump is used to play an outgoing message and then record a message from the line. Tone detection is used to monitor for commands from the caller. Before entering this flow diagram, the data pump is acting like a normal modem. After exiting this procedure, the data pump returns to behaving as a modem.

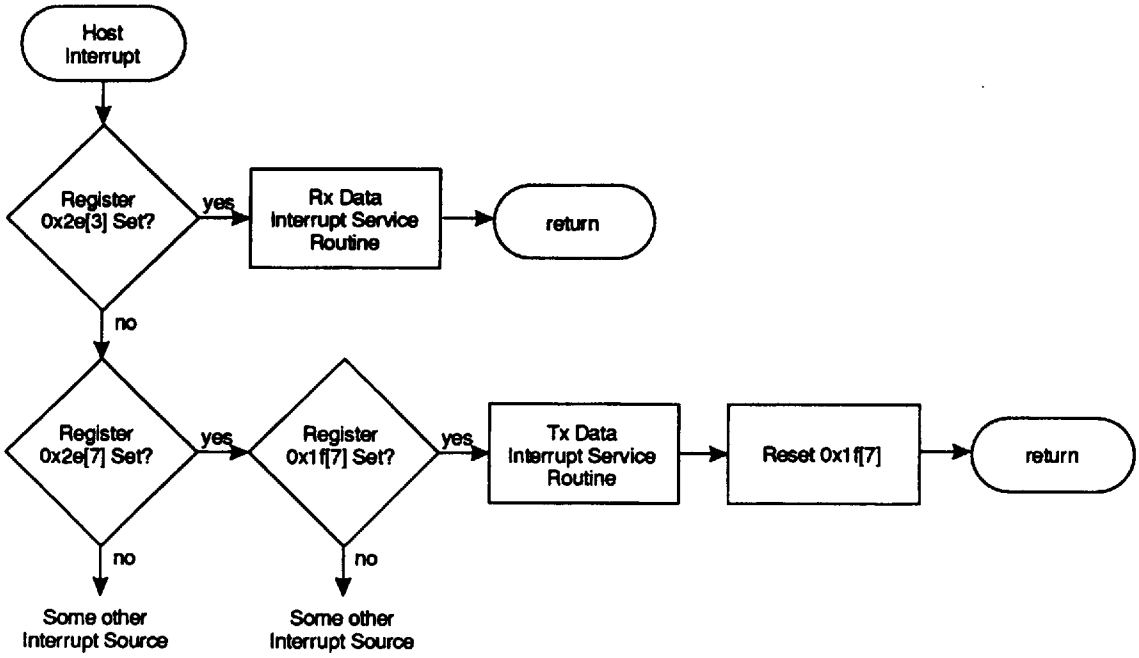


Figure MJ-9. Host Interrupt Processing with Voice-Thru Mode

Design Information (continued)

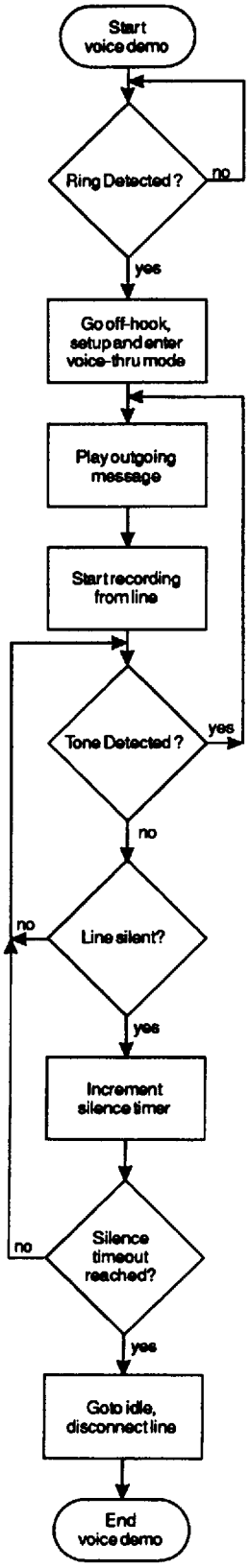


Figure MJ-10. Voice Demo Flow Chart

Improved On-line Monitoring

A problem that arises with echo canceling modems is an inability to reliably detect the presence or absence of receive signal energy. When a network connection is abruptly terminated, the remote signal goes away. However, since the characteristics of the echo have changed drastically, the echo canceler stops canceling. Therefore, the receiver sees an echo of the transmit signal. The receive level (C/S RAM location 0x4a) will indicate the level of the uncanceled echo, instead of the actual signal from the remote modem.

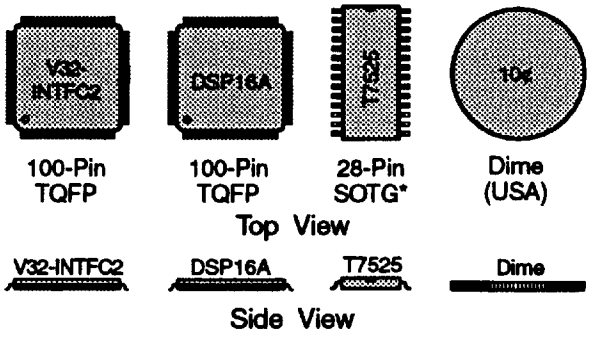
An echo correlation feature has been added to the data pump to detect this condition. The echo correlator compares the signal at the input to the receiver with an estimate of the near and far transmit echo. The output of the echo correlator is read at C/S RAM location 0x44. This feature is active only in V.32 and V.32bis modes.

Bit 11 of the operating status word (C/S RAM location 0x3a) is used to report echo correlator and mean squared error status to the host controller. If the value of the echo correlator or the mean squared error pass some preset threshold, bit 11 will be set to alert the host controller. For the echo correlator, the threshold is fixed at 900 (0x384). The mean squared error requires that a threshold be programmed at C/S RAM location 0xb. The default value of this threshold at power-up and after a reset is zero. The host controller can change this threshold as needed.

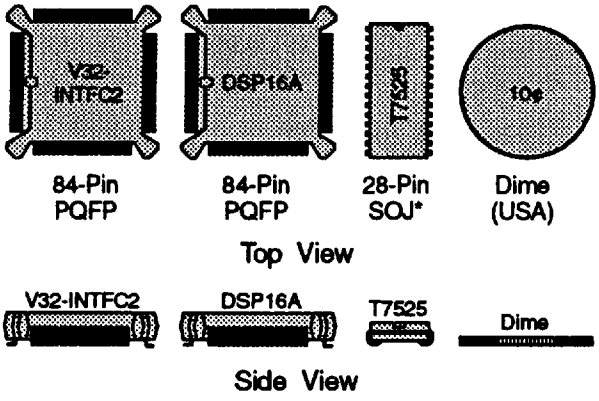
Since both the echo correlator and the mean squared error can cause this bit to be set, the host controller must take additional actions to interpret the meaning of this status bit. For example, after seeing this bit set, the host controller should check the actual echo correlator value (C/S RAM location 0x44). If this value is above the fixed threshold, then the echo correlator caused the status bit to be set. If the value was below the fixed threshold, the mean squared error level caused the bit to be set.

Note: The echo correlator still works with host code that operates as described in the July 1992 data book supplement. However, the host is no longer required to read and clear C/S RAM location 0x44. This value no longer grows continuously, but is now an averaged value that reaches a level greater than 900 when correlation is detected.

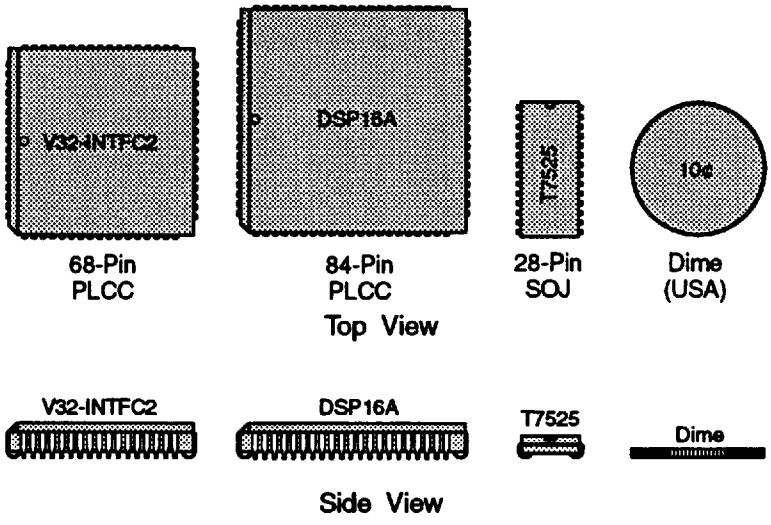
Introduction (continued)



A. V32lite Packages



B. LapTop Packages



C. DeskTop Packages

* For the 3.3V versions of these chip sets, the T7525 codec is replaced by a CSP1027 codec in a 44-pin PQFP package for the LapTop version or a 48-pin TQFP package for the V32lite option.

Figure 1. Package Option Size Comparison