

T-46-13-47

EP1800

ALTERA

48-MACROCELL EPLD

EP1800

FEATURES

- High density, User-Configurable LSI logic replacement for conventional and custom logic
- Functional and pin compatible with the Altera EP1810
- 20 MHz clock rates
- "Zero Power" (typically 35 μ A standby)
- 48 Macrocells with configurable I/O architecture allowing 64 inputs or 48 outputs
- Programmable registers providing D, T, SR or JK flipflops with individual Asynchronous Clear control.
- Programmable clock option allows independent clocking of all registers
- TTL/CMOS I/O compatibility
- 100% generically testable—provides 100% programming yield
- Programmable "Security Bit" allows total protection of proprietary designs
- CAD support from Altera's A+PLUS Development System featuring schematic capture design entry with extensive Primitive and TTL libraries
- Package in a 68 pin (window) and plastic (one time programmable) JLCC, PLCC and PGA configurations

GENERAL DESCRIPTION

The Altera EP1800 is a pin-compatible version of the popular EP1810 Erasable Programmable Logic Device (EPLD). Available in 68-pin PGA and 68-pin J-leaded chip carrier packages, the EP1800 contains 48 Macrocells with user-configurable I/O architecture, allowing up to 64 inputs and 48 outputs.

Each of the 48 Macrocells contains a programmable AND and fixed OR PLA structure, see EP1810 datasheet, with a maximum of eight product terms for logic implementation. In addition, single product terms control Output Enable/Asynchronous Clock and Asynchronous Clear functions.

The Altera proprietary programmable I/O architecture allows the EP1800 user to program output and feedback paths for both combinatorial or registered operation, active high or active low.

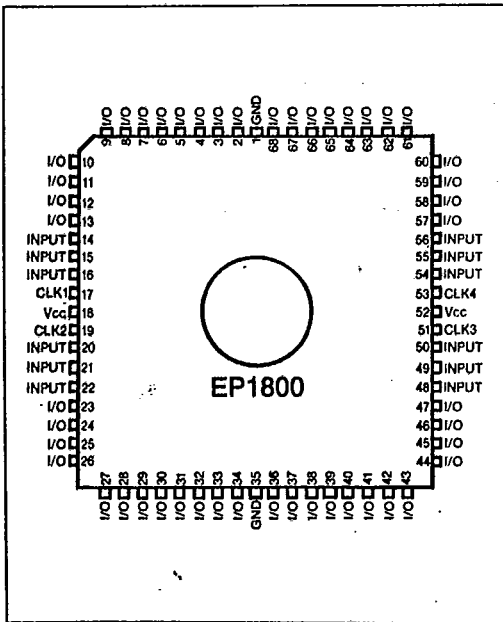
For increased flexibility, the EP1800 also includes programmable registers. Each of the 48 internal registers may be programmed to be D, T, SR or JK flipflop. In addition, each register may be clocked asynchronously on an individual basis or synchronously on a banked register basis.

For proper operation, standard high performance design practices should be followed. It is recommended that opaque labels be placed over device window. Input and output pins must be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic level (e.g. either V_{CC} or GND). Each set of V_{CC} and GND pins must be shorted together directly at the device. Power supply decoupling capacitors of at least .2 μ F must be connected between each V_{CC} pin and GND. For the most effective decoupling, connect one capacitor between each set of V_{CC} and GND pins, directly at the device.

Programming the EP1800 is accomplished by using the Altera A+PLUS PC-based development software which supports schematic capture, netlist, state machine and Boolean equation design entry methods. Once the design is entered, A+PLUS automatically performs translation into logical equations, Boolean minimization, and design fitting directly to an EP1800. The device may then be programmed to achieve customized working silicon within minutes at the designer's own desktop.

For full EP1800 functional description please consult the EP1810 datasheet.

CONNECTION DIAGRAM

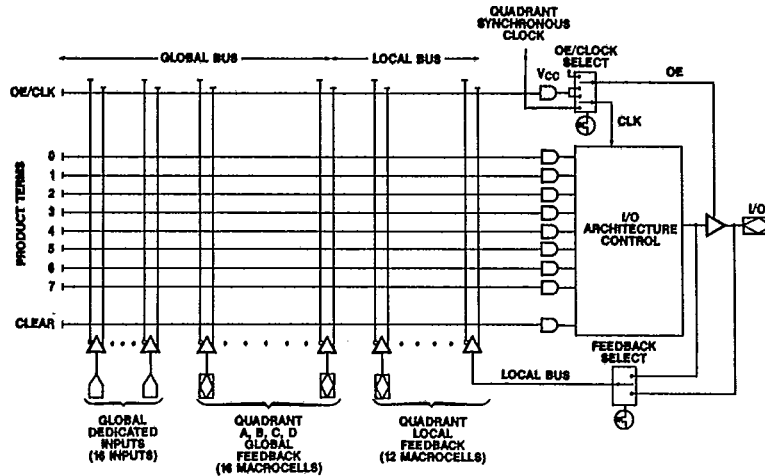


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Figure 1. Global Macrocell Logic Array



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Figure 2. ICC vs. FMAX

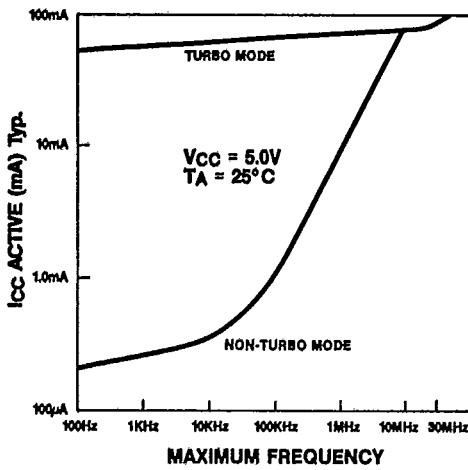
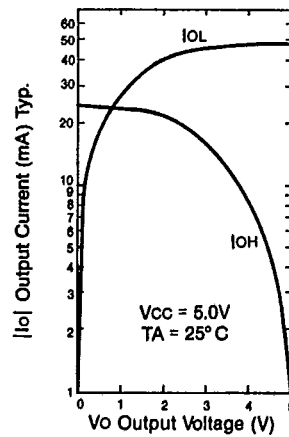


Figure 3. Output Drive Current



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ABSOLUTE MAXIMUM RATINGS

COMMERCIAL, INDUSTRIAL, MILITARY

Note: See Design Recommendations

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SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V _{CC}	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
V _{PP}	Programming supply voltage		-2.0	13.5	V
V _I	DC INPUT voltage		-2.0	7.0	V
I _{MAX}	DC V _{CC} or GND current		-300	+300	mA
I _{OUT}	DC OUTPUT current, per pin		-25	+25	mA
P _D	Power dissipation			1500	mW
T _{STG}	Storage temperature	No bias	-65	+150	°C
T _{AMB}	Ambient temperature	Under bias	-65	+135	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V _{CC}	Supply Voltage	note (6)	4.75 (4.5)	5.25 (5.5)	V
V _I	INPUT voltage		0	V _{CC}	V
V _O	OUTPUT voltage		0	V _{CC}	V
T _A	Operating temperature	For Commercial	0	70	°C
T _A	Operating temperature	For Industrial	-40	85	°C
T _C	Case temperature	For Military	-55	125	°C
T _R	INPUT rise time	note (9)		500	ns
T _F	INPUT fall time	note (9)		500	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)
 (V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
 (V_{CC} = 5V ± 10%, T_C = -55°C to 125°C for Military)*

Note (1) and (6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V _{IH}	HIGH level input voltage		2.0		V _{CC} + 0.3	V
V _{IL}	LOW level input voltage		-0.3		0.8	V
V _{OH}	HIGH level TTL output voltage	I _{OH} = -4mA DC	2.4			V
V _{OH}	HIGH level CMOS output voltage	I _{OH} = -2mA DC	3.84			V
V _{OL}	LOW level output voltage	I _{OL} = 4mA DC			0.45	V
I _I	Input leakage current	V _I = V _{CC} or GND	-10		+10	μA
I _{OZ}	3-state output off-state current	V _O = V _{CC} or GND	-10		+10	μA
I _{CC1}	V _{CC} supply current (standby)	V _I = V _{CC} or GND No load		35	150	μA
I _{CC2}	V _{CC} supply current (non-turbo)	V _I = V _{CC} or GND No load, f = 1.0 MHz note (7)		15	30 (40)	mA
I _{CC3}	V _{CC} supply current (turbo)	V _I = V _{CC} or GND No load, f = 1.0 MHz note (7)		90	140 (180)	mA

CAPACITANCE

Note (4)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V f = 1.0 MHz		15	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V f = 1.0 MHz		15	pF
C _{CLK}	Clock Pin Capacitance	V _{IN} = 0V f = 1.0 MHz		25	pF

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AC CHARACTERISTICS

($V_{CC} = 5V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$ for Commercial)
 ($V_{CC} = 5V \pm 10\%$, $T_A = -40^\circ C$ to $85^\circ C$ for Industrial)
 ($V_{CC} = 5V \pm 10\%$, $T_C = -55^\circ C$ to $125^\circ C$ for Military)*

SYMBOL	PARAMETER	CONDITIONS	EP1800-2		EP1800-3		EP1800		NON-TURBO ADDER	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	note (5)	
t_{PD1}	Input to non-registered output	$C_1 = 50pF$		65		75		85	30	ns
t_{PD2}	I/O input to non-registered output			70		80		90	30	ns
t_{IN}	Input pad and buffer delay			10		12		14	0	ns
t_{IO}	I/O input pad and buffer delay		5		5		5	0	ns	
t_{LAD}	Logic Array delay		40		44		48	30	ns	
t_{OD}	Output buffer and pad delay	$C_1 = 50pF$		15		19		23	0	ns
t_{ZX}	Output buffer enable			15		19		23	0	ns
t_{XZ}	Output buffer disable		$C_1 = 5pF$ note (2)		15		19		23	0
f_{max}	Maximum clock frequency	note (10)	20.8		18.5		16.1		0	MHz
t_{SU}	Register set-up time		12		14		18		0	ns
t_{HS}	Register hold time (system clock)		0		0		0		0	ns
t_H	Register hold time		30		30		30		0	ns
t_{CH}	Clock high time		24		27		30		0	ns
t_{CL}	Clock low time		24		27		30		0	ns
t_{IC}	Clock delay			40		44		48	30	ns
t_{CS}	System clock delay			4		4		4	0	ns
t_{FD}	Feedback delay			10		14		16	-30	ns
t_{CLR}	Register clear delay			40		44		48	30	ns
t_{CNT}	Minimum clock period (register output feedback to register input-internal data)			62		72		82	0	ns
f_{CNT}	Internal maximum frequency ($1/t_{CNT}$)	note (7)	16.2		13.8		12.2		0	MHz

Notes:

- Typical values are for $T_A = 25^\circ C$, $V_{CC} = 5V$.
- Sample tested only for an output change of 500mV.
- Minimum DC input is $-0.3V$. During transitions, the inputs may undershoot to $-2.0V$ for periods less than 20ns.
- Capacitance measured at $25^\circ C$. Sample tested only. Clock pin capacitance for dedicated clock inputs only. Pin 19, (high voltage pin during programming), has capacitance of 160 pF max.
- See TURBO-BIT™, page 19.
- Figures in () pertain to military and industrial temperature version.
- Measured with device programmed as four 12-Bit counters.
- EPLD automatically goes into standby mode if logic transitions do not occur when in non-turbo mode (approximately 100 ns after last transition).
- Clock t_r , $t_f = 250ns$ (100ns).
- The f_{MAX} values shown represent the highest frequency for pipelined data.

GRADE	AVAILABILITY	
	EP1800-2	EP1800-3 EP1800
Commercial ($0^\circ C$ to $70^\circ C$)		EP1800-3 EP1800
Industrial ($-40^\circ C$ to $85^\circ C$)		EP1800-3 EP1800
Military ($-55^\circ C$ to $125^\circ C$)		EP1800

* The specifications noted above apply to military operating range devices. MIL-STD-883 compliant product applications are provided in military product drawings available on request from Altera marketing at 408/984-2805, ext. 101. These military product drawings should be used for the preparation of source control drawings.

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