CYPRESS SEMICONDUCTOR

Timing Control Unit

Features

- **Timing Control Unit, Clock Generator for CY7C601A and CY7C611A SPARC processors**
- **Supports 25-, 33-, 40-MHz operation**
- **Simplifies interface to slow memory and peripherals by eliminating the need for wait-state logic**
- **Flexible clock extension architecture**
  - **—0-cycle to 14-cycle extensions**
  - **—user controlled (continuous cycle) extension**
- **24-pin 300-mil DIP and 28-pin PLCC packages**

Overview

Like most RISC processors, a fast-running 7C601/611 SPARC Integer Unit (IU) must spend time waiting for slower memory or peripheral devices. Because the 7C601/611 completes an instruction and generates a new address every clock, a complicated handshake protocol and a correspondingly complicated state machine must be used to keep the IU from getting ahead of the slow devices.

This protocol relies primarily on the signals $\overline{\text{MHOLD}}$ (Memory Hold) and $\overline{\text{MDS}}$ (Memory Data Strobe). $\overline{\text{MHOLD}}$ is asserted by the memory system,to freeze the processor when data is unavailable. $\overline{\text{MDS}}$ is used to strobe in the data when it becomes available. The timing relationships between these signals and other processor-generated signals must be accounted for by the state machine handling the handshaking.

The purpose of the 7C325 Timing Control Unit (TCU) is to simplify the wait state logic by controlling (stretching) the clock sent to the IU. If the IU accesses a device for which it must wait, the LOW portion of the clock sent to the IU is extended—i.e., held low—until the device is ready. Once the clock signal is subsequently released, the IU can continue. Because the IU effectively encounters only one clock cycle per access, the need for the complicated handshake state machine is eliminated. The single chip TCU is especially useful in embedded control applications where low chip count is highly desirable.

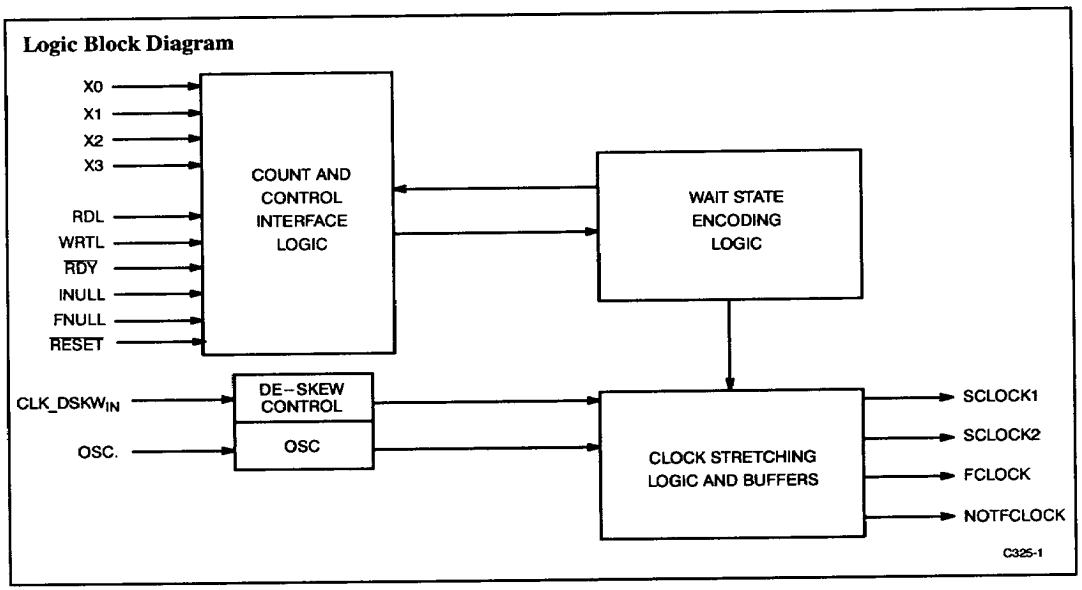
Functional Description

The number of stretched cycles in the 7C325 TCU is controlled by a four-bit binary count input: an input of 0001 will stretch the clock for one cycle (keep it LOW one extra cycle), an input of 0010 will stretch the clock for two cycles, and so on up to an input of 1110 to stretch the clock for fourteen cycles. A count input of 1111 will stretch the clock continuously until an $\overline{\text{RDY}}$ (ready) signal is asserted. An input of 0000 is the no stretch condition.

These counts are derived from the processor addresses. Because the input count is four bits wide, the address space can be divided into as many as sixteen subspaces, and devices that require the same number of wait cycles can be grouped into the same subspace.

For example, if all devices that require eight wait cycles are memory mapped to hex address 3xxxxxxx, then whenever the four most significant address bits are equal to 0011, a code converter will generate a count of 1000 to the CY7C325. This code converter can be easily implemented with a PAL or PLD. In addition, the user does not need to create the full sixteen subspaces. If only 0, 2, 4, and continuous wait cycles are needed, the user may create just four subspaces and, consequently, employ just two address bits to generate the TCU input count. It should also be noted that the subspaces can be of different sizes.

Logic Block Diagram



Functional Description (continued)

The code converter described above is preferred but not required. Users who wish to reduce cost or board space can eliminate the code converter by feeding the IU's address bits directly to the TCU and memory mapping the devices by their counts (e.g., memory map devices requiring eight wait cycles to hex address 8xxxxxxx). The code converter can also be eliminated by programming the number of wait cycles for each address into the IU's ASI bits.

The count inputs are sampled on the falling edge of the stretched clock, SCLOCK, which is used as the system clock by the IU and peripherals. It is one of the three clock signals provided by the 7C325. The other two are FCLOCK and NOTFCLOCK. If the count input is not 0000 when it is sampled, the stretched clock output will stay LOW for the specified number of cycles.

The two SCLOCK outputs can be buffered to increase their driving capability. However, the same buffer delay must be added to the FCLOCK output path and the NOTFCLOCK output—skew control feedback path to eliminate skew. There are several other signals that affect the stretching operation as well. RD is an output from the IU that indicates whether an access is a read (RD = 1) or a write (RD = 0). WRT, another IU output, is asserted only on the first cycle of a write. RD is needed because a read access (load) is treated differently from a write access (store). A minimum write accessconsists of two clock cycles. The first clock is used by the processor to reverse the data bus and by external logic to perform tasks such as access protection checking, address translation, and cache tag comparison. The second cycle is when the write is actually executed. Thus, the first cycle of a write is never stretched. Because WRT is active only during the first cycle of a write, it is used by the TCU to differentiate between the two cycles.

INULL and FNULL are signals asserted by the Integer Unit and Floating Point Unit, respectively, to nullify the current access. Assertion of either signal during the first cycle of a load or store will terminate an access. However, because INULL is always asserted in the second cycle of a store (to prevent assertion of MHOLD for the remainder of the write), it is ignored by the 7C325 once a write stretch has started.

Pin Description

The following sections contain brief descriptions of the pin functions.

Power and Ground

VCC: power, connected to the +5V power supply.

GND: ground.

Inputs

CLK: clock input to TCU's internal logic.

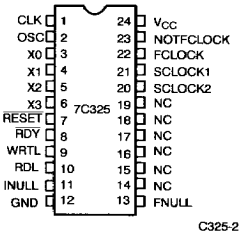
OSC: input from the oscillator.

X0 – X3: count inputs, derived from CPU address; equal to the number of cycles the clock will be stretched. These inputs are sampled by the falling edge of the SCLOCK.

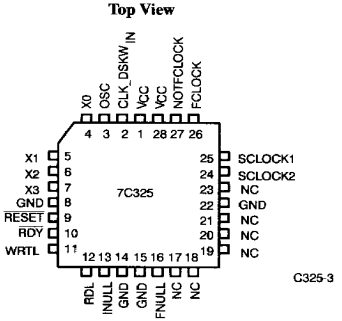
X{3..0}	Number of Cycles SCLOCK will be Stretched
0000	zero — no stretch
0001	one
0010	two
0011	three
0100	four
0101	five
0110	six
0111	seven
1000	eight
1001	nine
1010	ten
1011	eleven
1100	twelve
1101	thirteen
1110	fourteen
1111	countinuous until $\overline{RDY}$

Pin Configurations

DIP
Top View



PLCC
Top View



Pin Description (continued)

$\overline{\text{RESET}}$: reset; restores the TCU to a known state; sampled by the falling edge of FCLOCK.

$\overline{\text{RDY}}$: ready, from peripheral device; this input is sampled by the falling edge of FCLOCK. If this input is sampled LOW the TCU will terminate a continuous stretch. (a watchdog timer time-out signal can be ORed into this input as well)

WRTL: early write; this is the latched version of the processor signal WRT. It is sampled by the TCU at the falling edge of SCLOCK.

RDL: read/write; this is the latched version of the processor signal RD. It is sampled by the TCU at the falling edge of SCLOCK. (1 = read, 0 = write)

INULL: integer nullify from the processor. It is asserted by the IU to nullify its current access. If INULL is HIGH the TCU will end the current stretch.

FNULL: floating point nullify from the FPU. It is asserted by the FPU to nullify its current access. If FNULL is HIGH the TCU will end the current stretch.

Outputs

FCLOCK: non-stretched clock signal.

NOTFCLOCK: inverted FCLOCK – fed back to the TCU CLK input to eliminate skew.

SCLOCK1: system clock.

SCLOCK2: system clock. (repeated to provide extra load driving capability)

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PLDs

Selection Guide

	7C325–40	7C325–33	7C325–25
Frequency (MHz)	40	33	25
I_{CC} (mA)	190	190	90

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +V_{CC} Max.

DC Input Voltage ..... – 0.5V to +5.5V

DC Input Current ..... –30 mA to +5 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	7C325–40, 33		7C325–25		Units
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OH} = – 3.2 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OL} = 16 mA		0.5		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs[1]	2.0		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs[1]		0.8		0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.	–250	+50	–10	+10	μA
I_{OZ}	Output Leakage Current	$V_{SS} \le V_{OUT} \le V_{CC}$, V_{CC} = Max.	–100	+100	–40	+40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[2]	–30	–90	–30	–90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open		190		90	mA

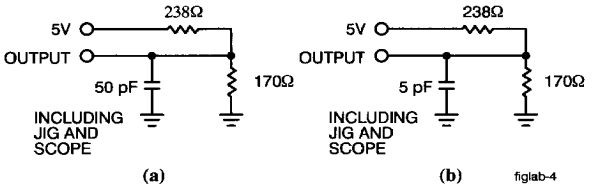
Notes

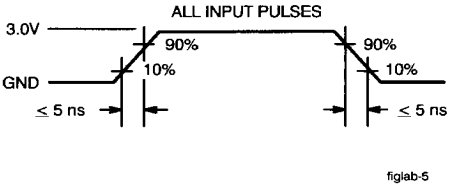
1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Capacitance

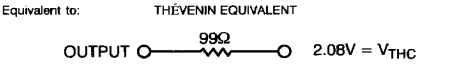
Parameters	Description	Max.	Units
C_{IN}	Input Capacitance	10	pF
C_{OUT}	Output Capacitance	10	pF

AC Test Loads and Waveforms





Speed	C_L	Package
40 MHz	15 pF	DC, PC
	50 pF	JC
33 MHz	15 pF	DC, PC
	50 pF	JC
25 MHz	50 pF	DC, PC, JC



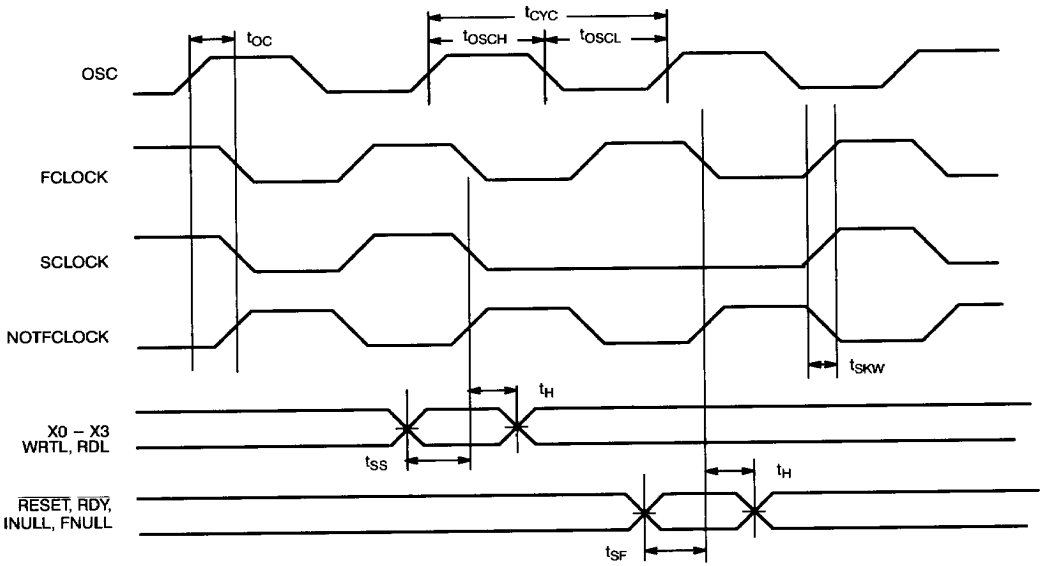
Switching Characteristics Over the Operating Range

Parameters	Description	7C325–40		7C325–33		7C325–25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{OC}	OSC to FCLOCK, NOTFCLOCK, and SCLOCKs delay[3]		8		12		15	ns
t_{SS}	Set-Up Time to SCLOCK Falling Edge	4		5.5		10		ns
t_{SF}	Set-Up Time to FCLOCK Falling Edge	4		5.5		10		ns
t_H	Hold Time	2		2		2		ns
t_{SKW}	Skew Between Any Two Clock Outputs[4]		1		1		1	ns
t_{CYC}	Cycle Time	25		30		40		ns
t_{OSCH}	Oscillator HIGH Time	.45 t_{CYC}		.45 t_{CYC}		.45 t_{CYC}		ns
t_{OSCL}	Oscillator LOW Time	.45 t_{CYC}		.45 t_{CYC}		.45 t_{CYC}		ns

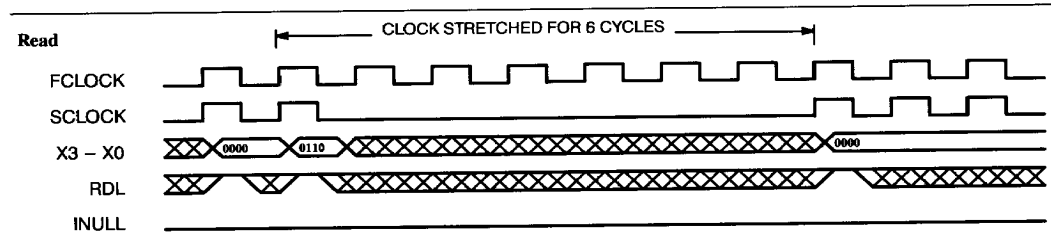
Notes

3. This specification is guaranteed for all device outputs changing state in a given cycle.
4. The capacitive loading at each clock output is with 10% of the other clock outputs.

Switching Waveforms

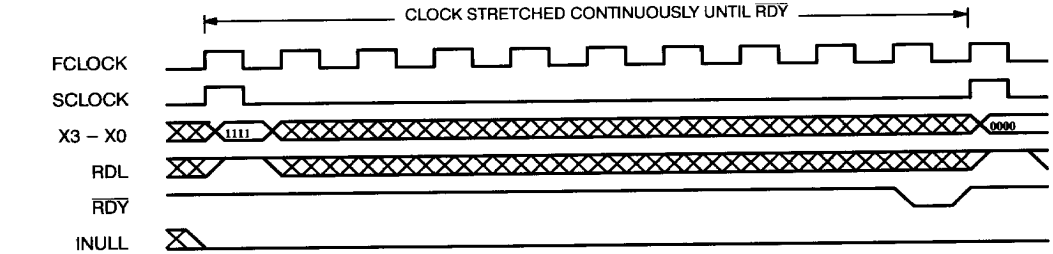


Read



(not shown – RESET, RDY, WRTL, OSC, NOTFCLOCK, FNULL)

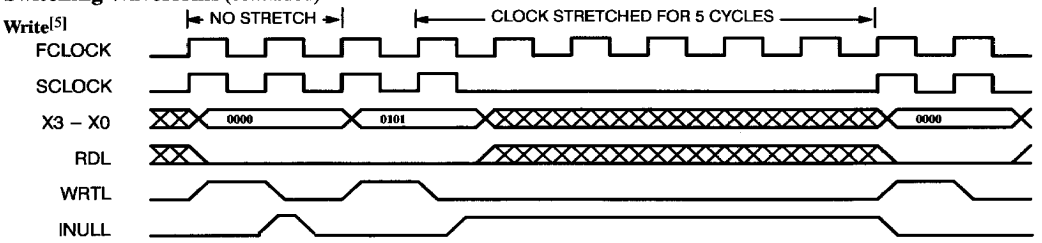
Read – Continuous Stretch



(not shown – RESET, WRTL, OSC, NOTFCLOCK, FNULL)

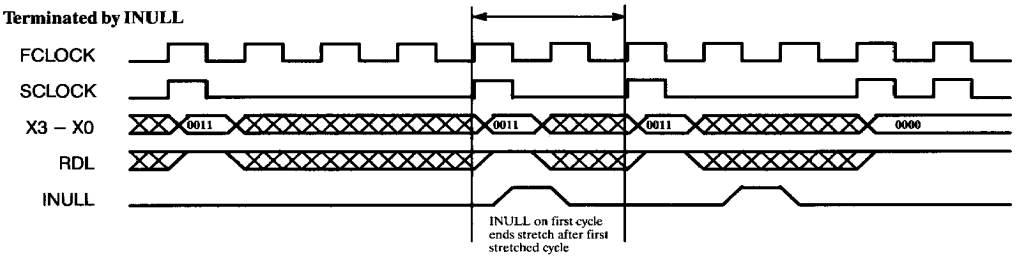
Switching Waveforms (continued)

Write[5]



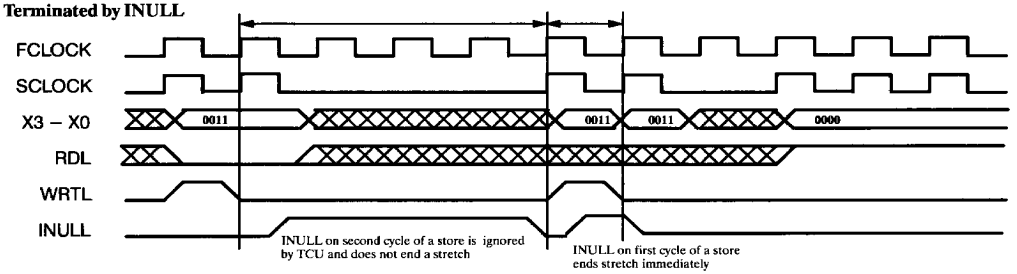
(not shown – $\overline{\text{RESET}}$, OSC, $\overline{\text{RDY}}$, NOTFCLOCK, FNULL)

Read Terminated by INULL



(not shown – $\overline{\text{RESET}}$, WRTL, $\overline{\text{RDY}}$, OSC, NOTFCLOCK, FNULL)

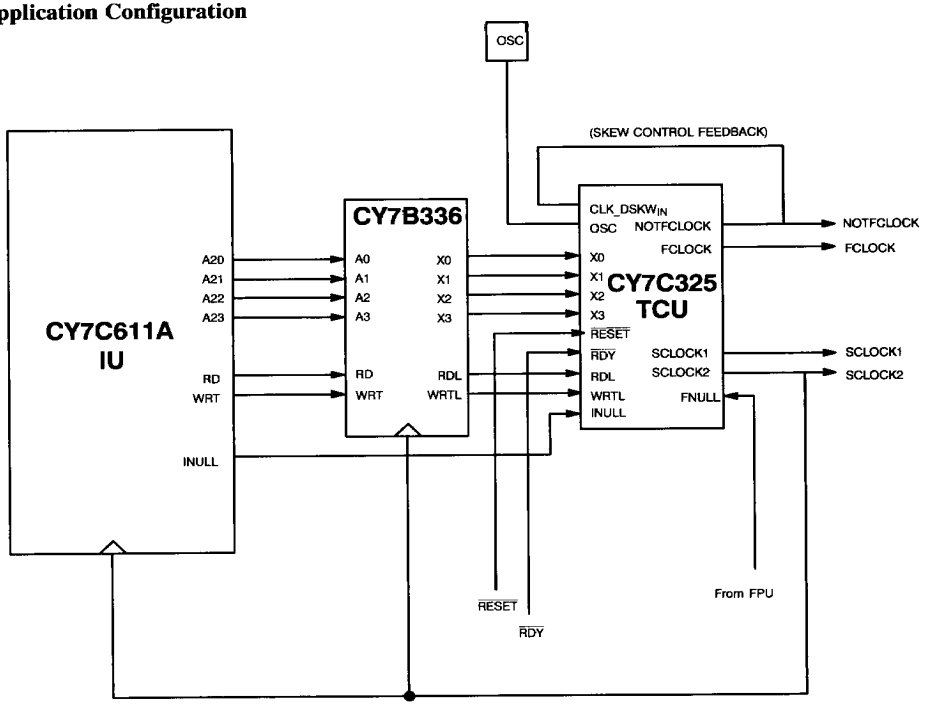
Write Terminated by INULL



(not shown – $\overline{\text{RESET}}$, OSC, $\overline{\text{RDY}}$, NOTFCLOCK, FNULL)

Note:
5. The first cycle of a write is not stretched.

Typical Application Configuration



Ordering Information

f_{MAX} (MHz)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
40	190	CY7C325–40PC	P13	Commercial
		CY7C325–40DC	D14	
		CY7C325–40JC	J64	
33	190	CY7C325–33PC	P13	Commercial
		CY7C325–33DC	D14	
		CY7C325–33JC	J64	
25	90	CY7C325–25PC	P13	Commercial
		CY7C325–25DC	D14	
		CY7C325–25JC	J64	

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