"Zero Delay" / Low Skew Output Buffer

Features

- On-chip PLL for clock synchronization
- On-chip loop filter for clock generation
- Low skew (±500 ps, maximum) between input and output clocks
- Low skew (±250 ps, maximum) between output clocks
- 25 MHz to 50 MHz reference frequency range
- 25 MHz to 100 MHz output frequency range
- Two-phase, non-overlapping clock generation
- TTL compatible input and output clocks
- Drop-in replacement for AV9172
- CMOS technology in 16-pin PDIP and SOIC
- 5V power supply

Description

CH9072 is a PLL clock synchronizer and multiplier designed to generate low skew clocks for clock distribution in high performance computer motherboards and workstations.

The control inputs, PCE (Phase Clock Enable) and INV* (Invert CLK1 input), determine CH9072's output state. There are six low skew outputs and the following list describes the six outputs relative to REFIN:

- one 1xf_{REFIN}
- two 2xf_{REFIN}
- one 1xf_{REFIN} that can be selected in phase or 180° out of phase with REFIN
- two output clocks programmable as 2xf_{REFIN} or as two-phase non-overlapping clocks.

CH9072 uses high performance, low power CMOS technology available in 16-pin PDIP and SOIC packages.

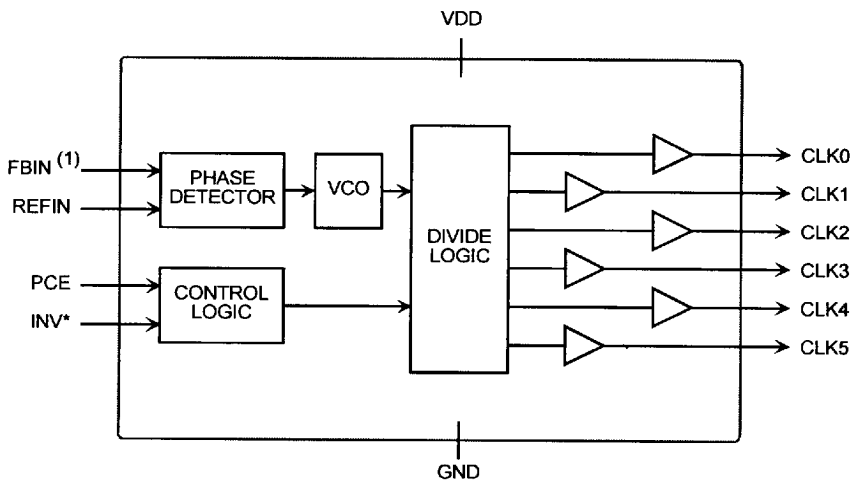

Figure 1: Block Diagram

(1) FBIN is normally connected externally to CLK0 only

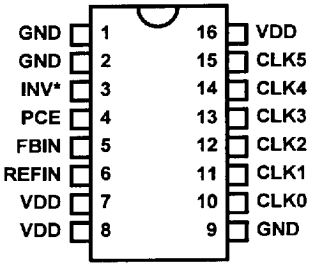

Figure 2: CH9072

Table 1 • Pin Description

Pin	Type	Symbol	Description
1, 2, 9	Power	GND	Ground
3	In	INV*	Invert CLK1 input (active low)
4	In	PCE	Phase clocks enable (active high). Converts CLK4 and CLK5 to phase clocks when asserted.
5	In	FBIN	Feedback input
6	In	REFIN	Reference clock input
7, 8, 16	Power	VDD	5V supply
10	Out	CLK0	Buffered reference clock output
11	Out	CLK1	A clock output in phase or 180° out of phase with REFIN
12	Out	CLK2	A clock output that is twice the frequency of CLK0
13	Out	CLK3	A clock output that is twice the frequency of CLK0
14	Out	CLK4	A clock output that is either a two-phase clock or a clock that is twice the frequency of CLK0
15	Out	CLK5	A clock output that is either a two-phase clock or a clock that is twice the frequency of CLK0

Note: For more information on the clock outputs, please refer to the appropriate configuration table

Table 2 • Configurations for CH9072A

PCE	INV*	CLK0	CLK1	CLK2	CLK3	CLK4	CLK5	
0	0	1x	1x*	2x	2x	2x	2x	**See Figure 3**
0	1	1x	1x	2x	2x	2x	2x	**See Figure 4**
1	0	1x	1x*	2x	2x	ϕ1	ϕ1	**See Figure 5**
1	1	1x	1x	2x	2x	ϕ2	ϕ2	**See Figure 6**

Note: 1x = indicates a duplicate output of the input reference clock REFIN
2x = indicates a clock output that is in phase and is twice the frequency of REFIN
1x* = indicates an inverted (i.e. 180° out of phase) clock output version of REFIN
ϕ1 = indicates a clock output with a duty cycle that is half the duty cycle of REFIN
ϕ2 = indicates a clock output that is a 180° out-of-phase version of ϕ1

CH9072A Timing Diagrams

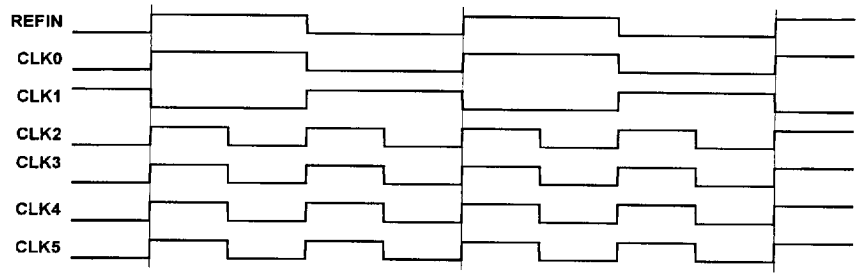

Figure 3: PCE = 0, INV* = 0

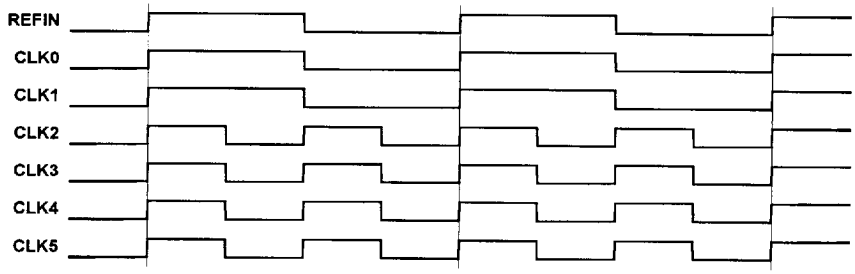

Figure 4: PCE = 0, INV* = 1

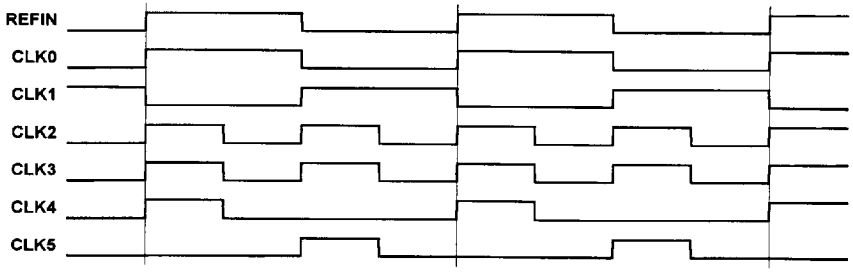

Figure 5: PCE = 1, INV* = 0

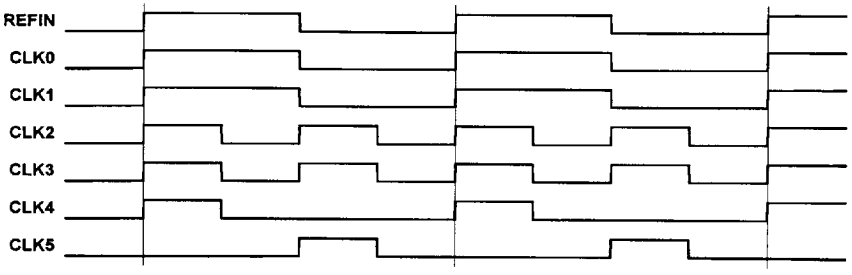

Figure 6: PCE = 1, INV* = 1

Table 3 • Configurations for CH9072B (in MHz)

PCE	INV*	CLK0	CLK1	CLK2	CLK3	CLK4	CLK5
0	0	66	66	66	66	66	66
1	0	66	66	66	66	66	33
0	1	66	66	66	33	33	66
1	1	66	66	66	33	33	33

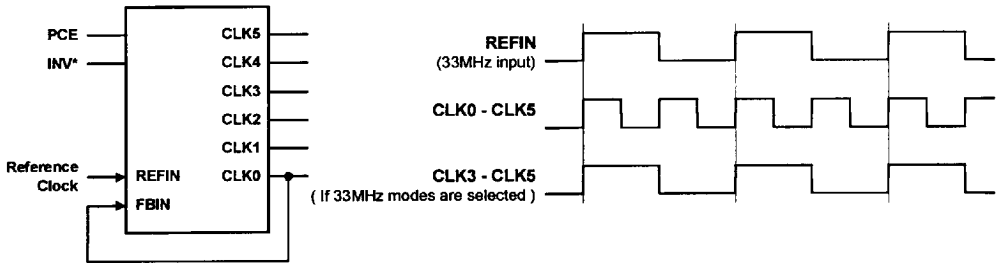

Figure 7: Timing Diagrams for CH9072B

Table 4 • Configurations for CH9072C (in MHz)

PCE	INV*	CLK0	CLK1	CLK2	CLK3	CLK4	CLK5
0	0	66	66	66	66	66	66
1	0	66	66	66	66	66	33
0	1	66	66	66	33	33	66
1	1	66	66	66	33	33	33

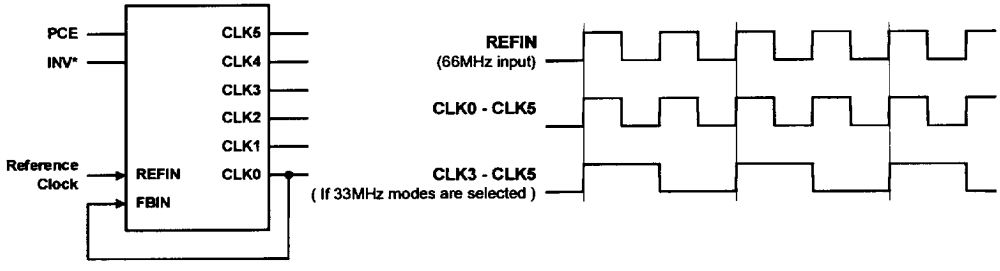

Figure 8: Timing Diagrams for CH9072C

Table 5 • Absolute Maximum Ratings

Symbol	Description	Value	Unit
VDD	Power supply voltage with respect to GND	–0.5 TO +7.0	V
VIN	Input voltage on any pin with respect to GND	–0.5 TO VDD+0.5	V
TSTOR	Storage temperature	–55 TO +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6 • DC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
VOH	Output high voltage	IOL = –25 mA	2.4			V
VOL	Output low voltage	IOL = 25 mA		0.5	0.8	V
VIH	Input high voltage	VDD = 5V	2.0			V
VIL	Input low voltage	VDD = 5V			0.8	V
IIL	Input low current	VIN = 0V	–5		5	µA
IIH	Input high current	VIN = VDD	–5		5	µA
CI	Input capacitance				10	pF
IDD	Operating current	VDD = 5V, No load, 50 MHz		35		mA

Table 7 • AC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
TIR	Input clock rise time				10	ns
TIF	Input clock fall time				10	ns
TR	Output rise time, 0.8 – 2.0V	15 pF load		0.7	1	ns
TR	Rise time, 20% – 80% VDD	15 pF load		1.2	2	ns
TF	Output fall time, 2.0 – 0.8V	15 pF load		0.7	1	ns
TF	Fall time, 80% – 20% VDD	15 pF load		1.2	2	ns
TDC	Output duty cycle	15 pF load. **Note 2**	45	49 / 51	55	%
T1S	Jitter, 1 sigma			60		ps
TABS	Jitter, absolute			±200		ps
FREFIN	Input frequency	**Note 1**	25		50	MHz
FOUT	Output frequency		25		100	MHz
TSKEW1	FBIN to REFIN skew	Input rise time <3ns. **Note 3**	–500	–300	500	ps
TSKEW1	FBIN to REFIN skew	Input rise time <10ns. **Note 3**	–1000	–500	1000	ps
TSKEW2	Skew between any two outputs at the same frequency	**Note 3**	–250	±50	250	ps
	Skew between any two outputs at different frequencies	**Note 3**			500	ps

Notes:
1. It may be possible to operate CH9072 outside these ranges. Consult Chrontel for details.
2. Duty cycle measured at 1.5V.
3. Skew measured at 1.5V on rising edges. Loading must be equal on outputs.

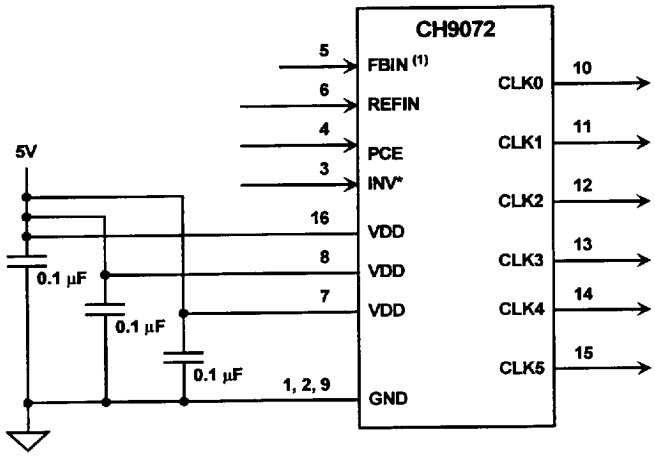

Figure 9: Application Schematic

(1) FBIN is normally connected externally to CLK0 only

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH9072x-N	300 mil PDIP	16	5V
CH9072x-S	300 mil SOIC	16	5V
Note: x = frequency table version			