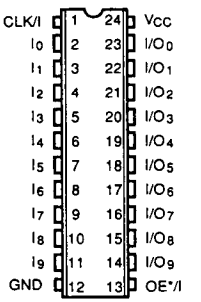
Multi-Level E²PLDs

FEATURES

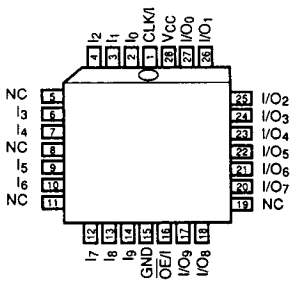
- 600-800 Gate Equivalent Logic Complexity
- Industry-Standard Data I/O ABEL™ PLD Design Tool Compatibility
- Advanced ERASIC Architecture
  - — True gate array style logic integration
  - — From 1 to 42 internal logic levels without using a pin
  - — Eliminates 2-level logic restriction of conventional PLDs
  - — 10 Buriable JK/T/D Flip-Flops
  - — Flip-flops may be connected to any logic level
  - — 2 term-controlled 4-bit input latches
  - — 64-way Programmable I/O Macrocell
- 2-Micron E²CMOS Technology
- Electrically Erasable and Programmable
  - — Reprogrammable 10,000 times (min.)
  - — Reprogrammable in plastic packages
  - — Reprogramming time less than 5 seconds, including erase and verify
  - — 100% Factory Tested
- Security Plus Provides Design Security Plus 100% Verification Capability
- High Performance
  - — 35ns Maximum One-level Propagation Delay
  - — 50ns Maximum Two-level Propagation Delay
  - — 15ns Maximum Internal Propagation Delay Per Level
- Low Power
  - — 20mA current for typical designs at 10MHz
  - — Uses power only for logic used
- Pin-compatible with 24-pin PAL® Devices
- Windowless 24-pin 300-mil DIP
- TTL and CMOS Compatible Inputs and Outputs
- 8mA/4mA Output Sink and Source Capability
- Programmable on Conventional PLD Programmers
- 5V Operation

PIN CONFIGURATION

24 Pin Skinny DIP Type "P3" Package



28 Pin PLCC Type "D" Package



PIN NAMES

I0...I9	Inputs
I/O0...I/O9	Inputs/Outputs
$\overline{OE}$/I	Output Enable/Input
CLK/I	Clock/Input

APPLICATIONS

- Programmable replacement for conventional logic families
- -LSTTL, ALS, CMOS
- Fast-turnaround, low-risk gate array alternative
- Low-power, high-functionality alternative to existing Programmable Logic Devices. One device may replace 3-4 PALs.

DESCRIPTION

The ERASIC XL78C800 is an electrically-reprogrammable CMOS ASIC component with multi-level logic capabilities. Designed to integrate a wide variety of user-defined logic functions onto a single package, this fast-turnaround ASIC device is an ideal choice when time-to-market, board space and power are at a premium.

The XL78C800 features an equivalent gate complexity of 600-800 gates packaged in a space-saving 300-mil 24-pin package. Fabricated using EXEL's high-performance double-metal E² -CMOS process, the XL78C800 typically requires a supply current of less than 20mA and may be electrically erased and programmed in less than five seconds total.

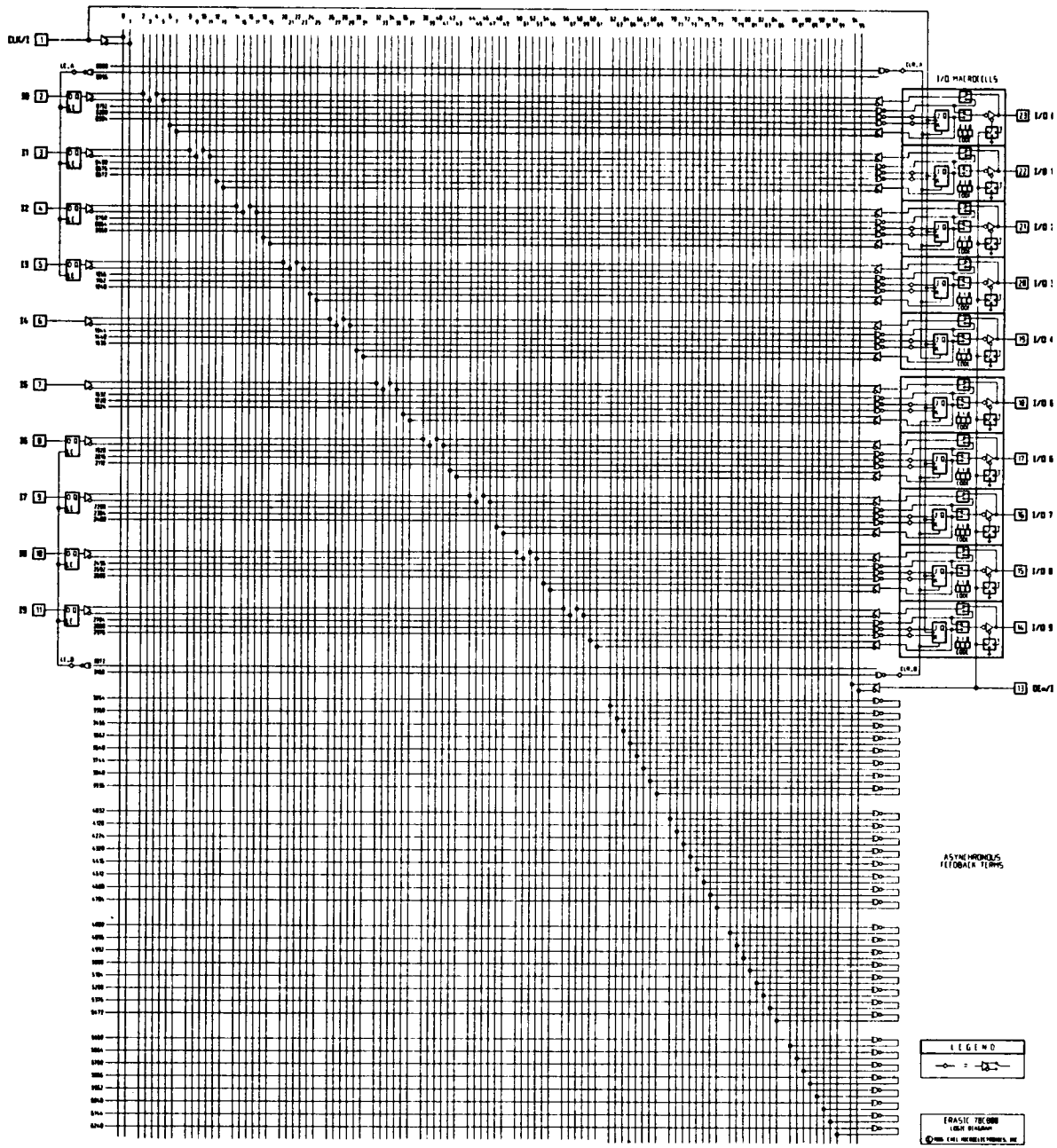


FIGURE 2. ERASIC XL78C800 LOGIC DIAGRAM

ERASIC XL78C800

The ERASIC XL78C800 is an advanced electrically-reprogrammable ASIC component designed for integration of complex user-defined logic. The XL78C800 offers multi-level logic and buriable JK Flip-Flops, thereby enhancing logic design options, increasing integration and maximizing performance.

Architectural Overview

At the heart of the ERASIC XL78C800's multi-level capabilities is the Folded-NOR architecture. This architecture, consisting of a single programmable NOR plane, can generate N internal levels of logic with N passes through the NOR plane. The folded terms, called asynchronous feedback terms, act as both array outputs and inputs, and are used to generate the multiple internal logic levels. The XL78C800 implements all combinatorial logic by using one or more NOR functions along with programmable input and output polarity.

Advantages of Multi-Level Logic

- increases design flexibility
- increases integration
- allows TTL-type design
- higher PLD utilization
- eliminates unnecessary I/O delays
- enhances design security

ERASIC XL78C800 ARCHITECTURE

The diagram in Figure 2 illustrates the key elements of the ERASIC XL78C800 architecture. The electrically-erasable NOR array consists of 96 inputs (vertical columns) by 66 terms (horizontal rows). Each term generates a NOR function of its enabled input lines. Inputs can be selectively enabled by programming the E^2PROM memory cell at the associated intersection. Each term, by selecting proper input and output polarity, can be made to operate logically (via DeMorgan's Theorem) as any 1-Level Boolean function, hence the name 'term,' not 'product term.'

Since each term can generate a generic one-level function, multi-level logic is generated simply by cascading multiple terms. The bottom-most 32 terms of the logic diagram are dedicated to this purpose. These asynchronous feedback terms feed back their output into the array as input, and allow creation of sum-of-products, product-of-sum, or higher-complexity multi-level logic functions.

The asynchronous feedback terms feed back only the NOR sense of their output and do not provide programmable output polarity. This is sufficient since next-level asynchronous logic functions which would require the OR output are easily transformed to eliminate this requirement. This transformation process is performed automatically by EXEL's AdET 1.0 software.

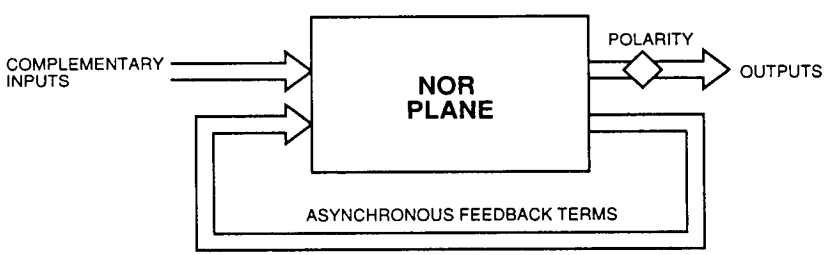


FIGURE 3A. SIMPLIFIED FOLDED-NOR ARCHITECTURE

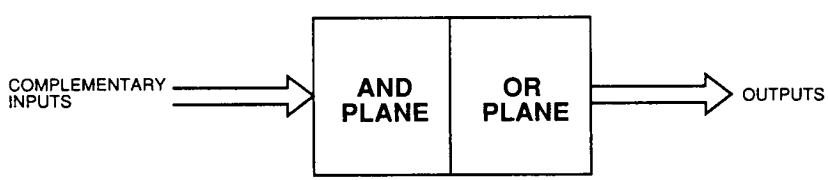
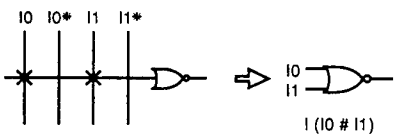


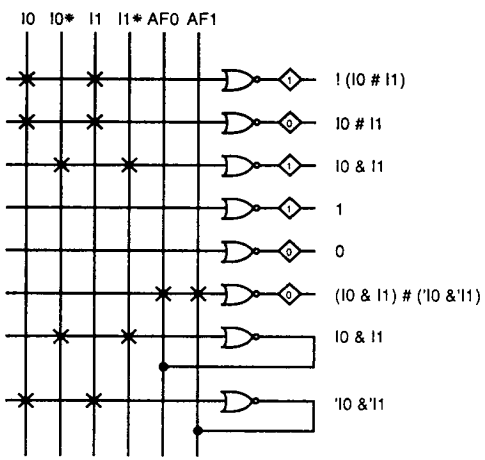
FIGURE 3B. SIMPLIFIED AND-OR ARCHITECTURE

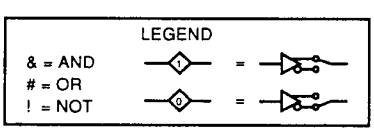
Logic Diagram Functionality

The XL78C800 logic diagram describes logic functionality in a manner similar to conventional PLD logic diagrams. An 'X' drawn at an intersection of term and input lines indicates that the input is enabled for that term. Since the XL78C800 is NOR-based, the inputs represent inputs to a NOR gate.



Addition of Polarity Control Elements (PCEs) and asynchronous feedbacks completes the basic set of array logic operators.





I/O MACROCELL ARCHITECTURE

The XL78C800's ten I/O Macrocells form an integral part of the device's logic capabilities. The three terms feeding the I/O Macrocell are called the J, K and O terms. J and K terms feed the JK Flip-Flop, while the O term is used for asynchronous output and/or asynchronous feedback. By providing dual synchronous and asynchronous logic paths, the XL78C800 allows the Flip-Flop to be used even if the I/O pin is used as an asynchronous input or output.

The I/O Macrocell architecture is detailed in Figure 4. In addition to the JK Flip-Flop, its major components are three programmable multiplexers and three polarity control elements. Each Macrocell may be independently configured via six architecture fuses. Three of the fuses set the state of the Polarity Control Elements, which are shown as diamonds. The PCE's act as inverters if their fuses are programmed to a "0," and as non-inverting buffers if programmed to a "1."

CONFIGURING THE I/O MACROCELLS

The remaining three architecture fuses C0, C1 and C2, set the state of the three multiplexers. The Out Mux selects either the O term or the Flip-Flop Q signal for output to the pin. The In Mux selects either the O term or the pin as an array input. The $\overline{OE}$ Mux selects either the $\overline{OE}$ input (pin 13), a fixed 0, or a fixed 1 as the output driver enable. The C2, C1 and C0 fuses are logically decoded into the four required Mux control signals, allowing the Macrocells to be configured simply by selecting a 3-bit code. The eight Macrocell configurations and their fuse codes are summarized below and illustrated in Figure 5. Note the availability of the 0 term as an additional asynchronous feedback in many of the configurations.

I/O Macrocell Fuse Codes

CONFIGURATION	CODE [C2, C1, C0]
O Term Output	011
O Term 3-State Output	111
Q Output	010
Q 3-State Output	110
Pad Input	000
Pad Input/O Term 3-State Output	101
Pad Input/Q 3-State Output	100
No Connect	001

The $\overline{OE}$ input pin is used as the Output Enable for Macrocell configurations with 3-State Outputs. When asserted, $\overline{OE}$ enables the selected outputs; when negated, $\overline{OE}$ disables the selected outputs (Hi-Z). $\overline{OE}$ has no effect on Macrocells in other configurations.

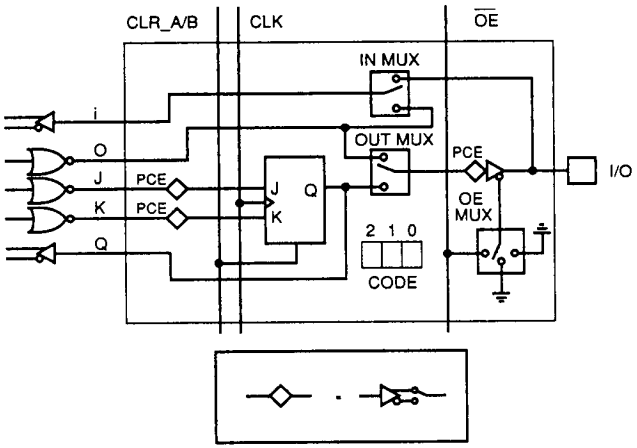


FIGURE 4. XL78C800 I/O MACROCELL

JK FLIP-FLOP OPERATION

The JK Flip-Flop is positive-edge triggered. The J and K inputs are driven by the J and K Terms, whose polarity is configured via two polarity control elements. The Q output is unconditionally fed back into the array and may additionally drive the pad via the programmable output driver. All Flip-Flops are initialized at power-up with Q set to 0. In addition, two asynchronous clear terms can be used to clear the Flip-Flops during logic operation. CLR_A clears the Flip-Flops within Macro-cells 0 through 4, while CLR_B clears the Flip-Flops within Macrocells 5 through 9.

JK Flip-Flop Operation

CLEAR	J	K	CLK	Q
1	X	X	X	0
0	0	0	↑	hold
0	0	1	↑	0
0	1	0	↑	1
0	1	1	↑	toggle

The JK Flip-Flop can easily emulate either a D or T Flip-Flop. For a D Flip-Flop, the J and K inputs are supplied with the D and $\overline{D}$ values respectively. Similarly, for a T Flip-Flop, the J and K inputs are both supplied with the T input value. The JK-to-D translation is done automatically in the AdET 1.0 design tool software.

TERM-CONTROLLED INPUT LATCHES

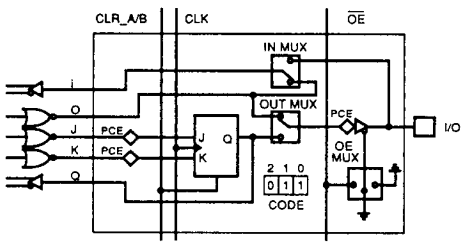
Inputs I0..I3 and I6..I9 serve as latchable 4-bit input ports. The latching of these ports is controlled by the LE_A and LE_B Terms, respectively. When LE is LOW, the latches are transparent and the Q outputs asynchronously follow the D inputs. When LE goes HIGH, data at the D inputs will be retained at the Q outputs until LE returns LOW.

The Latchable Input Ports are designed to provide a "snapshot" capability for asynchronously changing input signals that must be sensed at a particular point in time. The ports contain specially designed latches which quickly resolve the input levels when LE is asserted, providing unconditional stability regardless of the input signal characteristics.

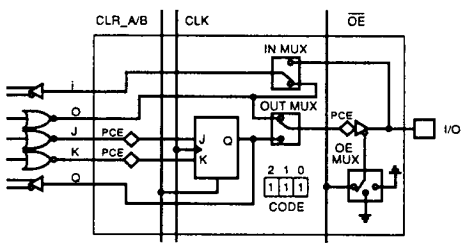
Each LE Term has programmable polarity via a Polarity Control Element. Additionally, if a Latchable Input Port is not required for a particular design, it can be made permanently transparent by programming its LE Term to a fixed LOW. Input latches are not cleared at power-up.

SECURITYPLUS SYSTEM

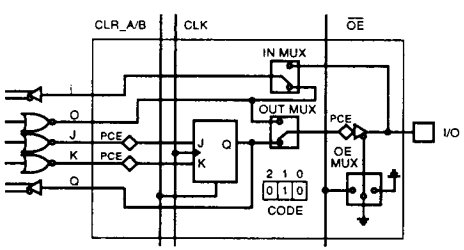
The XL78C800 incorporates an advanced design security system which offers a high-level of design copy-protection while maintaining 100% programming verification. SecurityPlus can be enabled by setting a special security E^2 cell during programming. When activated, it prevents the logic configuration from being read out or from being



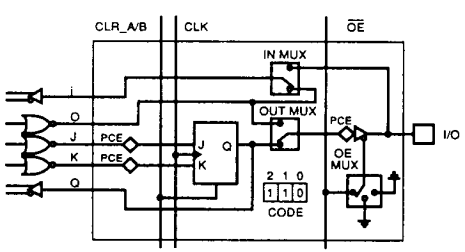
O Term Output



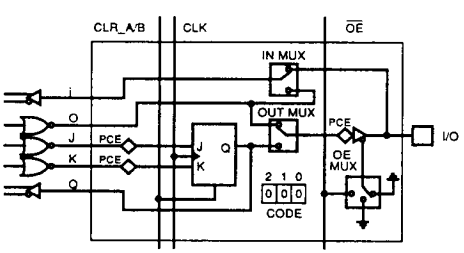
O Term 3-State Output



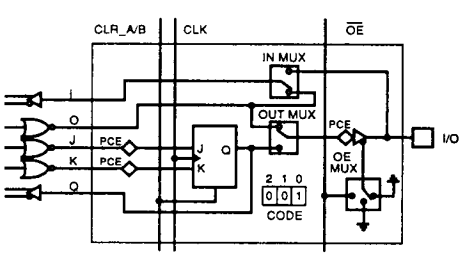
Q Output



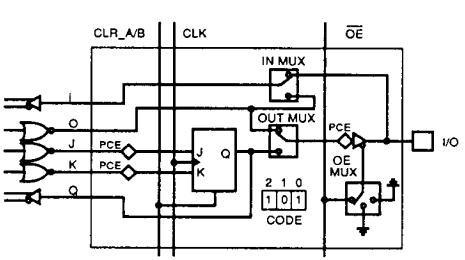
Q 3-State Output



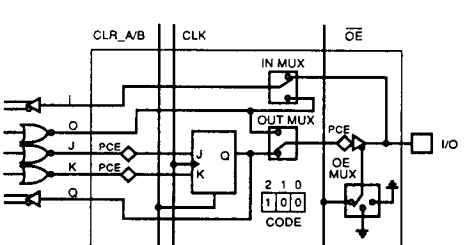
Pad Input



No Connect



O Term 3-State Output/Pad Input



Q 3-State Output/Pad Input

FIGURE 5. I/O MACROCELL CONFIGURATIONS

modified via additional programming. Only a complete erasure will disable the security. In addition, the XL78C800's E^2PROM technology eliminates the possibility of reverse-engineering via optical inspection, since programming does not create the blown fuses of bipolar fuse-link PLDs.

The SecurityPlus system is not activated until the first power-up following programming of the security bit. This allows the entire device, including the security bit itself, to be read out and verified as long as Vcc is maintained.

REGISTER PRELOAD

The XL78C800 incorporates an externally controlled preload function. Raising the CLOCK input to 12V causes any currently enabled outputs to be disabled. A preload value can then be placed on the I/O pins and will be preloaded into the JK Flip-Flops in the I/O Macrocells at the next rising edge of the clock. Thereafter, the device will return to normal operation.

ERASIC DESIGN TOOLS

Logic designs using the ERASIC XL78C800 can be created with the AdET 1.0 programmable logic development software. AdET is available from EXEL Microelectronics.

ERASIC PROGRAMMING TOOLS

The ERASIC XL78C800 may be programmed via industry-standard PLD programmers such as those offered by DATA I/O. The Data I/O Generic PLD adapter (Version 3) is required for the XL78C800.

EXEL also offers an ERASIC programming system for IBM-PC, XT, AT and compatibles and Sun Workstations. For further information please contact EXEL directly.

LOGIC DESIGN WITH THE ERASIC XL78C800

Logic design techniques for the ERASIC XL78C800 are illustrated in the 'ERASIC Sampler' circuit of Figure 6. This single-chip design contains numerous circuits ranging in complexity, and is shown in AdET form, along with schematics for reference.

One-Level Logic

The first Sampler circuit is a basic 4-input AND gate, in which IO_0 is the AND of I0..I3. The AdET notation for this circuit is simply:

IO_0 = I0 & I1 & I2 & I3; "AND"

Thus, pin 23 (which has been named IO_0) will be an AND function of pins 2, 3, 4 and 5 (which have been named 10, 11, 12, and 13). That is all that's needed, as polarity and I/O Macrocell architecture are derived automatically in the design software.

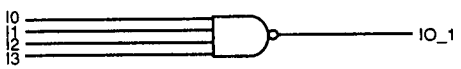
For those unfamiliar with AdET notation, the symbology is as follows:

& = AND
# = OR
! = NOT
$ = XOR

"comment" or /* comment */

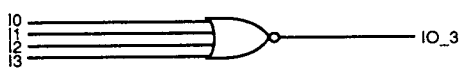
The next three circuits are similar, except they perform the NAND, OR and NOR functions, and are output on IO_1..IO_3. Like the AND, these one-level functions require a single term for implementation.

IO_1 = !(I0 & I1 & I2 & I3); "NAND"



IO_2 = I0 # I1 # I2 # I3; "OR"

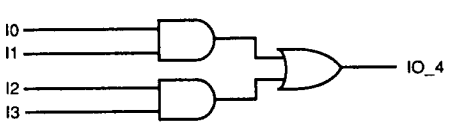
IO_3 = !(I0 # I1 # I2 # I3); "NOR"



Two-Level Logic

For two-level Sum-of-Products (SOP) functions, one enters equations as with conventional two-level PLDs.

IO_4 = (I0 & I1) # (I2 & I3);
"Sum-of-Products"



AdET automatically assign asynchronous feedbacks to achieve this two-level function. Feedbacks generate the first-level product terms. These terms are then summed by the 0 term and output to the pin. Much like conventional AND-OR PLDs, the default implementation for complex logic functions in the XL78C800 is minimized sum-of-products. That is, if one defines an output pin as a function of various input pins, and that function is not a one-level

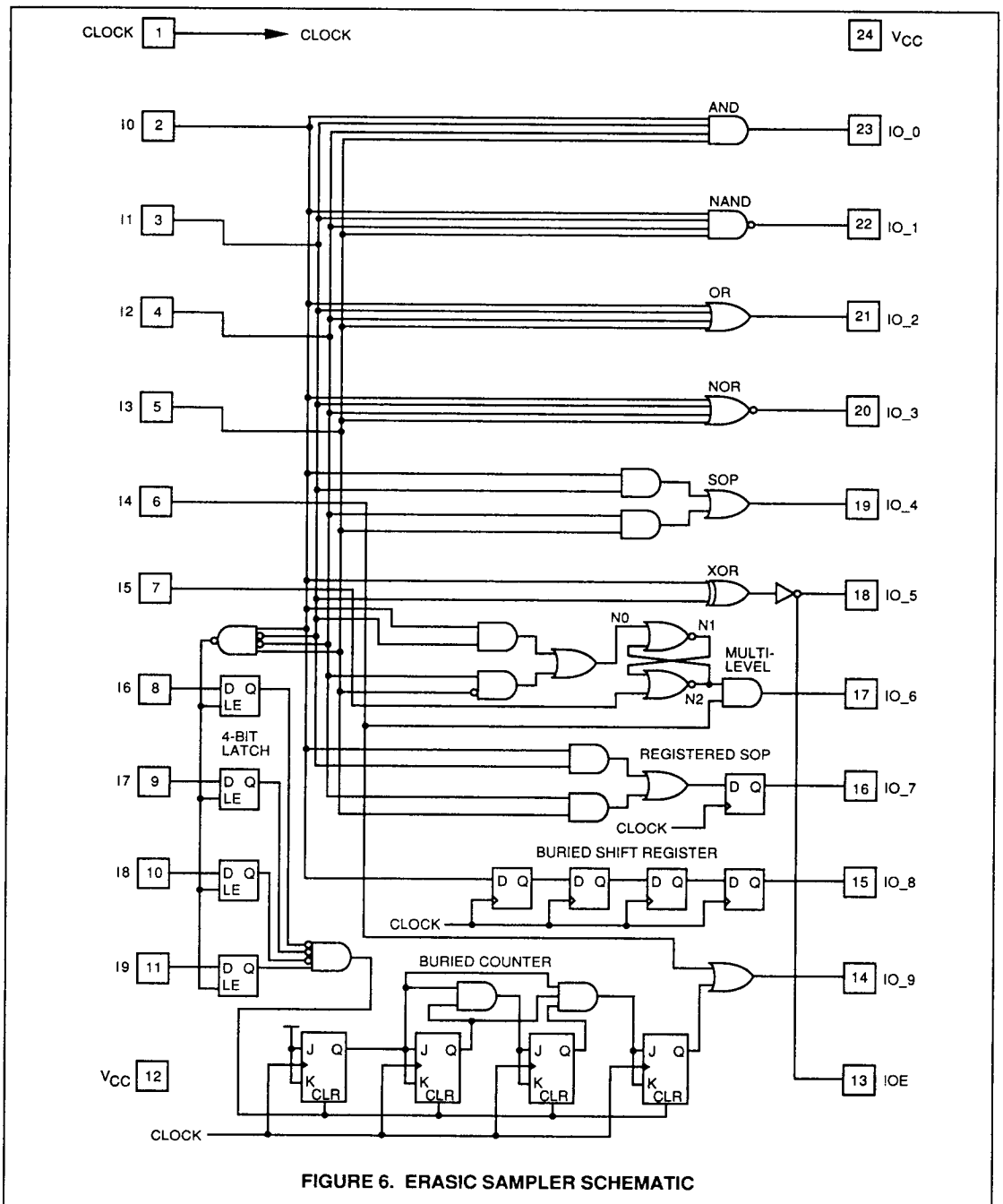


FIGURE 6. ERASIC SAMPLER SCHEMATIC

function (i.e. AND, NAND, OR, NOR), the function will be implemented as a two-level sum-of-products.

A Sum-of-Products function with an active-LOW output (AND-NOR) can be implemented by using the '!'operator on the left-hand side of the equation.

```
!IO_4 = (I0 & I1) # (I2 & I3);
"SOP, active-LOW output"
```

This function is the logical complement of previous active-high SOP function, being identical in implementation except for a complemented output polarity fuse. The Sampler design uses the active-high SOP function.

Another useful two-level function is the Exclusive-OR, which is described using the convenient XOR operator:

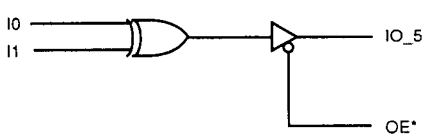
```
IO_5 = I0 $ I1; "XOR"
```

The XOR function is automatically implemented in sum-of-products form, in this case **!IO & I1 # I0 & !I1.**

If IO_5 is to be enabled only when the $\overline{OE}$ pin is brought LOW, and three-stated otherwise, one adds the statement:

```
Enable IO_5 = OE;
```

IO_5 is now enabled only when the $\overline{OE}$ signal is a 1. The fact that the $\overline{OE}$ pin is active-LOW is handled in the pin declaration by the '!' preceding the '$\overline{OE}$', allowing $\overline{OE}$ to be treated as an active-HIGH signal. (Note the distinction between pin and signal.) Any or all I/O pins can made three-state and/or bidirectional using this technique.

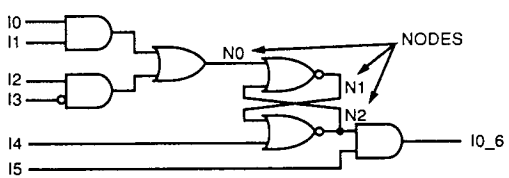


Multi-Level Logic

There are many circuits which are impossible or inefficient to implement in two or fewer levels of logic. In many cases, these circuits can be constructed using multi-level logic. Multi-level logic is logic composed of a variety of levels and interconnected in non-sequential fashion. Multi-level logic need not be a specific number of levels (e.g. two-level) and it need not be interconnected in a pre-determined, sequential fashion (e.g. AND->OR->AND->OR). It is, in effect, 'random-logic' as applied to PLDs.

Construction of multi-level logic circuits relies on the concept of nodes. Nodes are like pins, but are buried inside the device. Nodes can be given names, assigned logic functions and then used in the definition of other nodes or pins. This allows familiar PLD logic constructs to be cascaded and or interconnected in virtually any way. In addition, logic signals not needed outside the chip can stay inside, where they avoid delay and pin-usage. As an example, consider the asynchronous Set-Reset latch circuit below. Here, a cross-coupled pair of NORs is cleared when 14 is HIGH, and set when I0 and I1 are HIGH or 12 and 13 are HIGH and LOW respectively. IO_6 then outputs the latch value, asynchronously conditioned by I5. Describing this circuit requires three nodes, arbitrarily named N0, N1 and N2.

```
N0   = (I0 & I1) # (I2 &!I3);   "SR latch Set function"
N1   = (N0 # N2);               "SR latch NOR gate 1"
N2   = (I4 # N1);               "SR latch NOR gate 2"
IO_6 = I5 & N2;                 "output AND function"
```

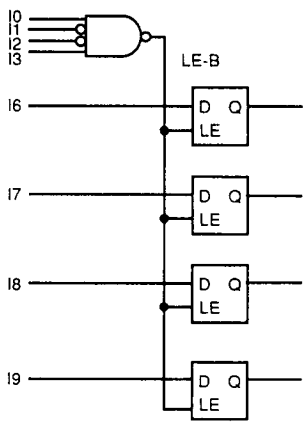


Node names are assigned in the AdET declaration section in a manner similar to pin name assignment. As is evident in the example circuit, multi-level logic is as easy to implement as fixed two-level logic, yet facilitates design of gate array and TTL-type circuits.

Input Latches

To demonstrate the use of the input latches, the Sampler adds input latches to inputs I6..I9. The latch-enable term named LE_B controls the latching, and is set into action via the statement:

```
LE_B = !(I0 & !I1 & !I2 & I3);
```



Thus, when I0..I3 are in the 1001 state, LE_B will be LOW and I6..I9 will asynchronously flow through the latches. When they are not in this state, I6..I9 will be latched. LE_B is used, in effect, as a LOW-going write strobe. Such latch constructs are especially useful when a byte or nibble needs to be latched from a data bus. Input latches are also useful in creating pipelined synchronous systems.

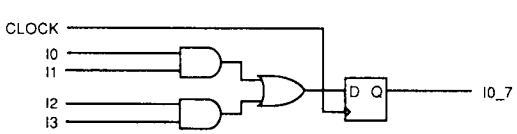
The input latches are defaulted to a fixed non-latching state. They are activated only when the LE terms are defined in the equation section. LE_A, for instance is not defined in the equation section, making I0..13 unlatched by default.

The latches are used as part of the last Sampler circuit, and are diagrammed again in that circuit.

Synchronous Logic

Synchronous logic design using the XL78C800's JK flip-flops is illustrated in three circuits. The first circuit is a registered 2-level logic function, employing an AdET notation identical to that used with conventional registered AND-OR PLDS.

```
IO_7 := (I0 & I1) # (I2 & I3);
```

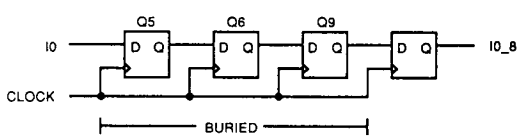


This is the implied synchronous notation of AdET, where the ' := ' operator signifies that IO_7 will be a registered function of the inputs on the right-side of the equation. The design software automatically configures the JK flip-flop as a D type, and sets the I/O Macrocell to the Q-Output configuration.

For reference, all XL78C800 flip-flops are clocked by pin 1 and are positive-edge triggered. They are cleared at power-up, and can be asynchronously cleared thereafter using the CLR_A or CLR_B terms. As with the Latch-Enable terms, the Clear terms are defaulted to a fixed inactive state when not assigned equations.

The second synchronous circuit is a 'buried' 4-bit shift register. It is so named because the flip-flops (except the last stage), are buried within the device, not requiring the use of any pins. Again, simple D flip-flops are used, but in this case, because they are buried, node names are used to identify the first three flip-flops. They are named Q5, Q6 and Q9, with the last stage outputting to the pin named IO_8. Note that because the flip-flop of I/O Macrocell 7 is used in the previous circuit, the shift register goes around that macrocell. Note also that flip-flops Q5..Q9 are cleared only a power-up, since CLR_B is defaulted to the inactive state.

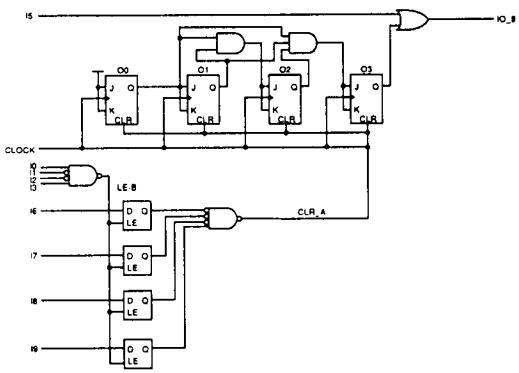
```
Q5 := 10;     "shift register stage 1"
Q6 := Q5;     "shift register stage 2"
Q9 := Q6;     "shift register stage 3"
IO_8 := Q9;   "shift register stage 4, output to pin"
```



The third and final synchronous circuit is a divide-by-16 circuit, featuring a buried 4-bit synchronous up-counter with an asynchronous 'force-HIGH' on the output. This circuit generates a frequency 1/16th that of the system clock (pin 1) on pin 14. The design uses JK flip-flops, which are assigned nodes names Q0 through Q3. The flip-flops are asynchronously cleared at power-up, or when the 4-bit latch of I6..I9 contains the nibble '0001.'

```
[ Q0.J ]  := 1;                "counter stage 1"
[ Q0.K ]  := 1;
[ Q1.J ]  := Q0;               "counter stage 2"
[ Q1.K ]  := Q0;
[ Q2.J ]  := Q0 & Q1;          "counter stage 3"
[ Q2.K ]  := Q0 & Q1;
[ Q3.J ]  := Q0 & Q1 & Q2;     "counter stage 4"
[ Q3.K ]  := Q0 & Q1 & Q2;
```

```
IO_9 = Q3 # 15;                "OR gate to output pin
Clr_A = !I6 & !I7 & !I8 & I9;
```



The J and K nodes of the flip-flop are identified using the .J and .K suffixes to the node name. Conceptually the JK flip-flop is given a node name, and then the J and K inputs of the flip-flop are individually identified via the suffixes. Even though J and K inputs themselves are not synchronous, AdET syntax requires them to be assigned functions using the ' := ' operator. If the flip-flop node name is given an equation directly (no suffixes), the flip-flop will be implemented as the default D type, as in the previous shift-register circuit.

AdET DESIGN FILE DESCRIPTION

As with any computer language, the AdET language requires certain constructs to occur in certain places. These constructs are highlighted in the ERASIC Sampler AdET design file (Figure 8). At the top are the module statement, a design title, the device name (what the JEDEC file will be called), and the device type. Following that are the pin and node name assignments. Each pin and node is assigned a unique, unchanging number. (Pin and node numbers for the ERASIC XL78C800 are detailed in Figure 7.) These numbers are then used to give the various entities names particular to the user-design. (In the Sampler, for instance, pin 1 is given the name 'Clock,' while node 49 is given the name 'NO.') Thereafter comes the EQUATION section, with the various Sampler circuits described, followed by the keyword END, completing the design.

Additional AdET Techniques

In addition to the equation-oriented design of the Sampler, AdET offers high-level constructs such as truth tables and state machines. With these constructs, only the 'what' of the design need be described, with the 'how' left to the software. High-level constructs allow logic functions to be treated as black boxes, with the derivation of the boxes' internal gate-level implementations left to AdET. The ERASIC XL78C800 fully supports all AdET high-level constructs. Additionally, it enhances the usefulness of such constructs, since it allows more of them to be placed on the same PLD, and lets them be interconnected in ways not before possible. More information on using high-level AdET design techniques is contained in the AdET manual.

Flip-Flops

Q0,Q1,Q2,Q3,Q4	node	47,45,43,41,39;
Q5,Q6,Q7,Q8,Q9	node	37,35,33,31,29;

Asynchronous Feedback Terms

AF00,AF01,AF02,AF03	node	49,50,51,52;
AF04,AF05,AF06,AF07	node	53,54,55,56;
AF08,AF09,AF10,AF11	node	57,58,59,60;
AF12,AF13,AF14,AF15	node	61,62,63,64;
AF16,AF17,AF18,AF19	node	65,66,67,68;
AF20,AF21,AF22,AF23	node	69,70,71,72;
AF24,AF25,AF26,AF27	node	73,74,75,76;
AF28,AF29,AF30,AF31	node	77,78,79,80;

Control Terms

CLR_A,CLR_B	node	27,28;
LE_A,LE_B	node	25,26;

Note: Flip-Flops Q0..Q9 are in Macrocells 0..9, respectively. Asynchronous feedback term AF00 is the topmost, AF31 the bottom-most.

FIGURE 7. XL78C800 INTERNAL NODE IDENTIFICATION IN AdET

```
module ERASIC_Sampler;

title 'ERASIC Sampler Design
       Design uses one 78C800 and contains various circuits which
          illustrate ABEL design techniques.

       Erich Goetting
       EXEL Microelectronics, Inc.'

 Sampler device 'XL78C800';

"pin declarations"

        Clock           pin 1;

        I0,I1,I2,I3     pin 2,3,4,5;      "latchable inputs"
        I4,I5           pin 6,7;
        I6,I7,I8,I9     pin 8,9,10,11;    "latchable inputs"

        IO_0, IO_1      pin 23,22;        "input/output pins"
        IO_2, IO_3      pin 21,20;
        IO_4, IO_5      pin 19,18;
        IO_6, IO_7      pin 17,16;
        IO_8, IO_9      pin 15,14;

        !OE             pin 13;           "output enable"

"node declarations"

        Q0,Q1,Q2,Q3,Q4    node  47,45,43,41,39;   "flip-flops"
        Q5,Q6,Q7,Q8,Q9    node  37,35,33,31,29;

        N0,N1,N2          node 49,50,51;  "for multi-level circuit"
        Clr_A,Clr_B       node 27,28;     "flip-flop clear terms"
        LE_A,LE_B         node 25,26;     "latch enable terms"


equations

"one-level circuits"

  IO_0 =   I0 & I1 & I2 & I3 ;   "AND"

  IO_1 = !(I0 & I1 & I2 & I3);   "NAND"

  IO_2 =   I0 # I1 # I2 # I3 ;   "OR"

  IO_3 = !(I0 # I1 # I2 # I3);   "NOR"

"two-level circuits"

  IO_4 = (I0 & I1) # (I2 & I3);  "Sum-of-Products"

  IO_5 = I0 $ I1;                "XOR"
  Enable IO_5 = OE;              "make XOR output three-state

"multi-level circuit"

   N0 = (I0 & I1) # (I2 & !I3);     "SR latch Set function"
   N1 = !(N0 # N2);                 "SR latch NOR gate 1"
   N2 = !(I4 # N1);                 "SR latch NOR gate 2"
  IO_6 = I5 & N2;                   "output AND function"

"input latches"

   LE_B = !(I0 & !I1 & (I2 & I3);


"synchronous circuits"

  "registered 2-level function"

  IO_7 := (I0 & I1) # (I2 & I3);

  "buried 4-bit shift register"

  Q5   := I0;                  " shift register stage 1"
  Q6   := Q5;                  " shift register stage 2"
  Q9   := Q6;                  " shift register stage 3"
  IO_8 := Q9;                  " shift register stage 4, output to pin"

  "divide-by-16 circuit"

  [Q0.J] := 1;                 "counter stage 1"
  [Q0.K] := 1;
  [Q1.J] := Q0;                "counter stage 2"
  [Q1.K] := Q0;
  [Q2.J] := Q0 & Q1;           "counter stage 3"
  [Q2.K] := Q0 & Q1;
  [Q3.J] := Q0 & Q1 & Q2;      "counter stage 4"
  [Q3.K] := Q0 & Q1 & Q2;

  IO_9   = Q3 # I5;            "OR gate to output pin"
  Clr_A  = !(I6 & !(I7 & (I8 & I9);

end
```

FIGURE 8. ERASIC SAMPLER AdET DESIGN FILE

XL78C800 PROGRAMMING

The XL78C800's CMOS E^2PROM technology provides the highest level of PLD programming features currently available. Electrically-erasable technology offers 100% testability and high-speed reprogrammability in plastic packages. As a result, users can perform a single incoming test procedure on these devices, regardless of their final logic configuration.

The XL78C800 employs a special ruggedized E^2PROM cell configuration, allowing it to be reprogrammed a minimum of 10,000 times, with a logic retention period of 10 years.

The XL78C800 can be erased, programmed, and verified in less than five seconds. Since all pins are used for logic functions, the XL78C800 uses the presence of V_{PP} on pin 6 (PMODE) to place the device into programming mode. Once in this mode, erase, programming, and verify operations are controlled via standard TTL-level signals.

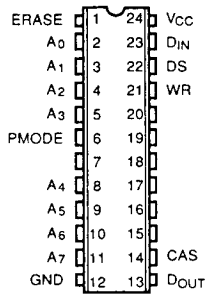


FIGURE 9. XL78C800 PIN CONFIGURATION IN PROGRAMMING MODE

PLD 5 P'DCTS

PROGRAMMING MODE PIN FUNCTIONALITY

Name	Type	Pin(s)	Description
PMODE	I	6	Programming Mode. Raising this input to V_{PP} volts places the device in the programming mode, thereby activating the pin functionality described below. If this input is below 6.0 volts, the device is in the logic mode.
A0..A3 A4..A7	I I	2..5 8..11	Address Inputs. Addresses used to select both the column and row address of all programmable cells.
CAS	I	14	Column Address Strobe. When asserted, this pin latches the current A0-A7 values into the Column Address Register, thereby selecting the column to be programmed or read. It must be asserted for the duration of any operation requiring a specific column address. When negated, CAS causes the output of the Column Address Register to asynchronously follow the A0-A7 values.
DS	I	22	Data Strobe. A LOW-HIGH-LOW transition of this pin latches the value of the Din pin into the Row Data Latch whose address is concurrently specified on A0-A7.
Din	I	23	Data Input. Data input for device programming.
Dout	O	13	Data Output. Data output for device programming verification. Valid except when WR is asserted.
ERASE	I	1	Write mode select and data latch clear. This pin has two functions. The first function is to condition the operation of the WR pin. If this pin is HIGH while WR is asserted, the chip will be unconditionally erased. If this pin is LOW while the WR pin is asserted, the data stored in the 66 Data Latches is written into the currently specified column. The second function is to clear the data latches. Whenever this pin is brought HIGH all 66 data latches will be cleared to the logic "0" state.
WR	I	21	Write. A LOW-HIGH-LOW pulse on this input causes the E^2 cells to be written, as conditioned by the state of the ERASE pin,
Vcc	I	24	+5V Power Supply. Vcc must be supplied during programming mode.
GND	I	12	Signal and Power Ground.

XL78C800 PROGRAMMING-MODE ARCHITECTURE

Referring to Figure 10, the primary programming-mode feature of the XL78C800 is the E^2 cell array. This single array stores all information defining the logic configuration of the device. The array is organized as a matrix of 66 rows by 162 columns. The 66 rows correspond to the 66 Terms in the array. The 162 columns are comprised of the 96 array input lines of the logic diagram, the architecture column, and 65 hidden 'don't care' columns. The 'don't care' columns do not appear in the logic diagram.

The address inputs, A_0-A_7, are used to specify the unique Column-Row address pair of each E^2 cell. Cells are accessed on a column-major basis. The Column Address is applied first and latched into the Column Address Register via the CAS input. The Column Address Register, in turn, selects one of the 162 columns via the Column Decoder. Following Column Address latching, Row Addresses applied to A_0-A_7 will asynchronously select E^2 cell addresses within the selected column.

Writing to the E^2 cells of a particular column is accomplished by first latching the Column Address, then strobing data into the 66 Data Latches, and then transferring the data values to the E^2 cells in the column. The Data Latches store a single bit for each of the 66-rows. Before writing new data, the Data Latches must be cleared by strobing the ERASE input. This action sets all latches to a logic "0." Each latch is written by applying the data to the Din input, applying its Row Address to A_0-A_7 and strobing the DS input. The Data Latches can be written in any order. Data Latches not written will default to a "0." Once a Data Latch is set to a "1," it can only be reset to a "0" via the ERASE strobe. When all 66 latches contain the desired data, the data is written to the E^2 cells of the selected column by pulsing the WR pin while holding ERASE at a logic "0." Columns having identical logic values for all 66 Data Latches may be written without re-entering the Data Latch values.

The 65 'don't care' columns are programmed with the NAND of the corresponding input columns, as defined in the Input Address section. A row in a don't care column is programmed to a "0" if all corresponding inputs are programmed to a "1," the logical don't care state.

Reading of the array is accomplished in a manner similar to writing. First, the ERASE pin must be strobed HIGH to enable readout. The column address is then applied and latched. Thereafter, the state of any E^2 cell within the selected column is presented asynchronously on the Dout pin.

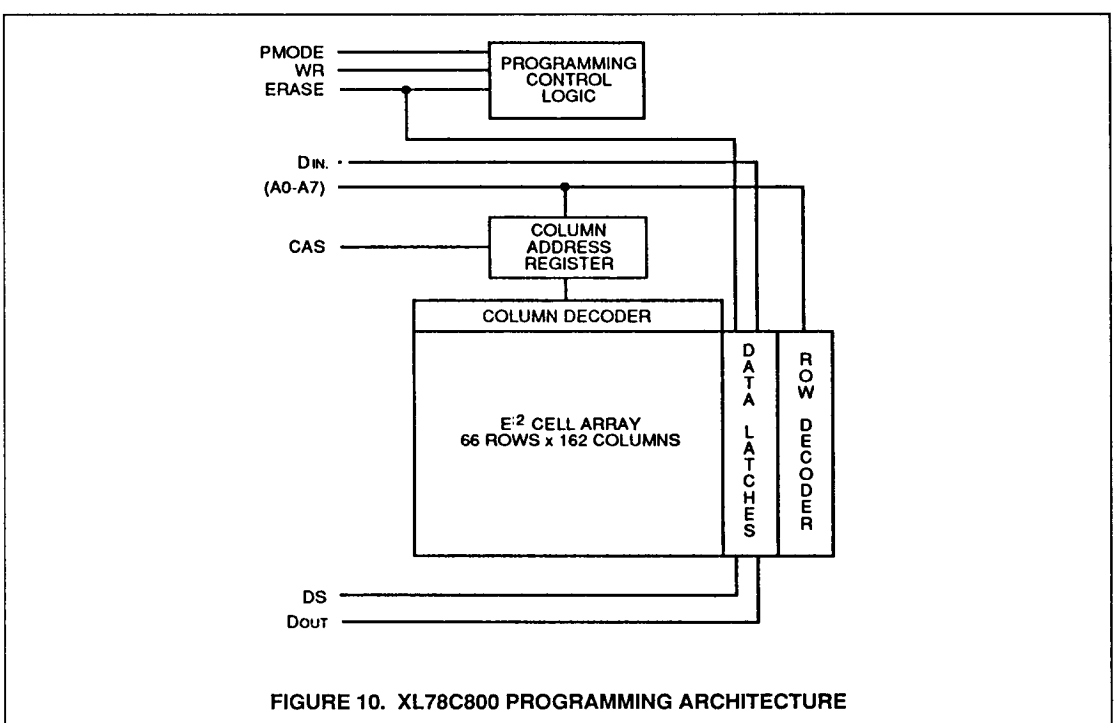


FIGURE 10. XL78C800 PROGRAMMING ARCHITECTURE

XL78C800 EE-FUSE ADDRESSES

Input Addresses

Input Name -> Column Address (HEX)

CLK	$3C	I5	$CD	AF0	$40	AF16	$8A
CLK*	$3D	I5*	$CE	AF0—	$41	AF16—	$8B
CLK—	$3E	I5—	$CF	AF1	$3A	AF17	$88
		i5	$83	AF1—	$3B	AF17—	$89
I0	$3F	i5*	$86	AF2	$38	AF18	$84
I0*	$42	i5—	$87	AF2—	$39	AF18—	$85
I0—	$43	Q5	$80	AF3	$34	AF19	$96
i0	$33	Q5*	$81	AF3—	$35	AF19—	$97
i0*	$36	Q5—	$82	AF4	$2E	AF20	$94
i0—	$37	I6	$C8	AF4—	$2F	AF20—	$95
Q0	$30	I6'	$C9	AF5	$2C	AF21	$90
Q0*	$31	I6—	$CC	AF5—	$2D	AF21 —	$91
Q0—	$32	i6	$8F	AF6	$28	AF22	$A2
I1	$44	i6*	$92	AF6—	$29	AF22—	$A3
I1*	$45	i6—	$93	AF7	$22	AF23	$AO
I1—	$46	Q6	$8C	AF7—	$23	AF23—	$A1
i1	$27	Q6'	$8D	AF8	$20	AF24	$9C
i1*	$2A	Q6—	$8E	AF8—	$21	AF24—	$9D
i1—	$2B	I7	$C7	AF9	$1C	AF25	$AE
Q1	$24	I7'	$CA	AF9—	$1D	AF25—	$AF
Q1*	$25	I7—	$CB	AFI0	$16	AF26	$AC
Q1—	$26	i7	$9B	AF10—	$17	AF26—	$AD
I2	$47	i7*	$9E	AF11	$14	AF27	$A8
I2*	$4A	i7—	$9F	AF11—	$15	AF27—	$A9
I2—	$4B	Q7	$98	AF12	$10	AF28	$BA
i2	$1B	Q7'	$99	AF12—	$11	AF28—	$BB
i2*	$1E	Q7—	$9A	AF13 .	$0A	AF29	$B8
i2—	$1F	I8	$C4	AF13—	$0B	AF29—	$B9
Q2	$18	I8'	$C5	AF14	$08	AF30	$B4
Q2*	$19	I8—	$C6	AF14—	$09	AF30—	$B5
Q2—	$1A	i8	$A7	AF15	$04	AF31	$C0
I3	$48	i8*	$AA	AF15—	$05	AF31—	$C1
I3*	$49	i8—	$AB				
I3—	$4C	Q8	$A4			OE	$BD
i3	$0F	Q8*	$A5			$\overline{OE}$	$BC
i3*	$12	Q8—	$A6			OE—	$BE
i3—	$13	I9	$BF				
Q3	$0C	I9*	$C2				
Q3*	$0D	I9—	$C3				
Q3—	$0E	i9	$B3				
I4	$4D	i9,	$B6				
I4*	$4E	i9—	$B7				
I4—	$4F	Q9	$B0				
i4	$03	Q9'	$B1				
i4*	$06	Q9—	$B2				
i4—	$07						
Q4	$00						
Q4*	$01						
Q4—	$02						

Legend: XX is true input, XX* is false input, XX— is don't care input.

Term Addresses

Term Name ->Row Address (HEX)

CLR_A	$1F	O5	$41	AF0	$14	AF17	$3B
LE_A	$20	J5	$2C	AF1	$13	AF18	$3A
O0	$04	K5	$2B	AF2	$12	AF19	$39
J0	$1D	O6	$40	AF3	$11	AF20	$38
K0	$1E	J6	$2A	AF4	$10	AF21	$37
O1	$03	K6	$29	AF5	$0F	AF22	$36
J1	$1B	O7	$3F	AF6	$0E	AF23	$35
K1	$1C	J7	$28	AF7	$0D	AF24	$34
O2	$02	K7	$27	AF8	$0C	AF25	$33
J2	$19	O8	$3E	AF9	$0B	AF26	$32
K2	$1A	J8	$26	AF10	$0A	AF27	$31
O3	$01	K8	$25	AF11	$09	AF28	$30
J3	$17	O9	$3D	AF12	$08	AF29	$2F
K3	$18	J9	$24	AF13	$07	AF30	$2E
O4	$00	K9	$23	AF14	$06	AF31	$2D
J4	$15	LE_B	$21	AF1 5	$05		
K4	$16	CLR_B	$22	AF16	$3C		

ARCHITECTURE FUSE ADDRESSES

All Architecture Information is accessed via Columns $D0 and $D1, with $D0 containing the TRUE information and $D1 containing the complement information. The row addresses of the architecture and polarity bits within these columns are given below.

O,J,K Polarity,	C2,C1,C0 for Mcell 0	$04,$1D,$IE,	$13,$12,$11
O,J,K Polarity,	C2,C1,C0 for Mcell 1	$03,$1B,$1C,	$10,$0F,$0E
O,J,K Polarity,	C2,C1,C0 for Mcell 2	$02,$19,$1A,	$0D,$0C,$0B
O,J,K Polarity,	C2,C1,C0 for Mcell 3	$01,$17,$18,	$0A,$09,$08
O,J,K Polarity,	C2,C1,C0 for Mcell 4	$00,$15,$16,	$07,$06,$05
O,J,K Polarity,	C2,C1,C0 for Mcell 5	$41,$2C,$2B,	$3C,$3B,$3A
O,J,K Polarity,	C2,C1,C0 for Mcell 6	$40,$2A,$29,	$39,$38,$37
O,J,K Polarity,	C2,C1,C0 for Mcell 7	$3F,$28,$27,	$36,$35,$34
O,J,K Polarity,	C2,C1,C0 for Mcell 8	$3E,$26,$25,	$33,$32,$31
O,J,K Polarity,	C2,C1,C0 for Mcell 9	$3D,$24,$23,	$30,$2F,$2E
CLR_A,CLR_B,	LE_A,LE_B	$1F,$22,	$20,$21
Security Fuse	$2D (column $00 only)		

Note:
[1] No E^2 Cells are present at the following silicon addresses, and therefore these addresses will always read as a "1":

1. Column: D0 Row: 14
2. Column: D1 Row: 14
3. Column: D1 Row: 2D

PROGRAMMING PROCEDURES

Programming and verification of the XL78C800 can be accomplished using the following procedures:

1. Enter Programming Mode
2. Chip Erase
3. Chip-Erase Verify
4. Column Write
5. Column Read (verification)
6. Exit Programming Mode

All procedures except 'Enter Programming Mode' must be performed while in Programming Mode. All Programming Mode control inputs (i.e. ERASE, CAS, DS, and WR) are defaulted to a negated state (OV) unless otherwise stated. The term 'strobe' is used to signify a negated-asserted-negated transition of a pin which is in the negated state. Unless otherwise stated, strobe is 10 microseconds in duration.

Enter Programming Mode

The chip is put into programming mode as follows:

1. Vcc = 4.75 to 5.25V
2. Delay = t_{PMD}
3. PMODE = V_{PP}
4. Delay = t_{CPD}

Chip Erase

Before the chip can be programmed with a new logic configuration, it must be erased to return all E^2 cells to their unprogrammed state. The chip is erased as follows:

1. ERASE = V_{IH}
2. Strobe WR for 1/2*t_{WRE}
3. Exit Programming Mode
4. Delay t_{REC}
5. Enter Programming Mode
6. ERASE = V_{IH}
7. Strobe WR for 1/2*t_{WRE}

Chip-Erase Verify

The All-Ones condition of an erased XL78C800 may be verified as follows:

1. Set address [A7:AO] = FF (hex)
2. Strobe Erase
3. Delay t_{DED}
4. If D_{OUT} = V_{IH}, then device is erased

Column Write

The Erasic device is programmed by a sequence of write operations. All columns must be correctly programmed for the device to function correctly. Each of the 162 columns in the device is written as follows:

1. Set address [A7: A0] = Column Address
2. Assert CAS to latch address into Column Address Register
3. Strobe ERASE for t_{YLSW} to clear Data Latches —this may be done concurrently with Step 2.
4. For each Row from 00 (hex) to 41 (hex):
   a. Set address [A7:A0] = Row Address
   b. Din = Data
   c. Strobe DS to latch data
5. Strobe WR for t_{WRW}
6. Delay t_{REC}
7. Negate CAS

Column Read

Programming of the device should be verified to assure proper device operation. All columns must be programmed before verification. Each of the 162 columns in the chip is verified as follows:

1. Set address [A7:A0] = Column Address
2. Assert CAS to latch address into Column Address Register
3. Strobe ERASE
4. For each row from 00 (hex) to 41 (hex):
   a Set address [A7:A0] = Row Address
   b. Delay t_{DD}
   c. Read D_{OUT}
   d. Verify if D_{OUT} = Data

Exit Programming Mode

Following Chip Erase, Chip Programming and Verifi- cation, the chip must be powered down in the following sequence.

1. ALL Control and Address pins brought to 0V This excludes PMODE, Vcc and $\overline{OE}$ (see Note)
2. PMODE = 0V
3. Delay t_{PMS}
4. $\overline{OE}$, Vcc = 0V

At all subsequent power-ups, all logic, architecture and security features will be activated.

NOTE: When PMODE is made inactive, the I/O Macrocells will again drive the pins in accordance with the configuration present at power up. In accordance with the programming procedures specified here, this will be the completely erased configuration, in which all I/O's will be in the 3-state output mode controlled by the $\overline{OE}$ pin.

Logic contention should be avoided at the D_{IN}, D_S, WR, and CAS during the period after which PMODE has been deactivated and Vcc is still active.

XL78C800 JEDEC FILE INFORMATION

Figure 11 illustrates a sample JEDEC Fuse Map for XL78C800. Each row in the Fuse Map corresponds to a Term in the logic diagram. The first 66 rows correspond to the main NOR array, with each row representing a Term. The total number of fuses in this section is 66 x 96 = 6336 fuses, with JEDEC addresses ranging from 0000 to 6335.

The 65 Architecture Fuses begin at fuse number 6336. Each I/O Macrocell is described by 6 Architecture Fuses (O polarity, J Polarity, K Polarity, C2, C1, and C0). Thereafter, four fuses describe the CLR_A, CLR_B, LE_A and LE_B Polarity control. The optional Security Fuse feature may be described in the "G" field.

L6336	
111011	(O, J, and K Polarity, C2, C1, C0 for I/O Macrocell 0)
:	
:	
001011	(O, J, and K Polarity, C2, C1, C0 for I/O Macrocell 9)
1000*	(CLR_A, CLR_B, LE_A, and LE_B Polarity)
G0*	(Security Enabled)

Architecture Fuse Detail

```
AdBT 1.00 - JEDEC      30-Oct-90  11:54 AM
JEDEC File For:  xl78c800

+-------------------------------------------------------+
! Design uses one 78C800 and contains various           !
! circuits which illustrate ABEL design techniques     !
+-------------------------------------------------------+
! Gabriel Jordan,  EXEL Microelectronics                !
+-------------------------------------------------------+ *
QP24*       N  Number of pins*
QF6400*     N  Number of fuses*

N Fuse  RAM  Data*

L0000  11111111111111111111111111111111111111111111101111101111011111011111111111111111111111111111111*
L0096  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L0192  11101111101111101111101111111111111111111111111111111111111111111111111111111111111111111111111*
L0288  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L0384  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L0480  11101111101111101111101111111111111111111111111111111111111111111111111111111111111111111111111*
L0576  11111101111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L0672  11111101111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L0768  11011111011111101111011111111111111111111111111111111111111111111111111111111111111111111111111*
L0864  11111110111111011111111111111111111111111111111111111111111111111111111111111111111111111111111*
L0960  11111110111111011111111111111111111111111111111111111111111111111111111111111111111111111111111*
L1056  11011111011111101111011111111111111111111111111111111111111111111111111111111111111111111111111*
L1152  11111110111111011111011111111111111111111111111111111111111111111111111111111111111111111111111*
L1248  11111110111111011111011111111111111111111111111111111111111111111111111111111111111111111111111*
L1344  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L1440  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L1536  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L1632  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L1728  11011111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L1824  11011111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L1920  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L2016  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L2112  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L2208  11101111101111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L2304  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L2400  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L2496  11011111101111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L2592  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L2688  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L2784  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L2880  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L2976  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L3072  11101111101111101111101111111111111111111111111111111111111111111111111111111111111111111111111*
L3168  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L3264  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L3360  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L3456  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L3552  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L3648  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L3744  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L3840  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L3936  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4032  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4128  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4224  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4320  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4416  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4512  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4608  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4704  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4800  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4896  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4992  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5088  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5184  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5280  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5376  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5472  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5568  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5664  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5760  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5856  11101111101111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5952  11111111111111101111101111111111111111111111111111111111111111111111111111111111111111111111111*
L6048  11111111111111111111111101111111111111111111111111111111111111111111111111111111111111111110111*
L6144  11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111010101*
L6240  11111111111111101111011111111111111111111111111111111111111111111111111111111111111111111111111*
L6336  111011*
L6342  000011*
L6348  011011*
L6354  111011*
L6360  000011*
L6366  001111*
L6372  101011*
L6378  101010*
L6384  101010*
L6390  001011*
L6396  1000*
C0F64*
A0B2
```

FIGURE 11. SAMPLE JEDEC FUSE MAP

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Ambient Temperature Under Bias .....-55°C to +125°C
Storage Temperature .....-65°C to +150°C
Voltage on Any Pin (Except Pins 1, 6)* (Note 2) .....-0.5V to +7.0V
Programming Mode Pin Voltage (Pin 6)* .....-0.5V to +21.25V
Preload Voltage (Pin 1)* .....-0.5V to +13.0V
DC Output Current 50mA
*With respect to ground

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Notes 3, 8, 10)

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Condition	Device Grades	Limits			Unit
				Min.	Typ.	Max.	
V_{IL}	Input Low Voltage			-0.5		0.8	V
V_{IH}	Input High Voltage			2.0		Vcc	V
I_{OL}	Output Low Current	V_{OL} = 0.5V		12	16		mA
I_{OH}	Output High Current	V_{OH} = 2.4V		-4	-8		mA
I_{OH}	Input Leakage Current-High	V_{IN} = V_{CC}				10	µA
I_{IL}	Input Leakage Current-Low	V_{IN} = 0V				-10	µA
I_{LO}	Output Leakage Current, 3-state	V_O = 0 to V_{CC}		-10		10	µA
I_{CC}	Power Supply Current	V_{IN} < 0.2V or V_{IN} > (V_{CC}-0.2V) f_{CLK} = 0 Hz to 10MHz	-35, -45		17 15	35 30	mA mA
V_{PP}	Programming Mode Voltage on PMode	(Pin 6)		20.75	21	21.25	V
I_{PP}	Programming Supply Current					1.0	mA
V_{PL}	Preload Mode Voltage on Pin 1			11	12	13	V
I_{PL}	Preload Supply Current					1.0	mA

CAPACITANCE

Symbol	Parameter	Plastic DIP/PLCC Package			Ceramic Side Brazed Package			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
C_{IN}	Input Pin Capacitance		4	6		5	7	pF
C_{ID}	I/O Pin Capacitance		4	6		5	7	pF
C_{CLK}	Clock Pin Capacitance		5	7		6	8	pF

AC ELECTRICAL CHARACTERISTICS-LOGIC MODE (Notes 4, 5, 6)

Symbol	Parameter	XL78C800-35 LIMITS Min.	Typ.	Max.	Unit
AGGREGATE TIMINGS					
tPD1L	Input Pad to Output Pad Delay, One Level Asynchronous (tPDI + tPDT + tPDO)			35	ns
tPD2L	Input Pad to Output Pad Delay, Two Level Asynchronous (tPDI + 2*tPDT + tPDO)			55	ns
tOEL	OE* Pin LOW to Output LOW-Z			15	ns
tOEH	OE* Pin HIGH to Output HIGH-Z			15	ns
tPDQP	CLK Input Pad to Q Output at I/O Pad (tPDQ + tPDO)			25	ns
tCKL	Clock LOW Time	20			ns
tCKH	Clock HIGH Time	20			ns
tCKRF	Clock Rise and Fall Time			5	ns
tCKP1	Clock Period (1 Level State Machine)	50			ns
tCLK1	Clock Frequency (1 Level State Machine)			20.0	ns
tCKP2	Clock Period (2 Level State Machine)	70			ns
tCLK2	Clock Frequency (2 Level State Machine)			14.2	ns
COMPONENT TIMINGS					
Input Timing					
tPDI	Input Buffer or Transparent Latch (LE negated) Delay			5	ns
tIS	Latch Input Set-up Time to LE Term Asserted			5	ns
tIH	Latch Input Hold Time from LE Term Asserted			0	ns
Term Timing					
tPDT	Term Input to Output Delay			20	ns
I/O Macrocell Timing					
tPDIO	Input Buffer Delay			5	ns
tPDO	Output Buffer Delay			10	ns
tJKS	J and K Input Set-up Time to Clock Pin HIGH			5	ns
tJKH	J and K Input Hold Time from Clock Pin HIGH	0			ns
tPDQ	Q Output Delay from Clock Pin HIGH			15	ns
tPDR	CLR Term Asserted to Q=O Delay			5	ns
tRR	CLR Term Negated Before Clock Pin HIGH			5	ns
tCLR	Clear Term Pulse Width (Note 9)	20			ns
Register Preload Timing					
tPLCKH	Preload Clock (Clock = VPL) HIGH Time	100			ns
tPLZ	Preload Clock HIGH to Outputs in HIGH-Z			50	ns
tPLS	Preload Data on I/O Pin Set-up Time to Clock HIGH	20			ns
tPLH	Preload Data on I/O Pin Hold Time from Clock HIGH	5		15	ns
Power-up Timing (Note 7)					
tINIT	Power-up Initialization Time			5	ms

AC ELECTRICAL CHARACTERISTICS-PROGRAMMING MODE (Note 8)

Symbol	Parameter	XL78C800 LIMITS Min.	Typ.	Max.	Unit
Program Mode Access					
t_{PMD}	V_{CC} Active to PMODE Active	5			ms
t_{CPD}	PMODE Active to any Control Pin Active	5			ms
t_{REC}	WR LOW to Any Input Change	1			ms
t_{CPS}	Control Pin Deactive to PMODE Deactive	1			ms
t_{PMS}	PMODE Deactive to V_{CC} Deactive	1			ms
Chip Erase					
t_{EWS}	ERASE Set-up Time to WR Rising Edge	200			ns
t_{DED}	Chip Erase Verify to Output Valid			200	ns
t_{WRE}	WR Pulse Width for Chip Erase	100			ms
t_{REC}	WR LOW to Any Input Change	1			ms
Row Data Latch Write Sequence					
t_{YLSW}	ERASE Pulse Width for Clearing Data Latches	100			ns
t_{EDS}	ERASE LOW to DS HIGH	100			ns
t_{AS}	Row Address Set-up Time to DS Rising Edge	100			ns
t_{AH}	Row Address Hold Time from DS Falling Edge	100			ns
t_{DIS}	D_{IN} Set-up Time to DS Pulse Rising Edge	100			ns
t_{DIH}	D_{IN} Hold Time from DS Pulse Falling Edge	100			ns
t_{DSW}	DS Pulse Width	100			ns
Column Write Cycle					
t_{CAS}	Column Address Set-up Time to CAS Rising Edge	100			ns
t_{CWS}	CAS Set-up Time to WR Rising Edge	100			ns
t_{WRW}	WR Pulse Width for Program	10			ms
t_{REC}	WR LOW to Any Input Change	1			ms
Column Read Sequence					
t_{DD}	Data Output Valid from Row Address			200	ns
Power-up Timing					
t_{INIT}	Power-up Init Time			5	ms

NOTES:

1. Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the Electrical Characteristics section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltage larger than the rated maxima.

3. All voltages are referenced to ground (GND). Parameters are valid over the specified temperature and operating supply ranges. Typical values are at 25°C, typical supply voltage and typical processing parameters.

4. The Aggregate Timing data specifies input pad to output pad delay paths for common end-user designs. Timing is characterized independently for the Input, Term, and I/O Macrocell circuits to allow the timing characteristics of arbitrary user-circuits to be ascertained. Because of the internal nature of these circuits, their propagation delays are not directly tested, but are guaranteed via pad-to-pad delay testing methodologies.

5. For AC testing, input signal levels are 0.0V and 3.0V with a transition time of 6ns maximum. All time measurements are referenced at input and output voltages of 1.5V.

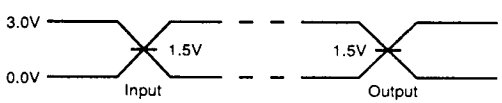
6. Delay times specified include delays through inverters, programmable inverters and multiplexers where appropriate.

7. Initialization occurs automatically at device power-up. Proper initialization requires a monotonic rise of Vcc from a voltage of 0.25V or less to the specified minimum V_{CC} voltage. Power-up initialization Time (t_{INIT}) is with respect to the point at which V_{CC} first reaches the specified minimum voltage. During the initialization period, all outputs are unconditionally placed in a high impedance state and logic operation is suspended. Once initialized, the chip will not reinitialize for V_{CC} of 3V or greater.

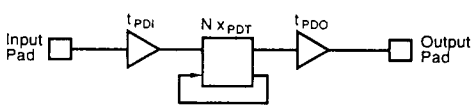
8. Programming mode voltage on PMODE Pin (6) = V_{PP}. Programming parameters are valid at temperatures of +5°C to +45°C, and at Vcc levels of 4.75 to 5.25V.

9. Minimum Clear Pulse width is always less than a one-level logic delay. Thus, one-level pulse generators can be used to clear the flip-flops.

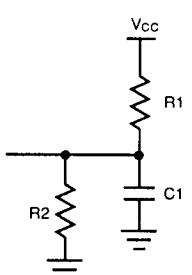
10. Maximum supply current specifications are based on test designs using all 66 terms, with a minimum of 46 terms in the LOW state at all times. Because terms which are unused or are in the HIGH state do not use current, designs which use fewer terms or which have fewer terms simultaneously LOW than the test circuit will have a lower maximum current.



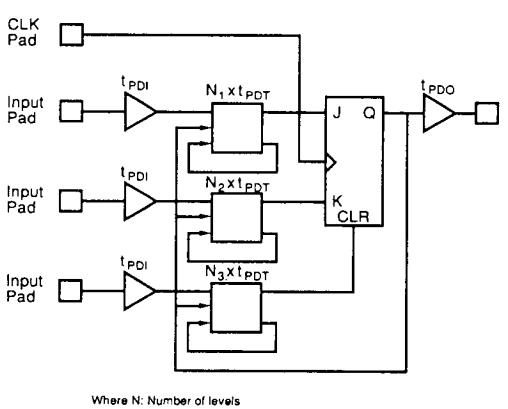
AC TESTING INPUT, OUTPUT WAVEFORM



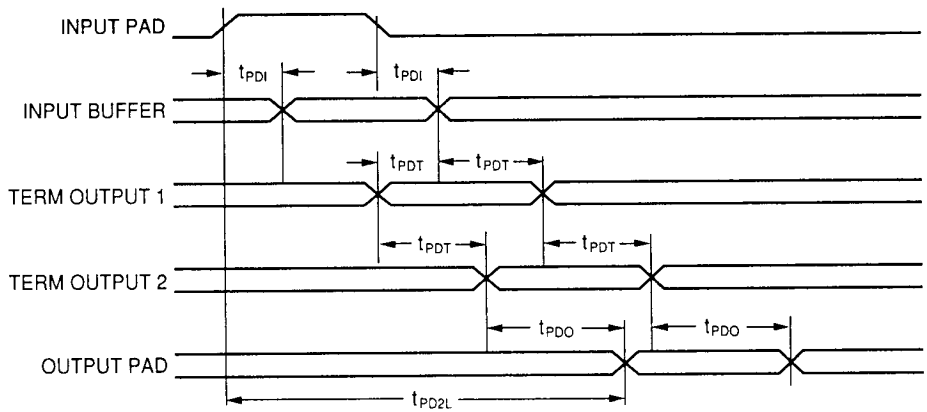
AGGREGATE INPUT PAD TO OUTPUT PAD DELAY MODEL



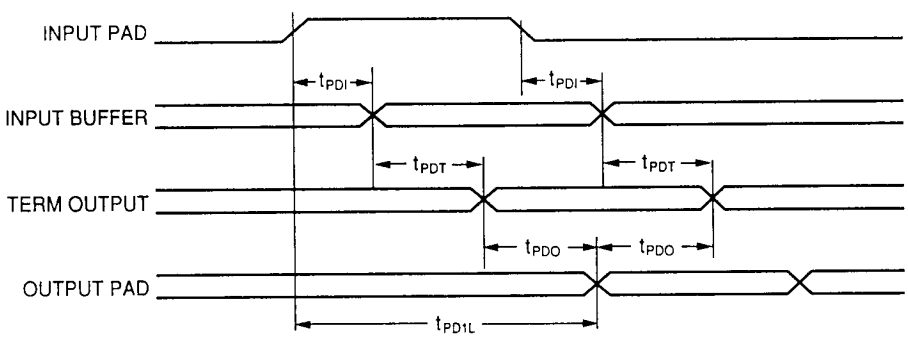
AC TESTING LOAD CIRCUIT



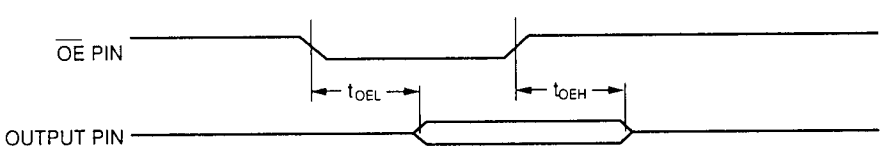
AGGREGATE SYNCHRONOUS DELAY MODEL



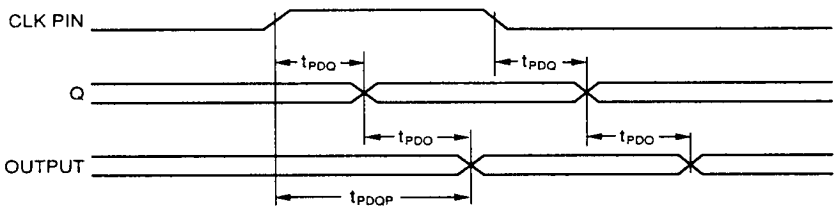
AGGREGATE INPUT PAD TO OUTPUT PAD TIMING (2-LEVEL ASYNCH)



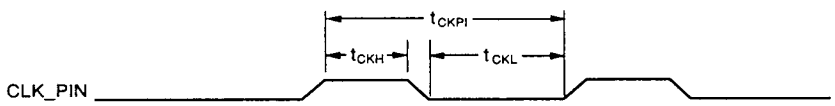
AGGREGATE INPUT PAD TO OUTPUT PAD TIMING (1-LEVEL ASYNCH)



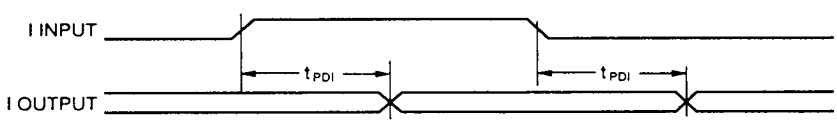
OUTPUT ENABLE DELAY



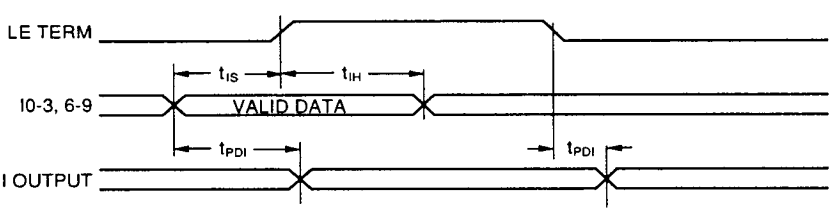
FLIP-FLOP TIMING



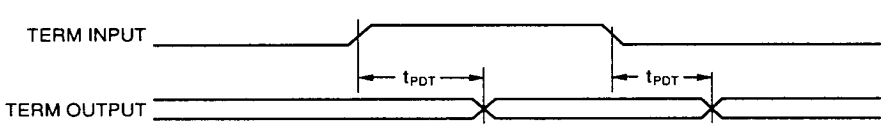
CLOCK TIMING



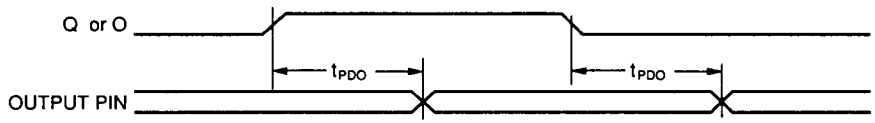
INPUT DELAY



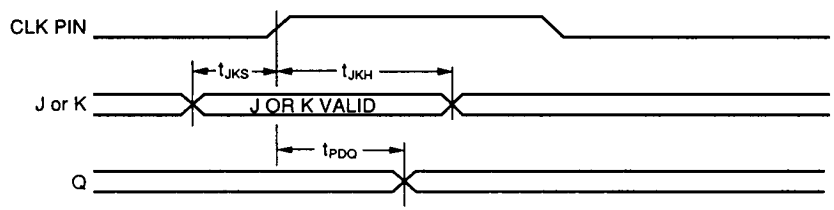
LATCH ENABLE TIMING



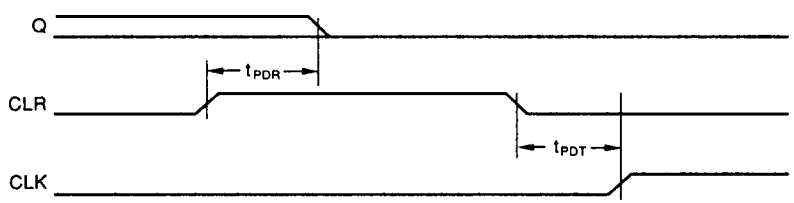
ARRAY DELAY



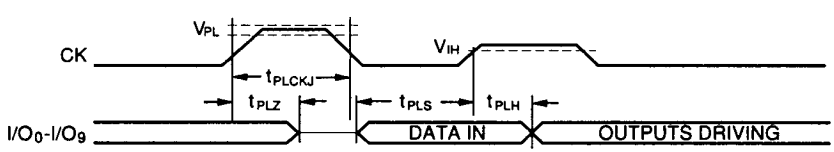
MACROCELL OUT DELAY



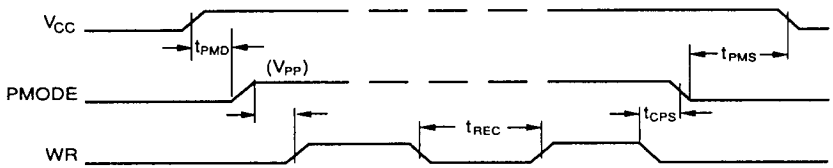
CLOCK IN TO Q OUTPUT TIMING



FLIP-FLOP RESET TIMING

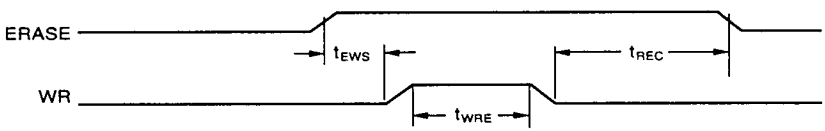


PRELOAD TIMING

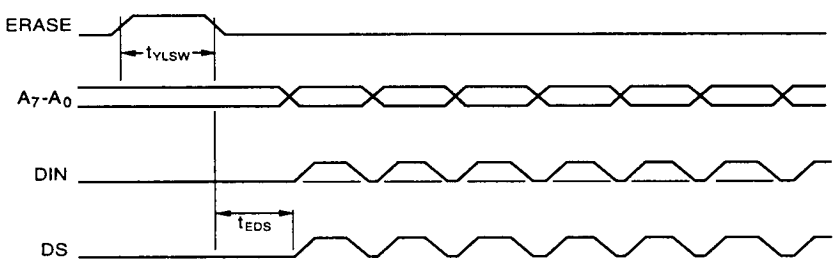


(Note: All subsequent programming timelines assume PMODE is at VPP

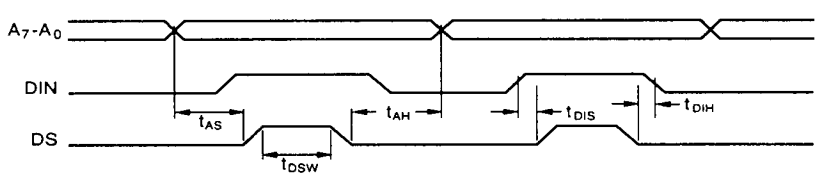
PROGRAM MODE ACCESS



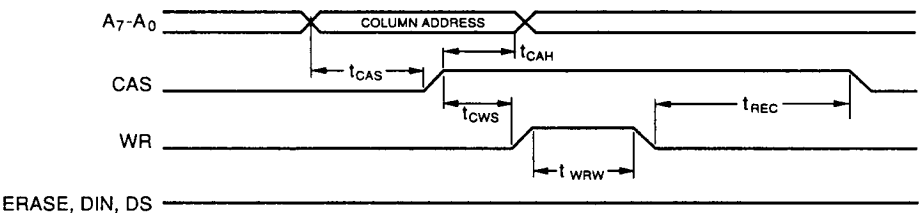
CHIP ERASE



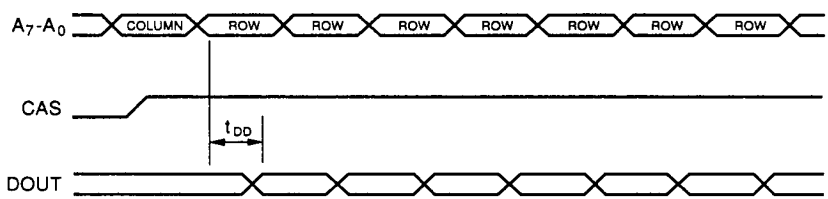
ROW DATA LATCH WRITE SEQUENCE



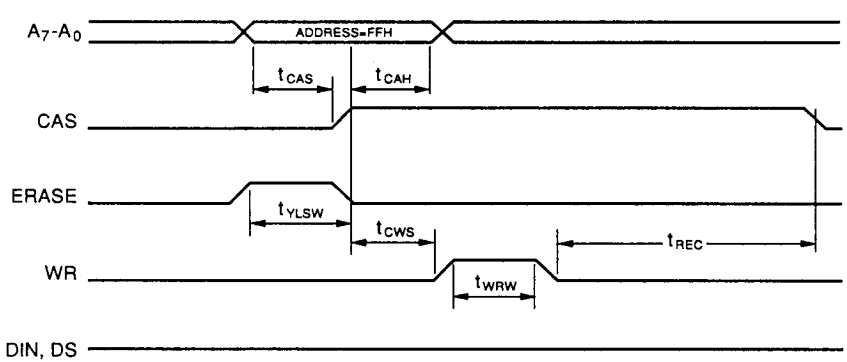
EXPANDED ROW DATA LATCH WRITE SEQUENCE



COLUMN WRITE CYCLE (NONVOLATILE WRITE)



COLUMN READ SEQUENCE



CHIP PROGRAM (ALL E^2 CELLS SET TO Lo Vt)