4. Electrical Specifications

4.1 Absolute Maximum Ratings

The following table lists absolute maximum ratings for all 87SLC devices Stresses beyond those listed in Table 4-1 may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those listed in Table 4-2 is possible. Exposure to conditions beyond the absolute maximum ratings listed in Table 4-1 can (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure Prolonged exposure to conditions at or near the absolute maximum ratings listed in Table 4-1 may also reduce useful life and reliability of the device.

Table 4-1. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Case Temperature	-25	125	°C	Power Applied
Storage Temperature	-65	150	°C	No Bias
Supply Voltage, V_{CC}	-0.5	6	V	With respect to V_{SS}
Voltage On Any Pin	-0.5	V_{CC}+0 5	V	With respect to V_{SS}
Power Dissipation		1.9	W	
Input Clamp Current, I_{IK}		10	mA	$V_I<V_{SS}$ or $V_I>V_{CC}$
Output Clamp Current, I_{OK}		25	mA	$V_O<V_{SS}$ or $V_O>V_{CC}$

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4.2 DC and AC Characteristics

Table 4-2. DC Characteristics for 87SLC (VCC = 5V ± 10%, TC = 0° to 100°C)

Symbol	Parameter	Min	Max	Units	Notes
V_{ILC}	Clock Input Low	-0.3	0.8	V	With respect to V_{SS}
V_{IHC}	Clock Input High	3.7	V_{CC}+0.3	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
I_{OH}	Output High Current		-1	mA	$V_{OH} = V_{OH(MIN)}$
I_{OL}	Output Low Current		4	mA	$V_{OL} = V_{OL(MAX)}$
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -1.0 mA
I_{LI}	Input Leakage		±15	µA	$0 < V_{IN} < V_{CC}$
I_{LO}	I/O Leakage		±15	µA	$0 < V_{O} < V_{CC}$
C_{IN}	Input Capacitance		10	pf	f_C = 1 MHz
C_{O}	I/O Capacitance		12	pf	f_C = 1 MHz
C_{CLK}	Clock Capacitance		20	pf	f_C = 1 MHz
I_{CC}	Active I_{CC} 25 MHz		320	mA	See Active I_{CC} Notes Typical = 75 mA
I_{CCAI}	Auto Idle I_{CC} 25 MHz		6.5	mA	See Idle I_{CC} Notes Typical = 2.5 mA
I_{CCSB}	Standby I_{CC} 0 MHz		0.2	mA	See Standby I_{CC} Notes Typical = 0.05 mA

Notes
Typical value is at room temperature and nominal V_{CC} of 5 0 volts Maximum value is at worst case temperature and maximum V_{CC} of 5.5 volts.

Active I_{CC} Operating Conditions
Typical value is taken during continuous execution running single precision Whetstone benchmark Maximum value is taken during continuous execution of FCOS instruction

Auto Idle I_{CC} Operating Conditions
Processor is in auto-idle mode
All inputs at 0 4 volts or (V_{CC}-0 4) Volts (CMOS levels)
Only clock switching, all other inputs static

Standby I_{CC} Operating Conditions·
Processor is in auto-idle mode
Clock stopped, all other inputs static
All inputs at 0 4 volts or (V_{CC}-0 4) Volts (CMOS levels)

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Table 4-3. DC Characteristics for 87SLCV (VCC = 2.7 to 3.6V, TC = 0° to 85°C)

Symbol	Parameter	Min	Max	Units	Notes
V_{ILC}	Clock Input Low	-0.3	0.5	V	With respect to V_{SS}
V_{IHC}	Clock Input High	V_{CC}-0.5	V_{CC}+0.3	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.3	V	
V_{IL}	Input Low Voltage	-0.3	0.6	V	
I_{OH}	Output High Current		-1	mA	$V_{OH} = V_{OH(MIN)}$
I_{OL}	Output Low Current		3	mA	$V_{OL} = V_{OL(MAX)}$
V_{OL}	Output Low Voltage		0.35	V	I_{OL} = 3.0 mA
V_{OH}	Output High Voltage	V_{CC}-0.4		V	I_{OH} = -1.0 mA
I_{LI}	Input Leakage		±15	µA	$0 < V_{IN} < V_{CC}$
I_{LO}	I/O Leakage		±15	µA	$0 < V_{O} < V_{CC}$
C_{IN}	Input Capacitance		10	pf	f_C = 1 MHz
C_{O}	I/O Capacitance		12	pf	f_C = 1 MHz
C_{CLK}	Clock Capacitance		20	pf	f_C = 1 MHz
I_{CC}	Active I_{CC} 25 MHz		170	mA	See Active I_{CC} Notes Typical = 50 mA
I_{CCAI}	Auto Idle I_{CC} 25 MHz		3.5	mA	See Idle I_{CC} Notes Typical = 1.0 mA
I_{CCSB}	Standby I_{CC} 0 MHz		0.1	mA	See Standby I_{CC} Notes Typical = 0.025 mA

Notes
Typical value is at room temperature and nominal V_{cc} of 3 0 volts Maximum value is at worst case temperature and maximum V_{cc} of 3 6 volts

Active I_{cc} Operating Conditions
Typical value is taken during continuous execution running single precision Whetstone benchmark Maximum value is taken during continuous execution of FCOS instruction

Auto Idle I_{cc} Operating Conditions
Processor is in auto-idle mode
All inputs at 0 4 volts or (V_{cc}-0 4) Volts (CMOS levels)
Only clock switching, all other inputs static

Standby I_{cc} Operating Conditions
Processor is in auto-idle mode
Clock stopped, all other inputs static
All inputs at 0 4 volts or (V_{cc}-0 4) Volts (CMOS levels)

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Table 4-4. AC Characteristics for 87SLC (V_{CC} = 5V ± 10%, T_C = 0° to 100°C)

Signal	Sym	Parameter	25 MHz (ns)		Fig.	Notes
			Min	Max		
CPUCLK2	T1	Period	20	∞	4 1	at 2.0 V
CPUCLK2	T2a	High Time	7			at 2.0 V
CPUCLK2	T2b	High Time	4			at 3.7 V
CPUCLK2	T3a	Low Time	7			at 2.0 V
CPUCLK2	T3b	Low Time	5			at 0.8 V
CPUCLK2	T4	Fall Time		7		3.7 to 0.8 V
CPUCLK2	T5	Rise Time		7		0.8 to 3.7 V
READYO#	T7	Out Delay	3	21	4 2	C_L = 75 pF
PEREQ	T7	Out Delay	4	33		
BUSY#	T7	Out Delay	4	27		
ERROR#	T7	Out Delay	4	33		
D15-D0	T8	Out Delay	0	27	4.3	C_L = 120 pF
D15-D0	T10	Setup Time	8			
D15-D0	T11	Hold Time	11			
D15-D0	T12	Float Time	5	24		C_L = 120 pF
PEREQ	T13	Float Time	1	35	4.4	C_L = 75 pF
BUSY#	T13	Float Time	1	35		
ERROR#	T13	Float Time	1	35		
READYO#	T13	Float Time	1	35		
ADS#	T14	Setup Time	14		4 3	
ADS#	T15	Hold Time	4			
READY#	T16	Setup Time	8			
READY#	T17	Hold Time	4			
CMD0#,W/R#, NPS1#,NPS2	T16	Setup Time	15			
CMD0#,W/R#, NPS1#,NPS2	T17	Hold Time	0			
STEN	T16	Setup Time	14			
STEN	T17	Hold Time	2			
RESETIN	T18	Setup Time	10		4.5	
RESETIN	T19	Hold Time	3			

Note All timing is measured from I/O signals at 1 5V and CPUCLK2 at 2 0V for a 5V supply system

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Table 4-5. AC Characteristics for 87SLCV (V_{CC} = 2.7 to 3.6V, T_C = 0° to 85°C)

Signal	Sym	Parameter	25 MHz (ns)		Fig.	Notes
			Min	Max		
CPUCLK2	T1	Period	20	∞	4 1	at 1 5 V
CPUCLK2	T2a	High Time	7			at 1 5 V
CPUCLK2	T2b	High Time	4			at V_{CC}-0 5V
CPUCLK2	T3a	Low Time	7			at 1 5 V
CPUCLK2	T3b	Low Time	5			at 0.5 V
CPUCLK2	T4	Fall Time		7		V_{CC}-0 5 to 0 5V
CPUCLK2	T5	Rise Time		7		0 5 to V_{CC}-0.5V
READYO#	T7	Out Delay	3	21	4.2	C_L = 50 pF
PEREQ	T7	Out Delay	4	33		
BUSY#	T7	Out Delay	4	27		
ERROR#	T7	Out Delay	4	33		
D15-D0	T8	Out Delay	0	27	4 3	C_L = 75 pF
D15-D0	T10	Setup Time	8			
D15-D0	T11	Hold Time	11			
D15-D0	T12	Float Time	5	24		C_L = 75 pF
PEREQ	T13	Float Time	1	35	4 4	C_L = 50 pF
BUSY#	T13	Float Time	1	35		
ERROR#	T13	Float Time	1	35		
READYO#	T13	Float Time	1	35		
ADS#	T14	Setup Time	14		4 3	
ADS#	T15	Hold Time	4			
READY#	T16	Setup Time	8			
READY#	T17	Hold Time	4			
CMD0#,W/R#, NPS1#,NPS2	T16	Setup Time	15			
CMD0#,W/R#, NPS1#,NPS2	T17	Hold Time	0			
STEN	T16	Setup Time	14			
STEN	T17	Hold Time	2			
RESETIN	T18	Setup Time	10		4 5	
RESETIN	T19	Hold Time	3			

Note All timing is measured from I/O signals at 1 2V and CPUCLK2 at 1 5V for a 5V supply system

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4.3 Interface Timing Diagrams

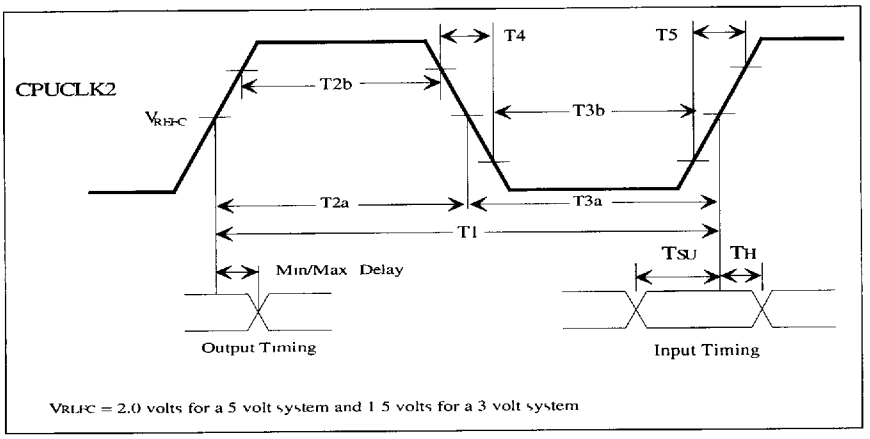

Figure 4-1. CPUCLK2 Timing and I/O Measurement Points

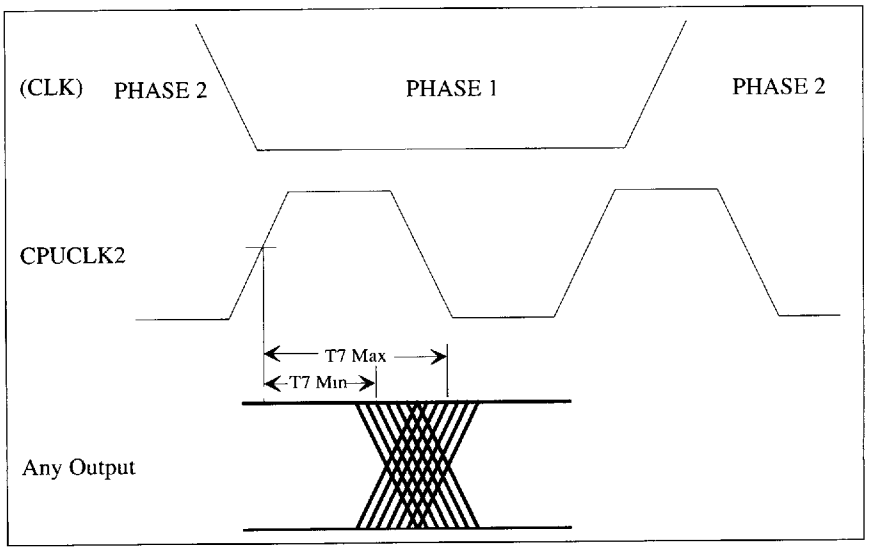

Figure 4-2. Output Timing

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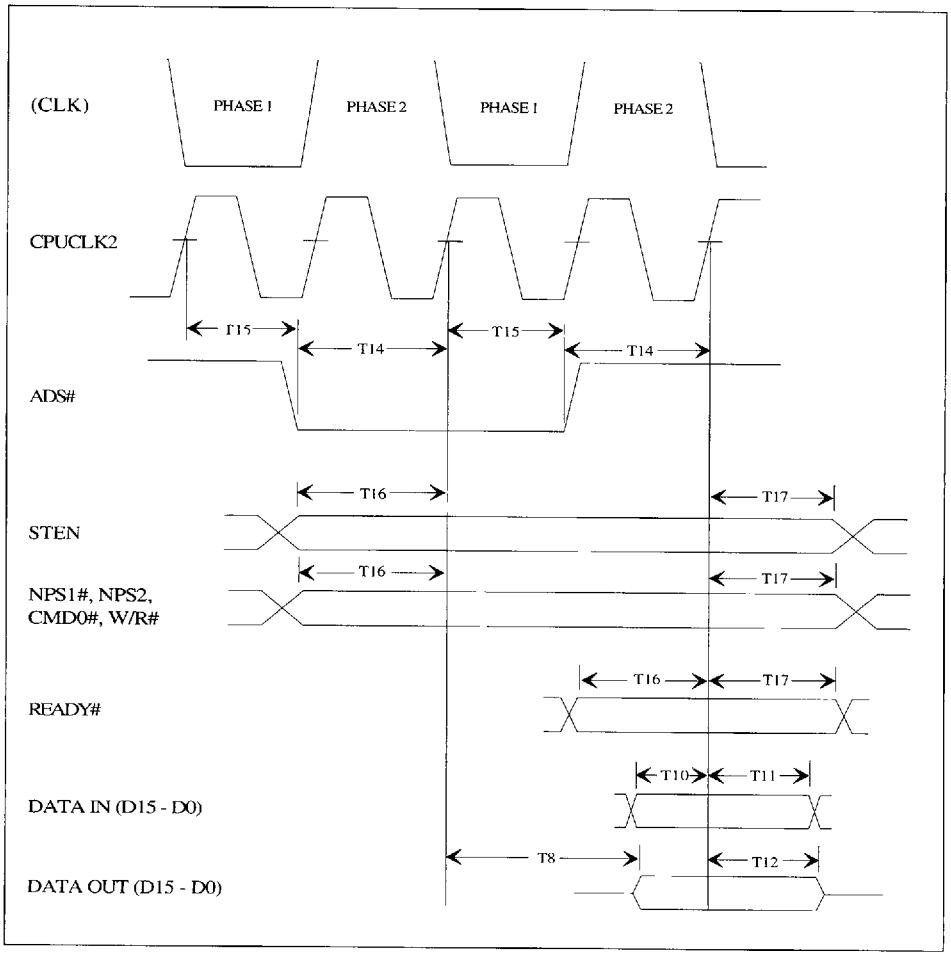

Figure 4-3. Data I/O Control Signal Timing

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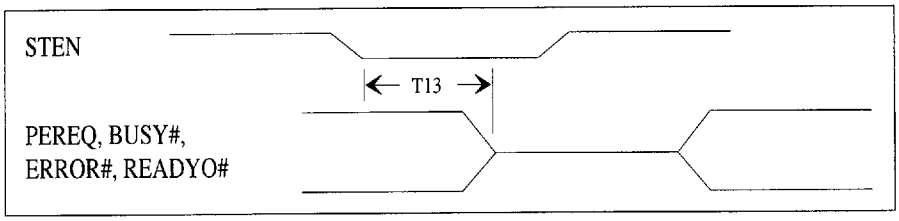

Figure 4-4. STEN Timing

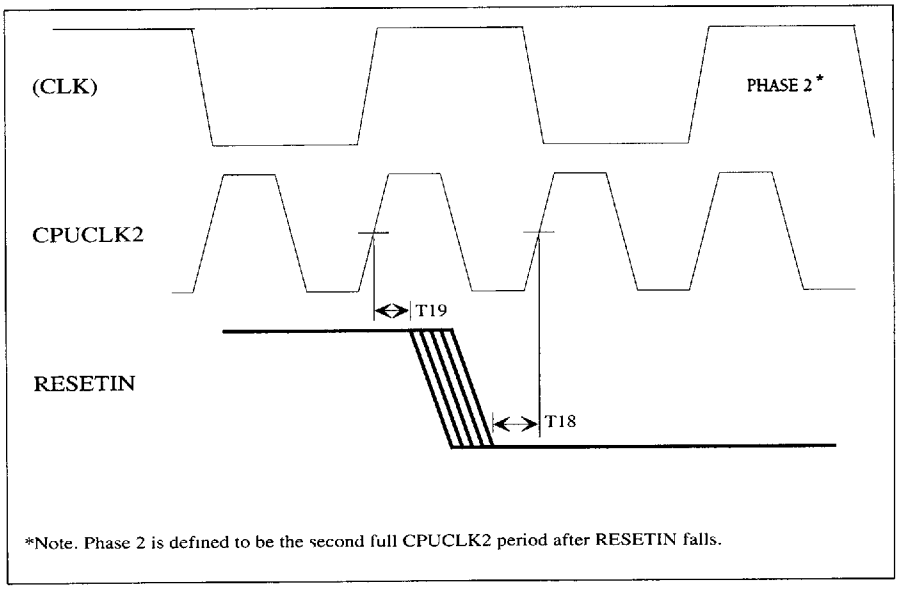

Figure 4-5. Reset Timing

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4.4 Functional Timing Parameters

Table 4-6 lists the functional timing requirements for 87SLC bus interface. This table references timing diagram Figure 4-6.

Table 4-6. Interface Timing Parameters

Signal	Symbol	Parameter	CPUCLK2 Clock Cycles		Notes
			Min	Max	
RESETIN	T20	Time Active	20		
RESETIN	T21	Time Inactive	8		Before first opcode write
BUSY#	T22	Time Active	6		
BUSY#	T23	Delay Inactive	6		From ERROR# transition
ERROR#	T24	Delay Active	6		From PEREQ inactive
BUSY#	T25	Delay Active		4	From READY# active
READY#	T26	Delay	4		Opcode write to next cycle
READY#	T27	Delay	4		Operand cycle to next operand cycle

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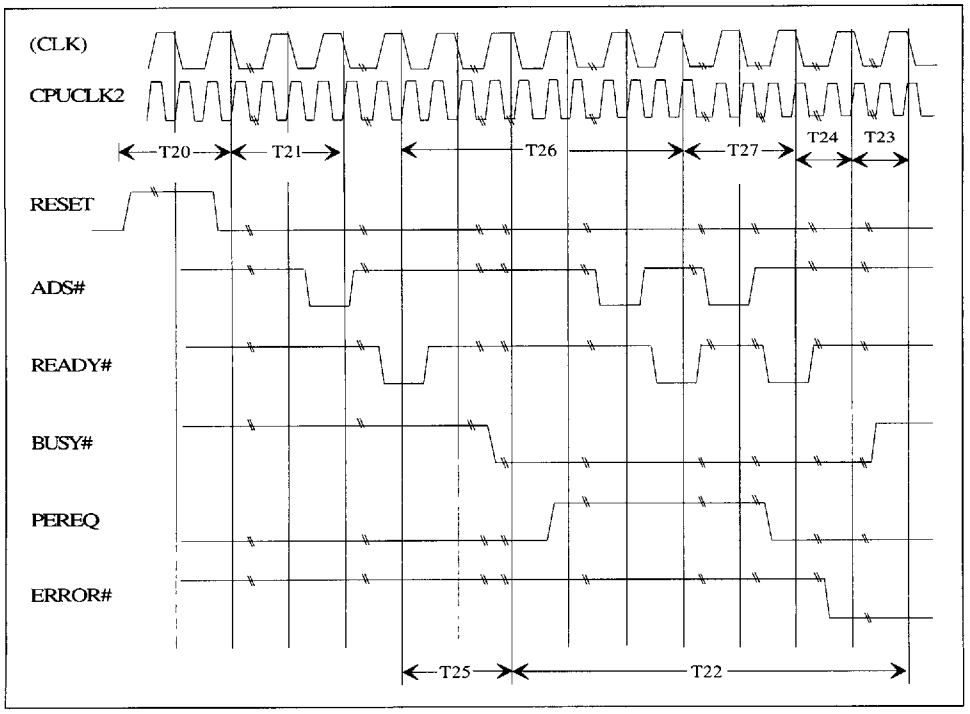

Figure 4-6. Functional Timing Diagram

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5. Mechanical Specifications

The standard package for the 87SLC coprocessor is an EIAJ standard 14x14 mm 80-lead quad flat pack.

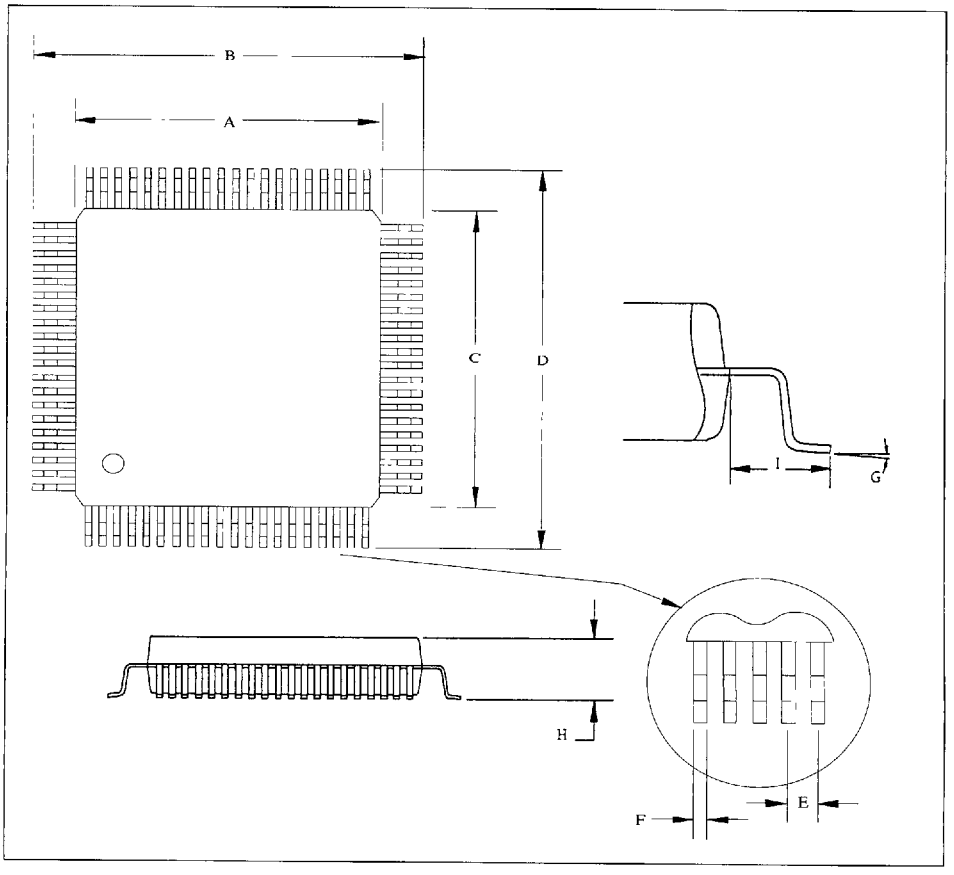

Figure 5-1. Package Outline (80-Pin PQFP)

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Table 5-1. Package Demensions (80-Pin PQFP)

DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A		0 551 REF			14.0 REF	
B	0 669	0.677	0.693	16.9	17.2	17.5
C		0.551 REF			14.0 REF	
D	0.669	0.677	0.693	16.9	17.2	17.5
E		0.026 REF			0.65 REF	
F	0.01	0.012	0.014	0.25	0.3	0.35
G	0 DEG		10 DEG	0 DEG		10 DEG
H			0.12			3.05
I		0.063			1.6 REF	

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