Complementary Power Darlingtons

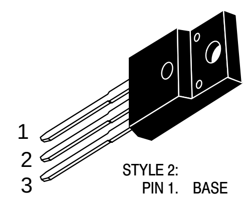
For Isolated Package Applications

NPN
MJF122
PNP
MJF127

COMPLEMENTARY SILICON POWER DARLINGTONS 5 AMPERES 100 VOLTS 30 WATTS

Designed for general–purpose amplifiers and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Electrically Similar to the Popular TIP122 and TIP127
- 100 $V_{CEO(sus)}$
- 5 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High DC Current Gain — 2000 (Min) @ I_C = 3 Adc
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation



CASE 221D–02
TO–220 TYPE

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector–Emitter Voltage		V_{CEO}	100	Vdc
Collector–Base Voltage		V_{CB}	100	Vdc
Emitter–Base Voltage		V_{EB}	5	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, T_A = 25°C)	Test No. 1 Per Fig. 14 Test No. 2 Per Fig. 15 Test No. 3 Per Fig. 16	V_{ISOL}	4500 3500 1500	V_{RMS}
Collector Current — Continuous Peak		I_C	5 8	Adc
Base Current		I_B	0.12	Adc
Total Power Dissipation* @ T_C = 25°C Derate above 25°C		P_D	30 0.24	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C		P_D	2 0.016	Watts W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	–65 to +150	I_C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	4.1	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

*Measurement made with thermocouple contacting the bottom insulated mounting surface (in a location beneath the die), the device mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.
(1) Proper strike and creepage distance must be provided.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	—	10	μAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	2	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 3 Vdc) (I_C = 3 Adc, V_{CE} = 3 Vdc)	h_{FE}	1000 2000	— —	—
Collector–Emitter Saturation Voltage (I_C = 3 Adc, I_B = 12 mAdc) (I_C = 5 Adc, I_B = 20 mAdc)	$V_{CE(sat)}$	— —	2 3.5	Vdc
Base–Emitter On Voltage (I_C = 3 Adc, V_{CE} = 3 Vdc)	$V_{BE(on)}$	—	2.5	Vdc
DYNAMIC CHARACTERISTICS				
Small–Signal Current Gain (I_C = 3 Adc, V_{CE} = 4 Vdc, f = 1 MHz)	h_{fe}	4	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJF127 MJF122	C_{ob}	— —	300 200	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

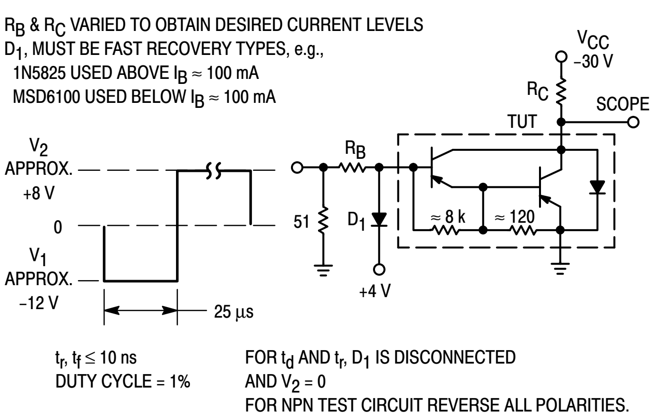

Figure 1. Switching Times Test Circuit

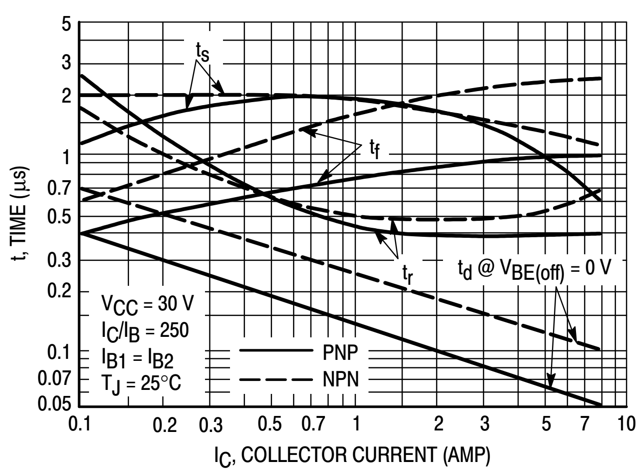

Figure 2. Typical Switching Times

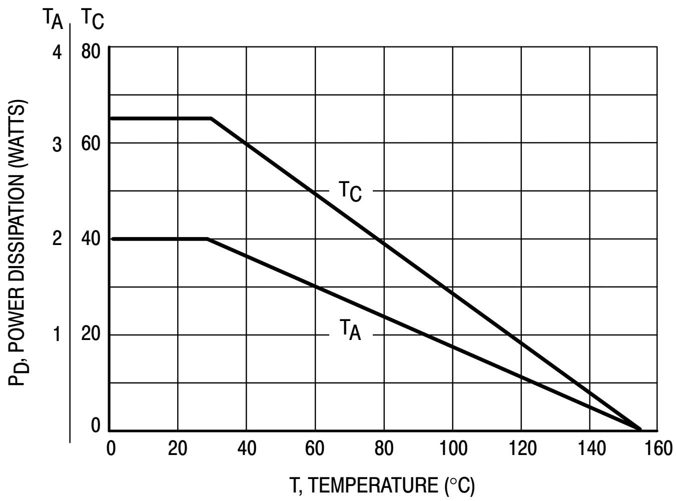

Figure 3. Maximum Power Derating

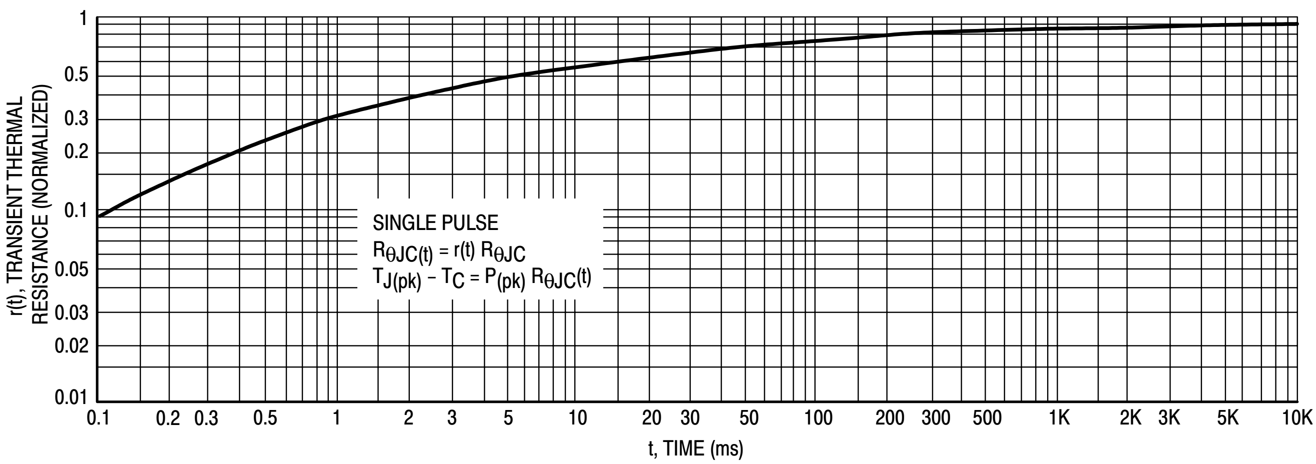

Figure 4. Thermal Response

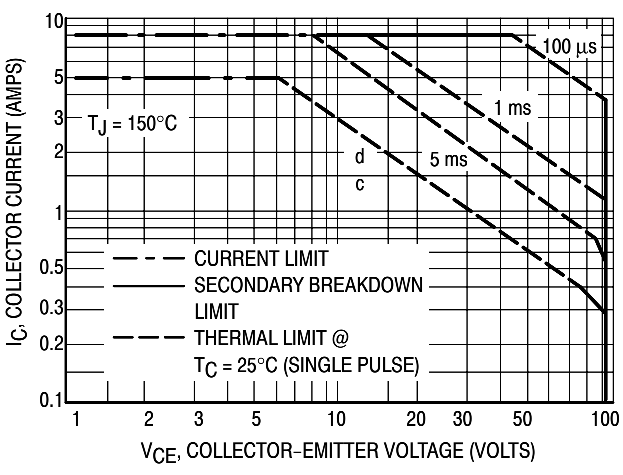

Figure 5. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

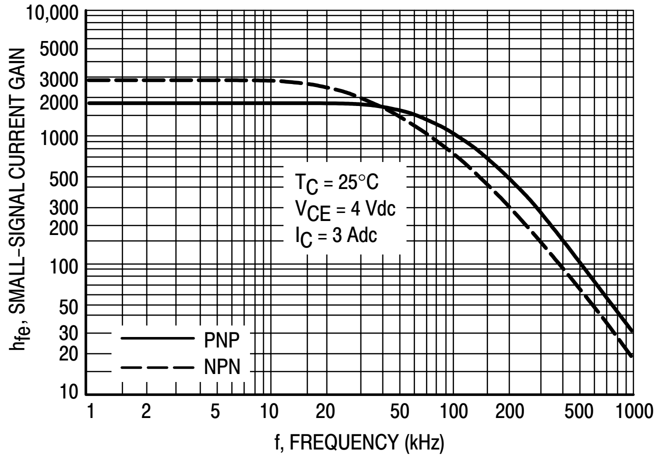

Figure 6. Typical Small–Signal Current Gain

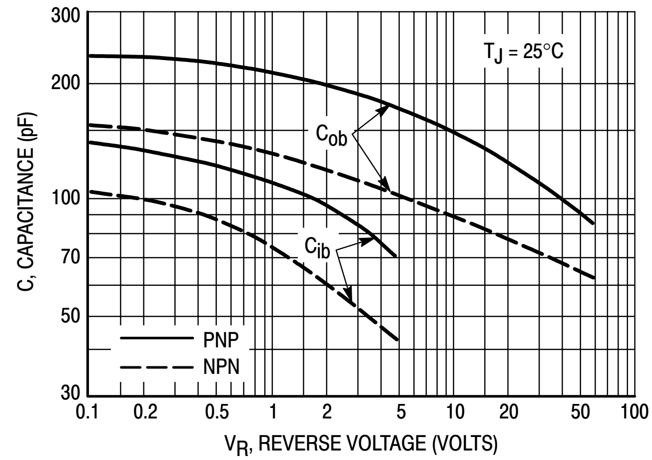

Figure 7. Typical Capacitance

NPN
MJF122

PNP
MJF127

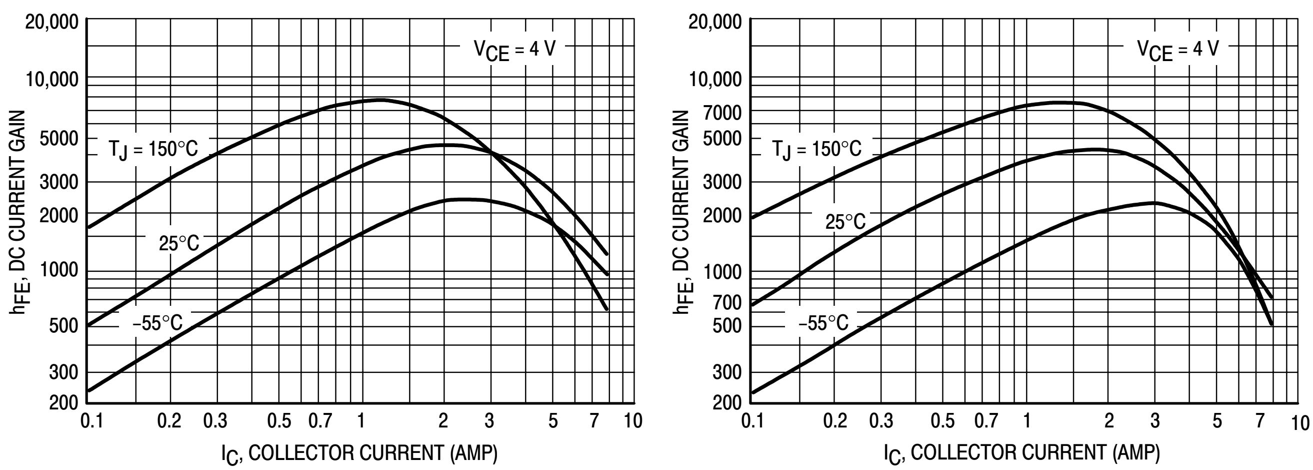

Figure 8. Typical DC Current Gain

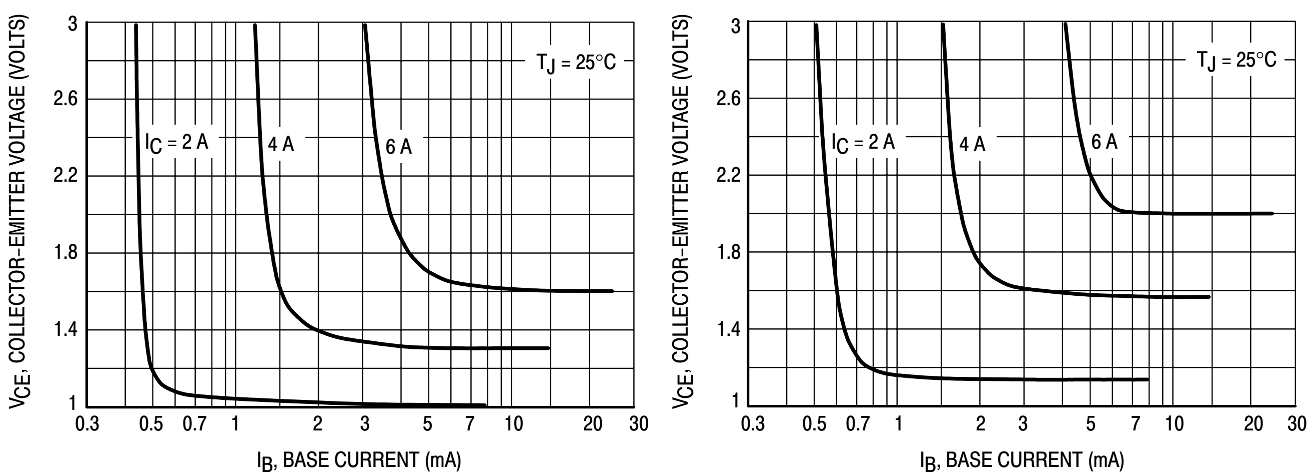

Figure 9. Typical Collector Saturation Region

NPN
MJF122

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MJF127

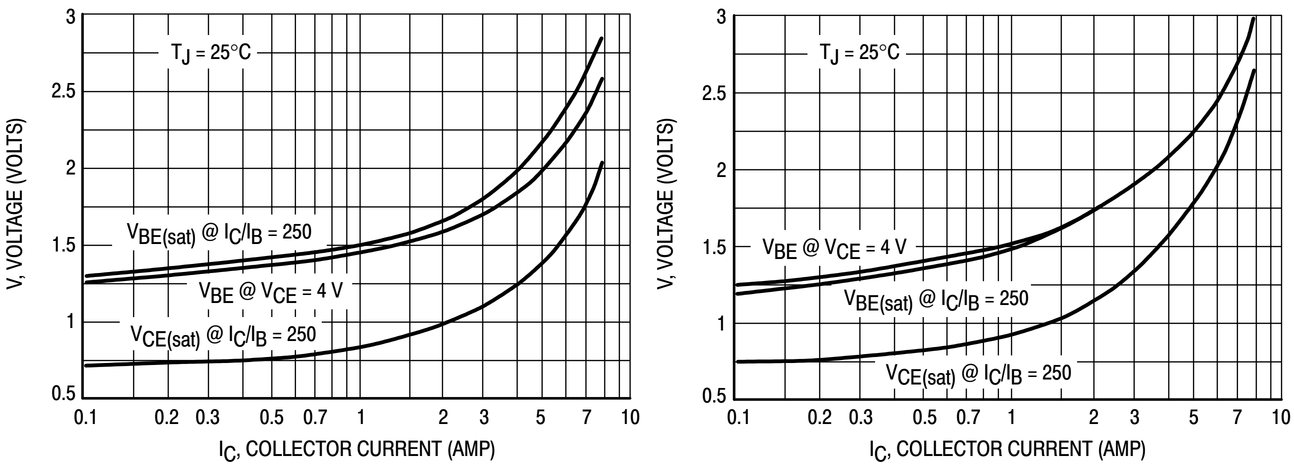


Figure 10. Typical “On” Voltages

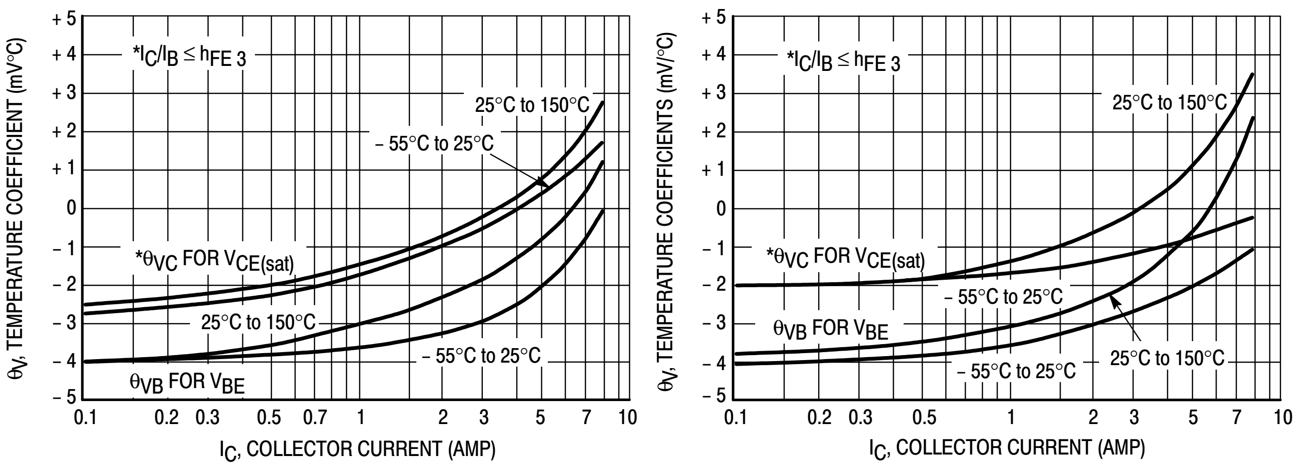


Figure 11. Typical Temperature Coefficients

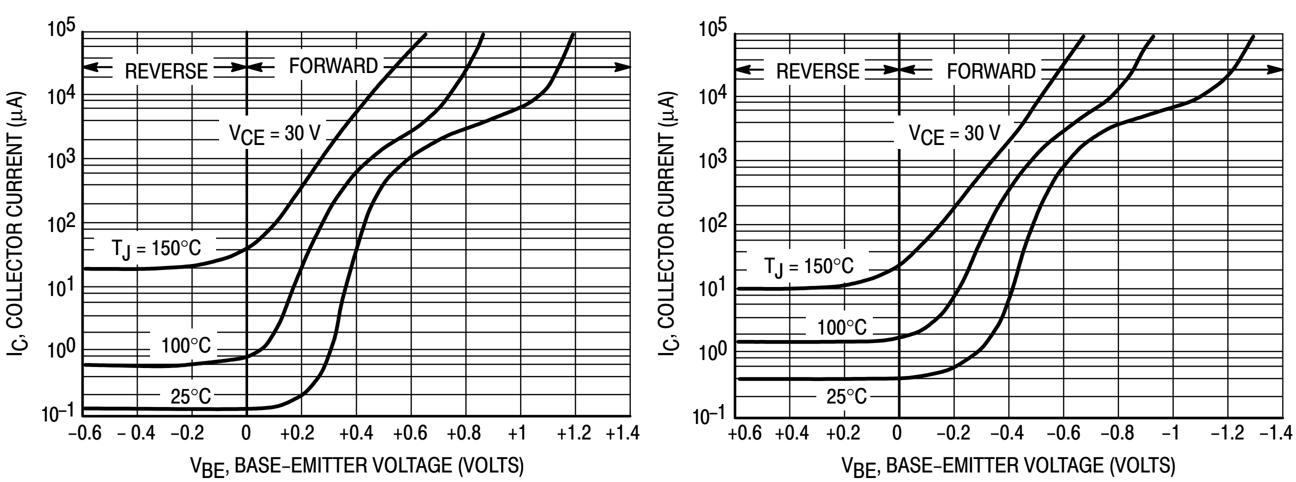


Figure 12. Typical Collector Cut–Off Region

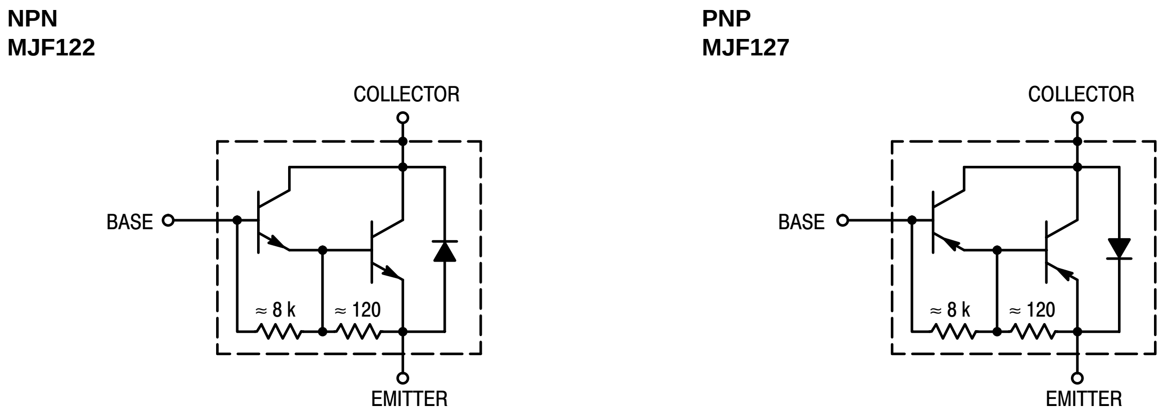


Figure 13. Darlington Schematic

TEST CONDITIONS FOR ISOLATION TESTS*

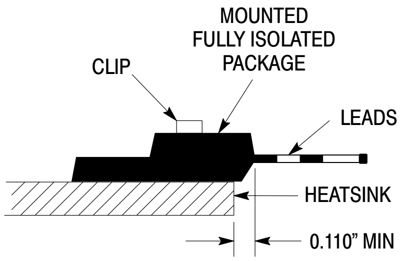


Figure 14. Clip Mounting Position for Isolation Test Number 1

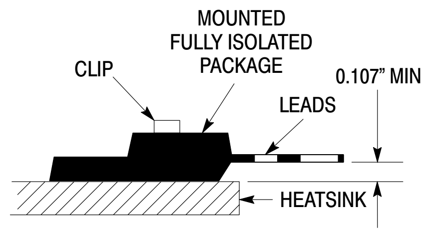


Figure 15. Clip Mounting Position for Isolation Test Number 2

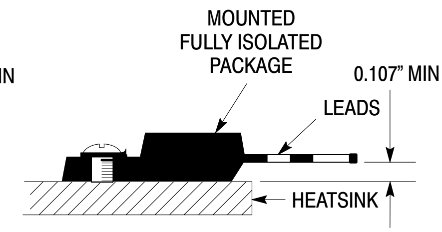


Figure 16. Screw Mounting Position for Isolation Test Number 3

*Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

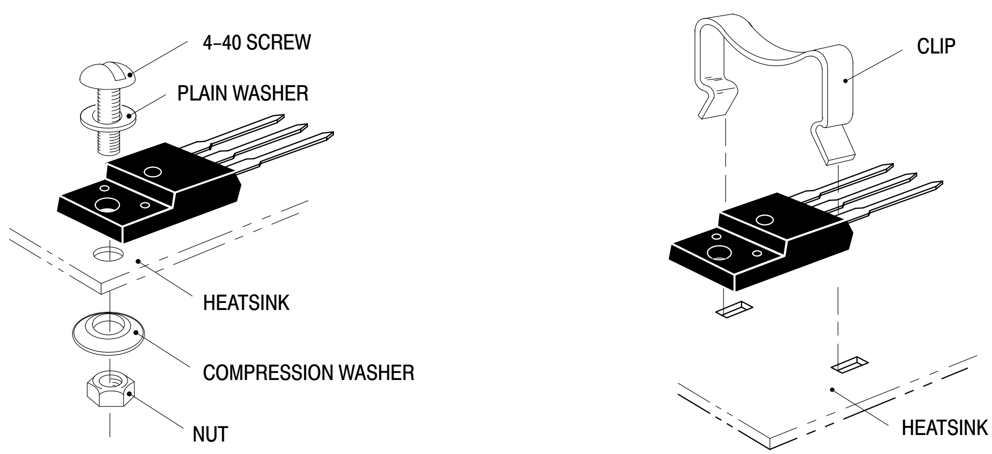


Figure 17. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

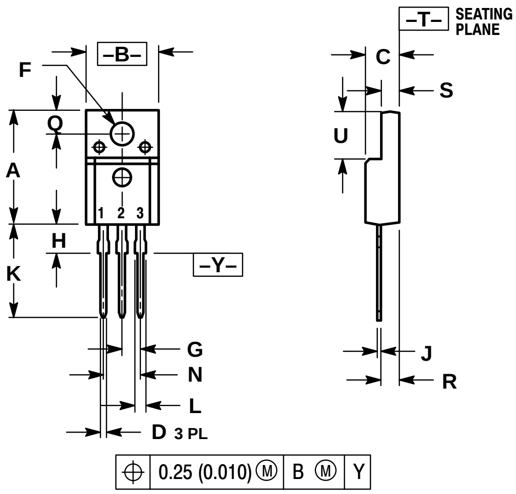
Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

PACKAGE DIMENSIONS

CASE 221D–02
TO–220 TYPE
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.621	0.629	15.78	15.97
B	0.394	0.402	10.01	10.21
C	0.181	0.189	4.60	4.80
D	0.026	0.034	0.67	0.86
F	0.121	0.129	3.08	3.27
G	0.100 BSC		2.54 BSC	
H	0.123	0.129	3.13	3.27
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
N	0.200 BSC		5.08 BSC	
Q	0.126	0.134	3.21	3.40
R	0.107	0.111	2.72	2.81
S	0.096	0.104	2.44	2.64
U	0.259	0.267	6.58	6.78

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

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