2.5 VOLT HIGH-SPEED TeraSync™ DDR/SDR FIFO 40-BIT CONFIGURATION

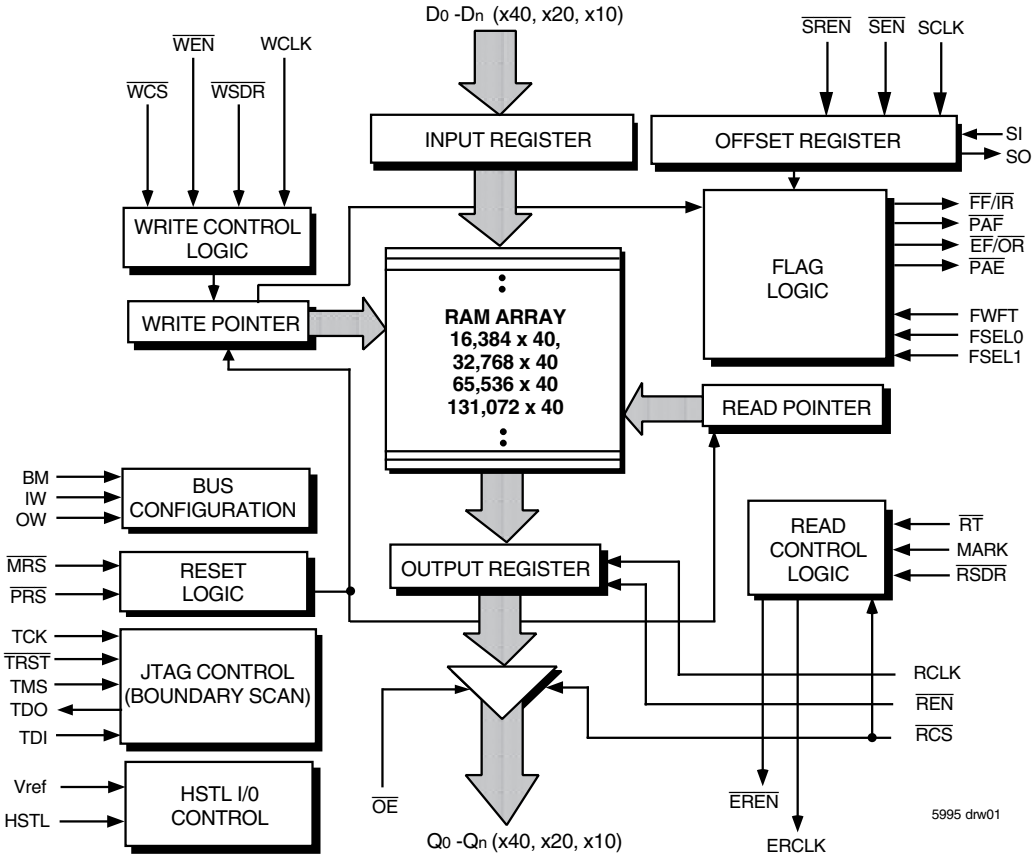
16,384 x 40, 32,768 x 40,
65,536 x 40, 131,072 x 40

IDT72T4088, IDT72T4098
IDT72T40108, IDT72T40118

FEATURES

- Choose among the following memory organizations:
  - IDT72T4088 — 16,384 x 40
  - IDT72T4098 — 32,768 x 40
  - IDT72T40108 — 65,536 x 40
  - IDT72T40118 — 131,072 x 40
- Up to 250MHz Operation of Clocks
  - 4ns read/write cycle time, 3.2ns access time
- Users selectable input port to output port data rates, 500Mb/s Data Rate
  -DDR to DDR
  -DDR to SDR
  -SDR to DDR
  -SDR to SDR
- User selectable HSTL or LVTTL I/Os
- Read Enable & Read Clock Echo outputs aid high speed operation
- 2.5V LVTTL or 1.8V, 1.5V HSTL Port Selectable Input/Ouput voltage
- 3.3V Input tolerant
- Mark & Retransmit, resets read pointer to user marked position
- Write Chip Select ($\overline{WCS}$) input enables/disables Write Operations
- Read Chip Select ($\overline{RCS}$) synchronous to RCLK
- Programmable Almost-Empty and Almost-Full flags, each flag can default to one of four preselected offsets
- Dedicated serial clock input for serial programming of flag offsets
- User selectable input and output port bus sizing
  -x40 in to x40 out
  -x40 in to x20 out
  -x40 in to x10 out
  -x20 in to x40 out
  -x10 in to x40 out
- Auto power down minimizes standby power consumption
- Master Reset clears entire FIFO
- Partial Reset clears data, but retains programmable settings
- Empty and Full flags signal FIFO status
- Select IDT Standard timing (using $\overline{EF}$ and $\overline{FF}$ flags) or First Word Fall Through timing (using $\overline{OR}$ and $\overline{IR}$ flags)
- Output enable puts data outputs into High-Impedance state
- JTAG port, provided for Boundary Scan function
- 208 Ball Grid array (PBGA), 17mm x 17mm, 1mm pitch
- Easily expandable in depth and width
- Independent Read and Write Clocks (permit reading and writing simultaneously)
- High-performance submicron CMOS technology
- Industrial temperature range (-40°C to +85°C) is available

FUNCTIONAL BLOCK DIAGRAM



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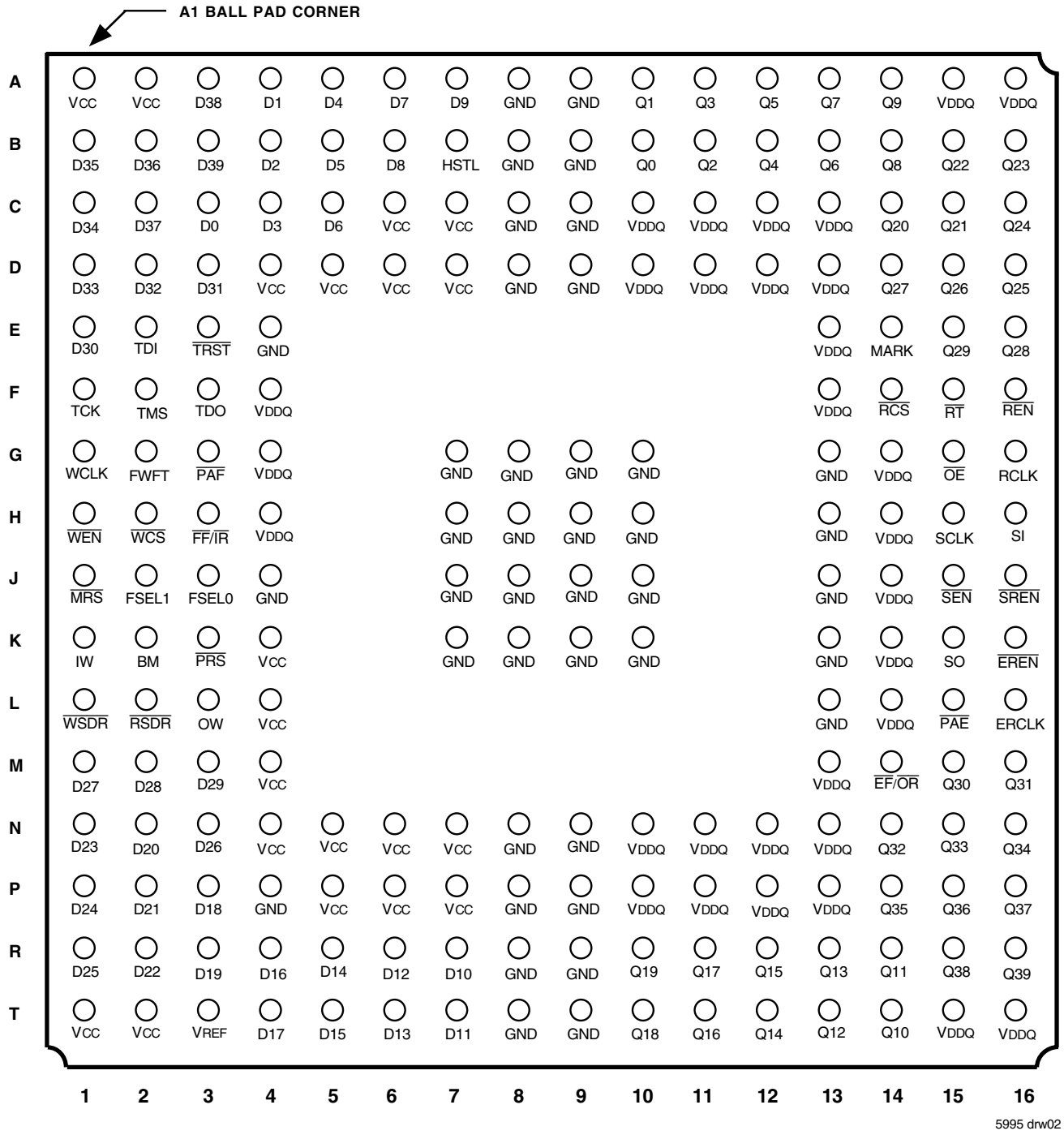
PIN CONFIGURATIONS



PBGA: 1mm pitch, 17mm x 17mm (BB208-1, order code: BB)
TOP VIEW

DESCRIPTION

The IDT72T4088/72T4098/72T40108/72T40118 are exceptionally deep, extremely high speed, CMOS First-In-First-Out (FIFO) memories with the ability to read and write data on both rising and falling edges of clock. The device has a flexible x40/x20/x10 Bus-Matching mode and the option to select single or double data rates for input and output ports. These FIFOs offer several key user benefits:

- Flexible x40/x20/x10 Bus-Matching on both read and write ports
- Ability to read and write on both rising and falling edges of a clock
- User selectable Single or Double Data Rate of input and output ports
- A user selectable MARK location for retransmit
- User selectable I/O structure for HSTL or LVTTL
- The first word data latency period, from the time the first word is written to an empty FIFO to the time it can be read, is fixed and short.
- High density offerings up to 5Mbit
- High speed operation of up to 250MHz

Bus-Matching Double Data Rate FIFOs are particularly appropriate for network, video, telecommunications, data communications and other applications that require fast data transfer on both rising and falling edges of the clock. This is a great alternative to increasing data rate without extending the width of the bus or the speed of the device. They are also effective in applications that need to buffer large amounts of data and match buses of unequal sizes.

Each FIFO has a data input port (Dn) and a data output port (Qn), both of which can assume either a 40-bit, 20-bit, or a 10-bit width as determined by the state of external control pins Input Width (IW), Output Width (OW), and Bus-Matching (BM) pin during the Master Reset cycle.

The input port is controlled by a Write Clock (WCLK) input and a Write Enable ($\overline{WEN}$) input. Data present on the Dn data inputs can be written into the FIFO on every rising and falling edge of WCLK when $\overline{WEN}$ is asserted and Write Single Data Rate ($\overline{WSDR}$) pin held HIGH. Data can be selected to write only on the rising edges of WCLK if $\overline{WSDR}$ is asserted. To guarantee functionality of the device, $\overline{WEN}$ must be a controlled signal and not tied to ground. This is important because $\overline{WEN}$ must be HIGH during the time when the Master Reset ($\overline{MRS}$) pulse is LOW. In addition, the $\overline{WSDR}$ pin must be tied HIGH or LOW. It is not a controlled signal and cannot be changed during FIFO operation.

Write operations can be selected for either Single or Double Data Rate mode. For Single Data Rate operation, writing into the FIFO requires the Write Single Data Rate ($\overline{WSDR}$) pin to be asserted. Data will be written into the FIFO on the rising edge of WCLK when the Write Enable ($\overline{WEN}$) is asserted. For Double Data Rate operations, writing into the FIFO requires $\overline{WSDR}$ to be deasserted. Data will be written into the FIFO on both rising and falling edge of WCLK when $\overline{WEN}$ is asserted.

The output port is controlled by a Read Clock (RCLK) input and a Read Enable ($\overline{REN}$) input. Data is read from the FIFO on every rising and falling edge of RCLK when $\overline{REN}$ is asserted and Read Single Data Rate ($\overline{RSDR}$) pin held HIGH. Data can be selected to read only on the rising edges of RCLK if $\overline{RSDR}$ is asserted. To guarantee functionality of the device, $\overline{REN}$ must be a controlled signal and not tied to ground. This is important because $\overline{REN}$ must be HIGH during the time when the Master Reset ($\overline{MRS}$) pulse is LOW. In addition, the $\overline{RSDR}$ pin must be tied HIGH or LOW. It is not a controlled signal and cannot be changed during FIFO operation.

Read operations can be selected for either Single or Double Data Rate mode. Similar to the write operations, reading from the FIFO in single data rate requires the Read Single Data Rate ($\overline{RSDR}$) pin to be asserted. Data will be read from the FIFO on the rising edge of RCLK when the Read Enable ($\overline{REN}$) is asserted. For Double Data Rate operations, reading into the FIFO requires $\overline{RSDR}$ to be deasserted. Data will be read out of the FIFO on both rising and falling edge of RCLK when and $\overline{REN}$ is asserted.

Both the input and output port can be selected for either 2.5V LVTTL or HSTL operation. This can be achieved by tying the HSTL signal LOW for LVTTL or HIGH for HSTL voltage operation. When the read port is setup for HSTL mode, the Read Chip Select ($\overline{RCS}$) input also has the benefit of disabling the read port inputs, providing additional power savings.

There is the option of selecting different data rates on the input and output ports of the device. There are a total of four combinations to choose from, Double Data Rate to Double Data Rate (DDR to DDR), DDR to Single Data Rate (DDR to SDR), SDR to DDR, and SDR to SDR. The rates can be set up using the $\overline{WSDR}$ and $\overline{RSDR}$ pins. For example, to set up the input to output combination of DDR to SDR, $\overline{WSDR}$ will be HIGH and $\overline{RSDR}$ will be LOW. Read and write operations are initiated on the rising edge of RCLK and WCLK respectively, never on the falling edge. If $\overline{REN}$ or $\overline{WEN}$ is asserted after a rising edge of clock, no read or write operations will be possible on the falling edge of that same pulse.

An Output Enable ($\overline{OE}$) input is provided for high-impedance control of the outputs. A read Chip Select ($\overline{RCS}$) input is also provided for synchronous enable/disable of the read port control input, $\overline{REN}$. The $\overline{RCS}$ input is synchronized to the read clock, and also provides high-impedance controls to the Qn data outputs. When $\overline{RCS}$ is disabled, $\overline{REN}$ will be disabled internally and the data outputs will be in High-Impedance. Unlike the Read Chip Select signal however, $\overline{OE}$ is not synchronous to RCLK. Outputs are high-impedanced shortly after a delay time when the $\overline{OE}$ transitions from LOW to HIGH.

The Echo Read Enable ($\overline{EREN}$) and Echo Read Clock (ERCLK) outputs are used to provide tighter synchronization between the data being transmitted from the Qn outputs and the data being received by the input device. These output signals from the read port are required for high-speed data communications. Data read from the read port is available on the output bus with respect to $\overline{EREN}$ and ERCLK, which is useful when data is being read at high-speed operations where synchronization is important.

The frequencies of both the RCLK and WCLK signals may vary from 0 to fMAX with complete independence. There are no restrictions on the frequency of one clock input with respect to another.

There are two possible timing modes of operation with these devices: IDT Standard mode and First Word Fall Through (FWFT) mode.

In IDT *Standard mode,* the first word written to an empty FIFO will not appear on the data output lines unless a specific read operation is performed. A read operation, which consists of activating $\overline{REN}$ and enabling a rising RCLK edge, will shift the word from internal memory to the data output lines. Be aware that in Double Data Rate (DDR) mode only the IDT *Standard mode* is available.

In *FWFT mode,* the first word written to an empty FIFO is clocked directly to the data output lines after three transitions of RCLK. A read operation does not have to be performed to access the first word written to the FIFO. However, subsequent words written to the FIFO do require a LOW on $\overline{REN}$ for access. The state of the FWFT input during Master Reset determines the timing mode in use.

For applications requiring more data storage capacity than a single FIFO can provide, the FWFT timing mode permits depth expansion by chaining FIFOs in series (i.e. the data outputs of one FIFO are connected to the corresponding data inputs of the next). No external logic is required.

These FIFOs have four flag pins, $\overline{EF}$/$\overline{OR}$ (Empty Flag or Output Ready), $\overline{FF}$/$\overline{IR}$ (Full Flag or Input Ready), $\overline{PAE}$ (Programmable Almost-Empty flag), and $\overline{PAF}$ (Programmable Almost-Full flag). The $\overline{EF}$ and $\overline{FF}$ functions are selected in IDT Standard mode. The $\overline{IR}$ and $\overline{OR}$ functions are selected in FWFT mode. $\overline{PAE}$ and $\overline{PAF}$ are always available for use, irrespective of timing mode.

DESCRIPTION (CONTINUED)

$\overline{PAE}$ and $\overline{PAF}$ flags can be programmed independently to switch at any point in memory. Programmable offsets mark the location within the internal memory that activates the $\overline{PAE}$ and $\overline{PAF}$ flags and can only be programmed serially. To program the offsets, set $\overline{SEN}$ active and data can be loaded via the Serial Input (SI) pin at the rising edge of SCLK. To read out the offset registers serially, set $\overline{SREN}$ active and data can be read out via the Serial Output (SO) pin at the rising edge of SCLK. Four default offset settings are also provided, so that $\overline{PAE}$ can be marked at a predefined number of locations from the empty boundary and the $\overline{PAF}$ threshold can also be marked at similar predefined values from the full boundary. The default offset values are set during Master Reset by the state of the FSEL0 and FSEL1 pins.

During Master Reset ($\overline{MRS}$), the following events occur: the read and write pointers are set to the first location of the internal FIFO memory, the FWFT pin selects IDT Standard mode or FWFT mode, the bus width configuration of the read and write port is determined by the state of IW and OW, and the default offset values for the programmable flags are set.

The Partial Reset ($\overline{PRS}$) also sets the read and write pointers to the first location of the memory. However, the timing mode and the values stored in the programmable offset registers before Partial Reset remain unchanged. The flags are updated according to the timing mode and offsets in effect. $\overline{PRS}$ is useful for resetting a device in mid-operation, when reprogramming programmable flags would be undesirable.

The timing of the $\overline{PAE}$ and $\overline{PAF}$ flags are synchronous to RCLK and WCLK, respectively. The $\overline{PAE}$ flag is asserted upon the rising edge of RCLK only and not WCLK. Similarly the $\overline{PAF}$ is asserted and updated on the rising edge of WCLK only and not RCLK.

This device includes a Retransmit from Mark feature that utilizes two control inputs, MARK and $\overline{RT}$ (Retransmit). If the MARK input is enabled with respect to the RCLK, the memory location being read at the point will be marked. Any subsequent retransmit operation (when $\overline{RT}$ goes LOW), will reset the read pointer to this "marked" location.

The device can be configured with different input and output bus widths as previously stated. These rates are: x40 to x40, x40 to x20,x40 to x10, x20 to x40, and x10 to x40.

If, at any time, the FIFO is not actively performing an operation, the chip will automatically power down. Once in the power down state, the standby supply current consumption is minimized. Initiating any operation (by activating control inputs) will immediately take the device out of the power down state.

A JTAG test port is provided, here the FIFO has fully functional boundary Scan feature, compliant with IEEE 1449.1 Standard Test Access Port and Boundary Scan Architecture.

The Double Data Rate FIFO has the capability of operating in either LVTTL or HSTL mode. HSTL mode can be selected by enabling the HSTL pin. Both input and output ports will operate in either HSTL or LVTTL mode, but cannot be selected independent of one another.

The IDT72T4088/72T4098/72T40108/72T40118 are fabricated using IDT's high-speed submicron CMOS technology.

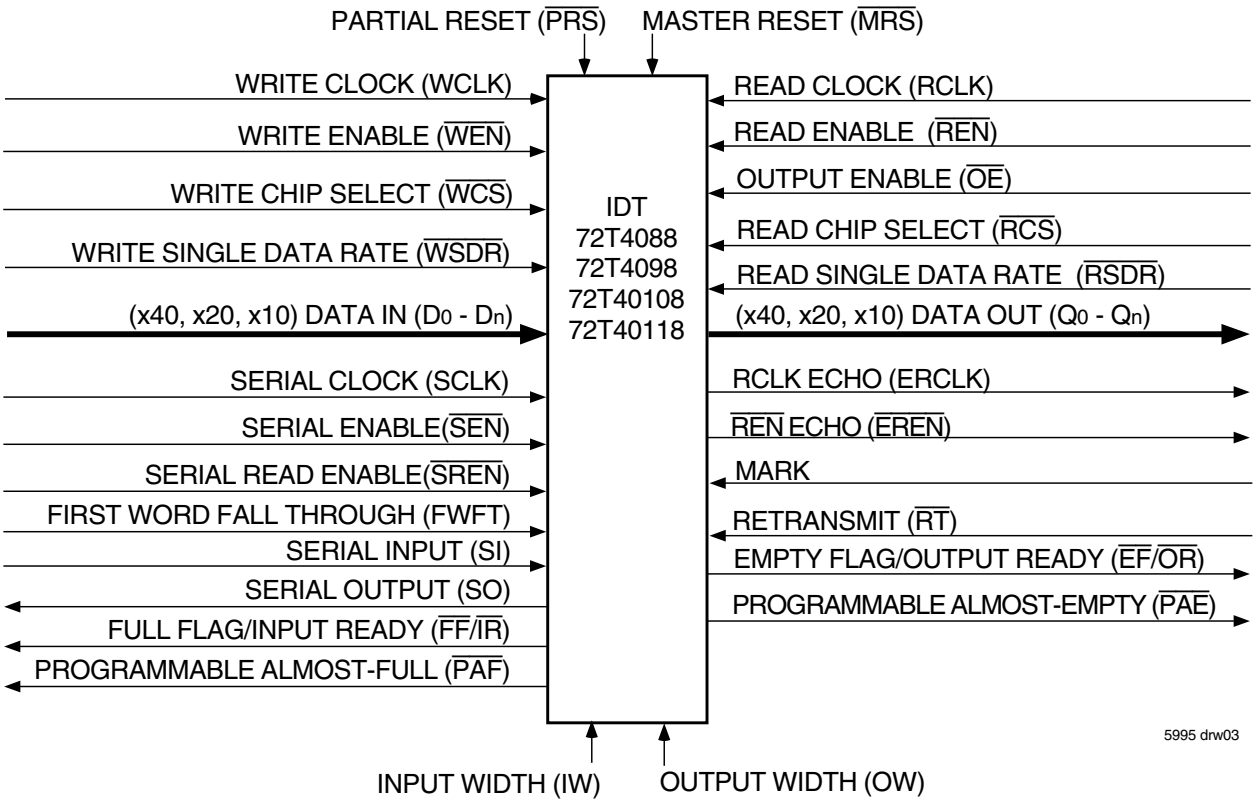


Figure 1. Single Device Configuration Signal Flow Diagram

TABLE 1 — BUS-MATCHING CONFIGURATION MODES

BM	IW	OW	Write Port Width	Read Port Width
L	L	L	x40	x40
H	L	L	x40	x20
H	L	H	x40	x10
H	H	L	x20	x40
H	H	H	x10	x40

NOTE:
1. Pin status during Master Reset.

TABLE 2 — DATA RATE-MATCHING CONFIGURATION MODES

WSDR	RSDR	Write Port Width	Read Port Width
H	H	Double Data Rate	Double Data Rate
H	L	Double Data Rate	Single Data Rate
L	H	Single Data Rate	Double Data Rate
L	L	Single Data Rate	Single Data Rate

NOTE:
1. Pin status during Master Reset.
2. Data Rate Matching can be used in conjunction with Bus-Matching modes.

PIN DESCRIPTION

Symbol & Pin No.	Name	I/O TYPE	Description
BM[1] (K2)	Bus-Matching	LVTTL INPUT	During Master Reset, this pin along with IW and OW selects the bus sizes for both write and read ports.
D_0-D_{39} (See Pin No. table for details)	Data Inputs	HSTL-LVTTL INPUT	Data inputs for a 40-, 20-, or 10-bit bus. When in 20- or 10- bit mode, the unused input pins are in a don't care state. The data bus is sampled on both rising and falling edges of WCLK when $\overline{WEN}$ is enabled and DDR Mode is enabled or on the rising edges of WCLK only in SDR Mode.
$\overline{EF}/\overline{OR}$ (M14)	Empty Flag/ Output Ready	HSTL-LVTTL OUTPUT	In the IDT Standard mode, the $\overline{EF}$ function is selected. $\overline{EF}$ indicates whether or not the FIFO memory is empty. In FWFT mode, the $\overline{OR}$ function is selected. $\overline{OR}$ indicates whether or not there is valid data available at the outputs.
ERCLK (L16)	Echo Read Clock	HSTL-LVTTL OUTPUT	Read Clock Echo output, must be equal to or faster than the Qn data outputs.
$\overline{EREN}$ (K16)	Echo Read Enable	HSTL-LVTTL OUTPUT	Read Enable Echo output, used in conjunction with ERCLK.
$\overline{FF}/\overline{IR}$ (H3)	Full Flag/ Input Ready	HSTL-LVTTL OUTPUT	In the IDT Standard mode, the $\overline{FF}$ function is selected. $\overline{FF}$ indicates whether or not the FIFO memory is empty. In FWFT mode, the $\overline{IR}$ function is selected. $\overline{IR}$ indicates whether or not there is space available for writing to the FIFO memory.
FSEL0[1] (J3)	Flag Select Bit 0	LVTTL INPUT	During Master Reset, this input along with FSEL1 will select the default offset values for the programmable flags $\overline{PAE}$ and $\overline{PAF}$. There are four possible settings available.
FSEL1[1] (J2)	Flag Select Bit 1	LVTTL INPUT	During Master Reset, this input along with FSEL0 will select the default offset values for the programmable flags $\overline{PAE}$ and $\overline{PAF}$. There are four possible settings available.
FWFT (G2)	First Word Fall Through	LVTTL INPUT	During Master reset, selects First Word Fall Through or IDT Standard mode. FWFT is not available in DDR mode. In SDR mode, the first word will always fall through on the rising edge.
HSTL[1] (B7)	HSTL Select	LVTTL INPUT	This input pin is used to select HSTL or 2.5V LVTTL device operation. If HSTL inputs are required, this input must be tied HIGH, otherwise it must be tied LOW and cannot toggle during operation.
IW[1] (K1)	Input Width	LVTTL INPUT	During Master Reset, this pin along with OW and BM, selects the bus width of the read and write port.
MARK (E14)	Mark Read Pointer for Retransmit	HSTL-LVTTL INPUT	When this pin is asserted the current location of the read pointer will be marked. Any subsequent Retransmit operation will reset the read pointer to this position. There is an unlimited number to times to set the mark location, but only the most recent location marked will be acknowledged.
$\overline{MRS}$ (J1)	Master Reset	HSTL-LVTTL INPUT	$\overline{MRS}$ initializes the read and write pointers to zero and sets the output registers to all zeros. During Master Reset, the FIFO is configured for either FWFT or IDT Standard mode, Bus-Matching configurations, and programmable flag default settings.
$\overline{OE}$ (G15)	Output Enable	HSTL-LVTTL INPUT	When HIGH, data outputs Q_0-Q_{39} are in high impedance. When LOW, the data outputs Q_0-Q_{39} are enabled. No other outputs are affected by $\overline{OE}$.
OW[1] (L3)	Output Width	LVTTL INPUT	During Master Reset, this pin along with IW and BM, selects the bus width of the read and write port.
$\overline{PAE}$ (L15)	Programmable Almost-Empty Flag	HSTL-LVTTL OUTPUT	$\overline{PAE}$ goes HIGH if the number of words in the FIFO memory is greater than or equal to offset n, which is stored in the Empty Offset register. $\overline{PAE}$ goes LOW if the number of words in the FIFO memory is less than offset n.
$\overline{PAF}$ (G3)	Programmable Almost-Full Flag	HSTL-LVTTL OUTPUT	$\overline{PAF}$ goes HIGH if the number of free locations in the FIFO memory is more than offset m, which is stored in the Full Offset register. $\overline{PAF}$ goes LOW if the number of free locations in the FIFO memory is less than or equal to m.
$\overline{PRS}$ (K3)	Partial Reset	HSTL-LVTTL INPUT	$\overline{PRS}$ initializes the read and write pointers to zero and sets the output registers to all zeros. During Partial Reset, the existing mode (IDT standard or FWFT) and programmable flag settings are not affected.
Q_0-Q_{39} (See Pin No. table for details)	Data Outputs	HSTL-LVTTL OUTPUT	Data outputs for a 40-, 20-, or 10-bit bus. When in 20- or 10- bit mode, the unused output pins should not be connected. The output data is clocked on both rising and falling edges of RCLK when $\overline{REN}$ is enabled and DDR Mode is enabled or on the rising edges of RCLK only in SDR Mode.
RCLK (G16)	Read Clock	HSTL-LVTTL INPUT	Input clock when used in conjunction with $\overline{REN}$ for reading data from the FIFO memory and output register.

PIN DESCRIPTION (CONTINUED)

Symbol & Pin No.	Name	I/O TYPE	Description
$\overline{RCS}$ (F14)	Read Chip Select	HSTL-LVTTL INPUT	$\overline{RCS}$ provides synchronous enable/disable control of the read port and High-Impedance control of the Qn data outputs, synchronous to RCLK. When using $\overline{RCS}$ the $\overline{OE}$ pin must be tied LOW. During Master or Partial Reset the $\overline{RCS}$ input is don't care, if $\overline{OE}$ is LOW the data outputs will be Low-Impedance regardless of $\overline{RCS}$.
$\overline{REN}$ (F16)	Read Enable	HSTL-LVTTL INPUT	When LOW and in DDR mode, $\overline{REN}$ along with a rising and falling edge of RCLK will send data in FIFO memory to the output register and read the current data in output register. In SDR mode data will only be read on the rising edge of RCLK only.
$\overline{RSDR}$(1) (L2)	Read Single Data Rate	LVTTL INPUT	When LOW, this input pin sets the read port to Single Data Clock mode. When HIGH, the read port will operate in Double Data Clock mode. This pin must be tied either HIGH or LOW and cannot toggle during operation.
$\overline{RT}$ (F15)	Retransmit	HSTL-LVTTL INPUT	$\overline{RT}$ asserted on the rising edge of RCLK initializes the read pointer to the first location in memory. $\overline{EF}$ flag is set to LOW ($\overline{OR}$ to HIGH in FWFT mode). The write pointer, offset registers, and flag settings are not affected. If a mark has been set via the MARK input pin, then the read pointer will initialize to the mark location when $\overline{RT}$ is asserted.
SCLK (H15)	Serial Clock	LVTTL INPUT	A rising edge of SCLK will clock the serial data present on the SI input into the offset registers provided that $\overline{SEN}$ is enabled. A rising edge of SCLK will also read data out of the offset registers provided that $\overline{SREN}$ is enabled.
$\overline{SEN}$ (J15)	Serial Input Enable	HSTL-LVTTL INPUT	$\overline{SEN}$ used in conjunction with SI and SCLK enables serial loading of the programmable flag offsets.
$\overline{SREN}$ (J16)	Serial Read Enable	HSTL-LVTTL INPUT	$\overline{SREN}$ used in conjunction with SO and SCLK enables serial reading of the programmable flag offsets.
SI (H16)	Serial Input	HSTL-LVTTL INPUT	This input pin is used to load serial data into the programmable flag offsets. Used in conjunction with $\overline{SEN}$ and SCLK.
SO (K15)	Serial Output	HSTL-LVTTL OUTPUT	This output pin is used to read data from the programmable flag offsets. Used in conjunction with $\overline{SREN}$ and SCLK.
TCK(2) (F1)	JTAG Clock	HSTL-LVTTL INPUT	Clock input for JTAG function. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data from TMS and TDI are sampled on the rising edge of TCK and outputs change on the falling edge of TCK. If the JTAG function is not used this signal needs to be tied to GND.
TDI(2) (E2)	JTAG Test Data Input	HSTL-LVTTL INPUT	One of four terminals required by IEEE Standard 1149.1-1990. During the JTAG boundary scan operation, test data serially loaded via the TDI on the rising edge of TCK to either the Instruction Register, ID Register and Bypass Register. An internal pull-up resistor forces TDI HIGH if left unconnected.
TDO(2) (F3)	JTAG Test Data Output	HSTL-LVTTL OUTPUT	One of four terminals required by IEEE Standard 1149.1-1990. During the JTAG boundary scan operation, test data serially loaded output via the TDO on the falling edge of TCK from either the Instruction Register, ID Register and Bypass Register. This output is high impedance except when shifting, while in SHIFT-DR and SHIFT-IR controller states.
TMS(2) (F2)	JTAG Mode Select	HSTL-LVTTL INPUT	TMS is a serial input pin. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the the device through its TAP controller states. An internal pull-up resistor forces TMS HIGH if left unconnected.
$\overline{TRST}$(2) (E3)	JTAG Reset	HSTL-LVTTL INPUT	$\overline{TRST}$ is an asynchronous reset pin for the JTAG controller. The JTAG TAP controller does not automatically reset upon power-up, thus it must be reset by either this signal or by setting TMS= HIGH for five TCK cycles. If the TAP controller is not properly reset then the FIFO outputs will always be in high-impedance. If the JTAG function is used but the user does not want to use $\overline{TRST}$, then $\overline{TRST}$ can be tied with $\overline{MRS}$ to ensure proper FIFO operation. If the JTAG function is not used then this signal needs to be tied to GND. An internal pull-up resistor forces $\overline{TRST}$ HIGH if left unconnected.
WCLK (G1)	Write Clock	HSTL-LVTTL INPUT	Input clock when used in conjunction with $\overline{WEN}$ for writing data into the FIFO memory.
$\overline{WCS}$ (H2)	Write Chip Select	HSTL-LVTTL INPUT	The $\overline{WCS}$ pin can be regarded as a second $\overline{WEN}$ input, enabling/disabling write operations.
$\overline{WEN}$ (H1)	Write Enable	HSTL-LVTTL INPUT	When LOW and in DDR mode, $\overline{WEN}$ along with a rising and falling edge of WCLK will write data into the FIFO memory. In SDR mode data will only be read on the rising edge of RCLK only.

PIN DESCRIPTION (CONTINUED)

Symbol & Pin No.	Name	I/O TYPE	Description
$\overline{WSDR}$[1] (L1)	Write Single Data Rate	LVTTL INPUT	When LOW, this input pin sets the write port to Single Data Clock mode. When HIGH, the write port will operate in Double Data Clock mode. This pin must be tied either HIGH or LOW and cannot toggle during operation.
V_{CC} (See below)	+2.5V Supply	INPUT	There are Vcc supply inputs and must be connected to the 2.5V supply rail.
V_{DDQ} (See below)	O/P Rail Voltage	INPUT	This pin should be tied to the desired voltage rail for providing power to the output drivers. Nominally 1.5V or 1.8V for HSTL, 2.5V for LVTTL.
GND (See below)	Core Ground Pin	INPUT	These are Ground pins are for the core device and must be connected to the GND rail.
Vref (T3)	Reference Voltage	INPUT	This is a Voltage Reference input and must be connected to a voltage level determined in the Recommended DC Operating Conditions section. This provides the reference voltage when using HSTL class inputs. If HSTL class inputs are not being used, this pin must be connected to GND.

NOTES:
1. Inputs should not change state after Master Reset.
2. These pins are for the JTAG port. Please refer to pages 25-28 and Figures 5-7.

PIN NUMBER TABLE

Symbol	Name	I/O TYPE	Pin Number
D_{0-39}	Data Inputs	HSTL-LVTTL INPUT	D0-C3, D1-A4, D2-B4, D3-C4, D4-A5, D5-B5, D6-C5, D7-A6, D8-B6, D9-A7, D10-R7, D11-T7, D12-R6, D13-T6, D14-R5, D15-T5, D16-R4, D17-T4, D18-P3, D19-R3, D20-N2, D21-P2, D22-R2, D23-N1, D24-P1, D25-R1, D26-N3, D(27-29)-M(1-3), D30-E1, D(31-33)-D(3-1), D34-C1, D(35,36)-B(1,2), D37-C2, D38-A3, D39-B3
Q_{0-39}	Data Outputs	HSTL-LVTTL OUTPUT	Q0-B10, Q1-A10, Q2-B11, Q3-A11, Q4-B12, Q5-A12, Q6-B13, Q7-A13, Q8-B14, Q9-A14, Q10-T14 Q11-R14, Q12-T13, Q13-R13, Q14-T12, Q15-R12, Q16-T11, Q17-R11, Q18-T10, Q19-R10, Q(20,21)-C(14,15), Q(22,23)-B(15,16), Q24-C16, Q(25-27)-D(16-14), Q(28,29)-E(16,15), Q(30,31)-M(15,16), Q(32-34)- N(14-16), Q(35-37)-P(14-16), Q(38,39)-R(15,16)
V_{CC}	+2.5V Supply	INPUT	A(1,2), C(6,7), D(4-7), K4, L4, M4, N(4-7), P(5-7), T(1,2)
V_{DDQ}	O/P Rail Voltage	INPUT	A(15,16), C(10-13), D(10-13), E13, F(4,13), G(4,14), H(4,14), J14, K14, L14, M13, N(10-13), P(10-13), T(15,16)
GND	Ground Pin	INPUT	A(8,9), B(8,9), C(8,9), D(8,9), E4, G(7-10,13), H(7-10,13), J(4,7-10,13), K(7-10,13), L13, N(8,9), P(4,8,9), R(8,9), T(8,9)

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5 to +3.6[2]	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Compliant with JEDEC JESD8-5. V_{CC} terminal only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}[2,3]	Input Capacitance	V_{IN} = 0V	10[3]	pF
C_{OUT}[1,2]	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES:

1. With output deselected, ($\overline{OE} \geq V_{IH}$).
2. Characterized values, not currently tested.
3. C_{IN} for Vref is 20pF.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		2.375	2.5	2.625	V
GND	Supply Voltage		0	0	0	V
V_{IH}	Input High Voltage	— LVTTL	1.7	—	3.45	V
		— eHSTL	V_{REF}+0.2	—	—	V
		— HSTL	V_{REF}+0.2	—	—	V
V_{IL}	Input Low Voltage	— LVTTL	-0.3	—	0.7	V
		— eHSTL	—	—	V_{REF}-0.2	V
		— HSTL	—	—	V_{REF}-0.2	V
V_{REF} (HSTL only)	Voltage Reference Input	— eHSTL	0.8	0.9	1.0	V
		— HSTL	0.68	0.75	0.9	V
T_A	Operating Temperature Commercial		0	—	70	°C
T_A	Operating Temperature Industrial		-40	—	85	°C

NOTE:

1. V_{REF} is only required for HSTL or eHSTL inputs. V_{REF} should be tied LOW for LVTTL operation.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 2.5V ± 0.125V, T_A = 0°C to +70°C;Industrial: V_{CC} = 2.5V ± 0.125V, T_A = -40°C to +85°C)

Symbol	Parameter		Min.	Max.	Unit
I_{LI}	Input Leakage Current		–10	10	µA
I_{LO}	Output Leakage Current		–10	10	µA
V_{OH}[5]	Output Logic "1" Voltage,	I_{OH} = –8 mA @V_{DDQ} = 2.5V ± 0.125V (LVTTL)	V_{DDQ}-0.4	—	V
		I_{OH} = –8 mA @V_{DDQ} = 1.8V ± 0.1V (eHSTL)	V_{DDQ}-0.4	—	V
		I_{OH} = –8 mA @V_{DDQ} = 1.5V ± 0.1V (HSTL)	V_{DDQ}-0.4	—	V
V_{OL}	Output Logic "0" Voltage,	I_{OL} = 8 mA @V_{DDQ} = 2.5V ± 0.125V (LVTTL)	—	0.4V	V
		I_{OL} = 8 mA @V_{DDQ} = 1.8V ± 0.1V (eHSTL)	—	0.4V	V
		I_{OL} = 8 mA @V_{DDQ} = 1.5V ± 0.1V (HSTL)	—	0.4V	V
I_{CC1}[1,2]	Active V_{CC} Current (V_{CC} = 2.5V)	I/O = LVTTL	—	20	mA
		I/O = HSTL	—	60	mA
		I/O = eHSTL	—	60	mA
I_{CC2}[1]	Standby V_{CC} Current (V_{CC} = 2.5V)	I/O = LVTTL	—	10	mA
		I/O = HSTL	—	50	mA
		I/O = eHSTL	—	50	mA

NOTES:

1. Both WCLK and RCLK toggling at 20MHz. Data inputs toggling at 10MHz. $\overline{WCS}$ = HIGH, $\overline{REN}$ or $\overline{RCS}$ = HIGH.
2. Typical I_{CC1} calculation: for LVTTL I/O I_{CC1} (mA) = 0.6mA x fs, fs = WCLK frequency = RCLK frequency (in MHz)
   for HSTL or eHSTL I/O I_{CC1} (mA) = 38mA + (0.7mA x fs), fs = WCLK frequency = RCLK frequency (in MHz)
3. Typical I_{DDQ} calculation: With Data Outputs in High-Impedance: I_{DDQ} (mA) = 0.15mA x fs
   With Data Outputs in Low-Impedance: I_{DDQ} (mA) = (C_L x V_{DDQ} x fs x 2N)/2000
   fs = WCLK frequency = RCLK frequency (in MHz), V_{DDQ} = 2.5V for LVTTL; 1.5V for HSTL; 1.8V for eHSTL, N = Number of outputs switching.
   t_A = 25°C, C_L = capacitive load (pf)
4. Total Power consumed: PT = [(V_{CC} x I_{CC}) + (V_{DDQ} x I_{DDQ})].
5. Outputs are not 3.3V tolerant.

AC ELECTRICAL CHARACTERISTICS[1]

(Commercial: V_{CC} = 2.5V ± 5%, T_A = 0°C to +70°C;Industrial: V_{CC} = 2.5V ± 5%, T_A = -40°C to +85°C)

		Commercial		Commercial		Com'l & Ind'l[2]		Commercial		
		IDT72T4088L4 IDT72T4098L4 IDT72T40108L4 IDT72T40118L4		IDT72T4088L5 IDT72T4098L5 IDT72T40108L5 IDT72T40118L5		IDT72T4088L6-7 IDT72T4098L6-7 IDT72T40108L6-7 IDT72T40118L6-7		IDT72T4088L10 IDT72T4098L10 IDT72T40108L10 IDT72T40118L10		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_{S1}	Clock Cycle Frequency SDR	—	250	—	200	—	150	—	100	MHz
f_{S2}	Clock Cycle Frequency DDR	—	150	—	150	—	150	—	100	MHz
t_A	Data Access Time	0.6	3.2	0.6	3.6	0.6	3.8	0.6	4.5	ns
t_{ASO}	Data Access Serial Output Time	0.6	3.2	0.6	3.6	0.6	3.8	0.6	4.5	ns
t_{CLK1}	Clock Cycle Time SDR	4	—	5	—	6.7	—	10	—	ns
t_{CLK2}	Clock Cycle Time DDR	6.7	—	6.7	—	6.7	—	10	—	ns
t_{CLKH1}	Clock High Time SDR	1.8	—	2.3	—	2.8	—	4.5	—	ns
t_{CLKH2}	Clock High Time DDR	2.8	—	2.8	—	2.8	—	4.5	—	ns
t_{CLKL1}	Clock Low Time SDR	1.8	—	2.3	—	2.8	—	4.5	—	ns
t_{CLKL2}	Clock Low Time DDR	2.8	—	2.8	—	2.8	—	4.5	—	ns
t_{DS}	Data Setup Time	1.2	—	1.5	—	2.0	—	3.0	—	ns
t_{DH}	Data Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{ENS}	Enable Setup Time	1.2	—	1.5	—	2.0	—	3.0	—	ns
t_{ENH}	Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{WCSS}	$\overline{WCS}$ setup time	1.2	—	1.5	—	2.0	—	3.0	—	ns
t_{WCSH}	$\overline{WCS}$ hold time	0.5	—	0.5	—	0.5	—	0.5	—	ns
f_C	Clock Cycle Frequency (SCLK)	—	10	—	10	—	10	—	10	MHz
t_{SCLK}	Serial Clock Cycle	100	—	100	—	100	—	100	—	ns
t_{SCKH}	Serial Clock High	45	—	45	—	45	—	45	—	ns
t_{SCKL}	Serial Clock Low	45	—	45	—	45	—	45	—	ns
t_{SDS}	Serial Data In Setup	15	—	15	—	15	—	15	—	ns
t_{SDH}	Serial Data In Hold	5	—	5	—	5	—	5	—	ns
t_{SENS}	Serial Enable Setup	5	—	5	—	5	—	5	—	ns
t_{SENH}	Serial Enable Hold	5	—	5	—	5	—	5	—	ns
t_{RS}	Reset Pulse Width[3]	30	—	30	—	30	—	30	—	ns
t_{RSS}	Reset Setup Time	15	—	15	—	15	—	15	—	ns
t_{HRSS}	HSTL Reset Setup Time	4	—	4	—	4	—	4	—	µs
t_{RSR}	Reset Recovery Time	10	—	10	—	10	—	10	—	ns
t_{RSF}	Reset to Flag and Output Time	—	10	—	12	—	15	—	15	ns
t_{OLZ}	Output Enable to Output in Low Z[4]	0	—	0	—	0	—	0	—	ns
t_{OE}	Output Enable to Output Valid	—	3.2	—	3.6	—	3.8	—	4.5	ns
t_{OHZ}	Output Enable to Output in High Z[4]	—	3.2	—	3.6	—	3.8	—	4.5	ns
t_{WFF}	Write Clock to $\overline{FF}$ or $\overline{IR}$	—	3.2	—	3.6	—	3.8	—	4.5	ns
t_{REF}	Read Clock to $\overline{EF}$ or $\overline{OR}$	—	3.2	—	3.6	—	3.8	—	4.5	ns
t_{PAFS}	Write Clock to Programmable Almost-Full Flag	—	3.2	—	3.6	—	3.8	—	4.5	ns
t_{PAES}	Read Clock to Programmable Almost-Empty Flag	—	3.2	—	3.6	—	3.8	—	4.5	ns
t_{ERCLK}	RCLK to Echo RCLK output	—	3.6	—	4	—	4.3	—	5	ns
t_{CLKEN}	RCLK to Echo $\overline{REN}$ output	—	3.2	—	3.6	—	3.8	—	4.5	ns
t_{RCSLZ}	RCLK to Active from High-Z	—	3.2	—	3.6	—	3.8	—	4.5	ns
t_{RCSHZ}	RCLK to High-Z[4]	—	3.2	—	3.6	—	3.8	—	4.5	ns
t_{SKEW1}	Skew time between RCLK and WCLK for $\overline{EF}$/$\overline{OR}$ and $\overline{FF}$/$\overline{IR}$	3.5	—	4	—	5	—	7	—	ns
t_{SKEW2}	Skew time between RCLK & WCLK for $\overline{EF}$/$\overline{OR}$ & $\overline{FF}$/$\overline{IR}$ in DDR mode	3.5	—	4	—	5	—	7	—	ns
t_{SKEW3}	Skew time between RCLK and WCLK for $\overline{PAE}$ and $\overline{PAF}$	4	—	5	—	6	—	8	—	ns

NOTES:
1. All AC timings apply to both IDT Standard mode and First Word Fall Through mode.
2. Industrial temperature range product for the 6-7ns speed grade is available as a standard device. All other speed grades are available by special order.
3. Pulse widths less than minimum values are not allowed.
4. Values guaranteed by design, not currently tested.

HSTL
1.5V AC TEST CONDITIONS

Input Pulse Levels	0.25 to 1.25V
Input Rise/Fall Times	0.4ns
Input Timing Reference Levels	0.75
Output Reference Levels	$V_{DDQ}/2$

NOTE:
1. V_{DDQ} = 1.5V±.

AC TEST LOADS

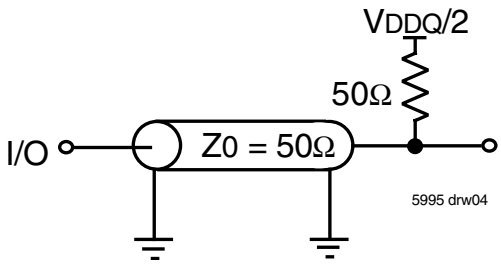


Figure 2a. AC Test Load

EXTENDED HSTL
1.8V AC TEST CONDITIONS

Input Pulse Levels	0.4 to 1.4V
Input Rise/Fall Times	0.4ns
Input Timing Reference Levels	0.9
Output Reference Levels	$V_{DDQ}/2$

NOTE:
1. V_{DDQ} = 1.8V±.

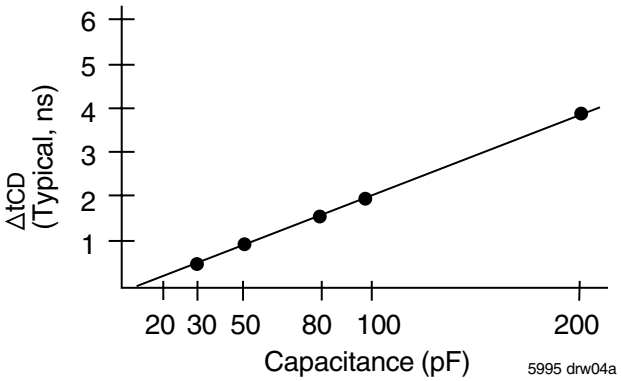


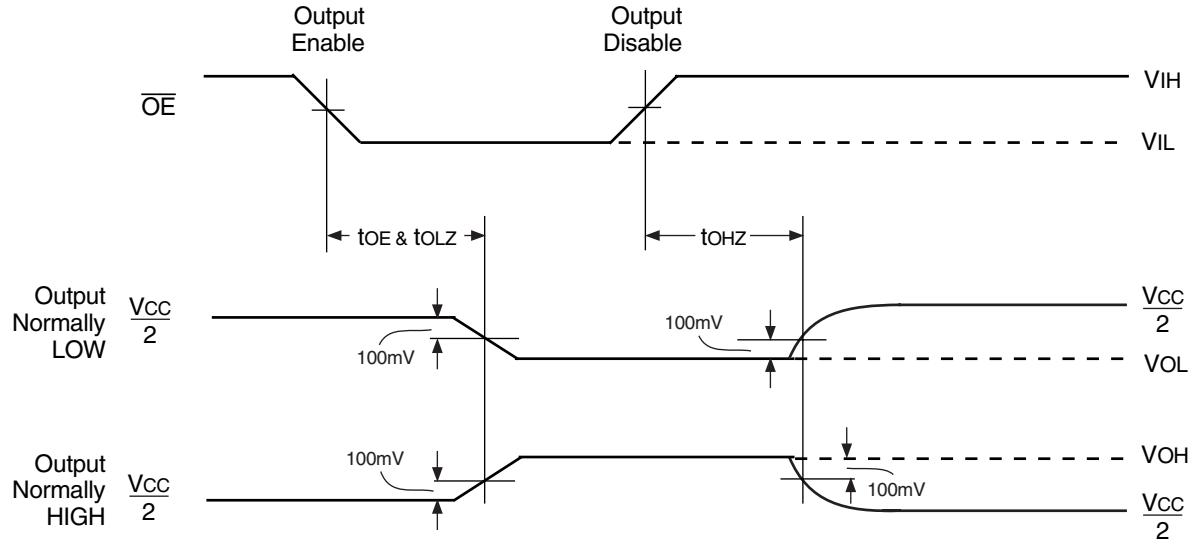
Figure 2b. Lumped Capacitive Load, Typical Derating

2.5V LVTTL
2.5V AC TEST CONDITIONS

Input Pulse Levels	GND to 2.5V
Input Rise/Fall Times	1ns
Input Timing Reference Levels	$V_{CC}/2$
Output Reference Levels	$V_{DDQ}/2$

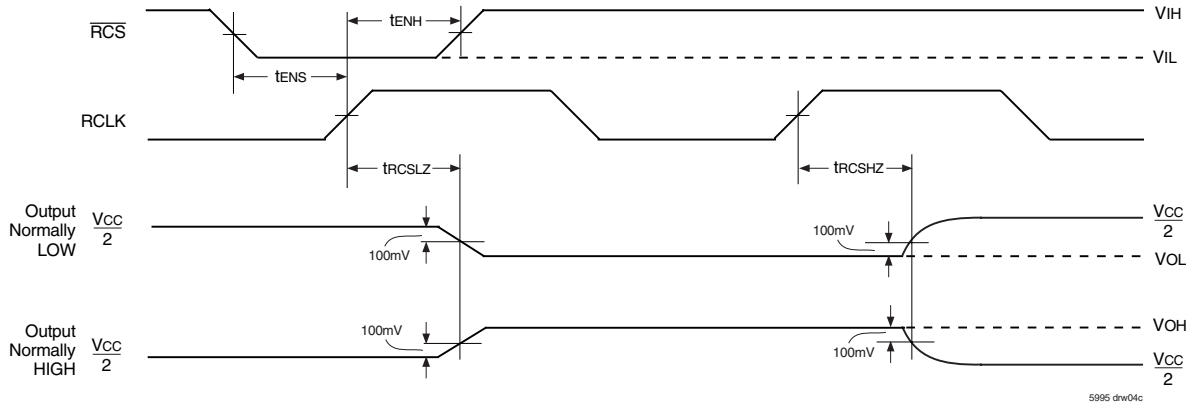
NOTE:
1. For LVTTL V_{CC} = V_{DDQ}.

OUTPUT ENABLE & DISABLE TIMING



NOTES:
1. $\overline{REN}$ is HIGH.
2. $\overline{RCS}$ is LOW.

READ CHIP SELECT ENABLE & DISABLE TIMING



NOTES:
1. $\overline{REN}$ is HIGH.
2. $\overline{OE}$ is LOW.

FUNCTIONAL DESCRIPTION

TIMING MODES: IDT STANDARD vs FIRST WORD FALL THROUGH (FWFT) MODE

The IDT72T4088/72T4098/72T40108/72T40118 support two different timing modes of operation: IDT Standard mode or First Word Fall Through (FWFT) mode. The selection of which mode will operate is determined during Master Reset, by the state of the FWFT input.

During Master Reset, if the FWFT pin is LOW, then IDT Standard mode will be selected. This mode uses the Empty Flag ($\overline{EF}$) to indicate whether or not there are any words present in the FIFO. It also uses the Full Flag function ($\overline{FF}$) to indicate whether or not the FIFO has any free space for writing. In IDT Standard mode, every word read from the FIFO, including the first, must be requested using the Read Enable ($\overline{REN}$) and RCLK.

If the FWFT pin is HIGH during Master Reset, then FWFT mode will be selected. This mode uses Output Ready ($\overline{OR}$) to indicate whether or not there is valid data at the data outputs (Qn). It also uses Input Ready ($\overline{IR}$) to indicate whether or not the FIFO has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to Qn after three RCLK rising edges, applying $\overline{REN}$ = LOW is not necessary. However, subsequent words must be accessed using the Read Enable ($\overline{REN}$) and RCLK.

Various signals, in both inputs and outputs operate differently depending on which timing mode is in effect.

IDT STANDARD MODE

In this mode, the status flags $\overline{FF}$, $\overline{PAF}$, $\overline{PAE}$, and $\overline{EF}$ operate in the manner outlined in Table 4. To write data into the FIFO, Write Enable ($\overline{WEN}$) must be LOW. Data presented to the DATA IN lines will be clocked into the FIFO on subsequent transitions of the Write Clock (WCLK). After the first write is performed, the Empty Flag ($\overline{EF}$) will go HIGH. Subsequent writes will continue to fill up the FIFO. The Programmable Almost-Empty flag ($\overline{PAE}$) will go HIGH after n + 1 words have been loaded into the FIFO, where n is the empty offset value. The default setting for these values are listed in Table 3. This parameter is also user programmable. See section on Programmable Flag Offset Loading.

Continuing to write data into the FIFO without performing read operations will cause the Programmable Almost-Full flag ($\overline{PAF}$) to go LOW. Again, if no reads are performed, the $\overline{PAF}$ will go LOW after (16,384-m) writes for the IDT72T4088, (32,768-m) writes for the IDT72T4098, (65,536-m) writes for the IDT72T40108 and (131,072-m) writes for the IDT72T40118. The offset "m" is the full offset value. The default setting for these values are listed in Table 3. This parameter is also user programmable. See the section on Programmable Flag Offset Loading.

When the FIFO is full, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. If no reads are performed after a reset, $\overline{FF}$ will go LOW after D writes to the FIFO. D = 16,384 writes for the IDT72T4088, 32,768 writes for the IDT72T4098, 65,536 writes for the IDT72T40108 and 131,072 writes for the IDT72T40118, respectively.

If the FIFO is full, the first read operation will cause $\overline{FF}$ to go HIGH. Subsequent read operations will cause $\overline{PAF}$ to go HIGH at the conditions described in Table 4 If further read operations occur, without write operations, $\overline{PAE}$ will go LOW when there are n words in the FIFO, where n is the empty offset value. Continuing read operations will cause the FIFO to become empty. Then the last word has been read from the FIFO, the $\overline{EF}$ will go LOW inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty.

When configured in IDT Standard mode, the $\overline{EF}$ and $\overline{FF}$ outputs are double register-buffered outputs. IDT Standard mode is available when the device is configured in both Single Data Rate and Double Data Rate mode.

Relevant timing diagrams for IDT Standard mode can be found in Figure 10, 11, 12, 13, 14, 15, 16, 17, 18 and 23.

FIRST WORD FALL THROUGH MODE (FWFT)

In this mode, the status flags $\overline{OR}$, $\overline{IR}$, $\overline{PAE}$, and $\overline{PAF}$ operate in the manner outlined in Table 5. To write data into to the FIFO, $\overline{WEN}$ must be LOW. Data presented to the DATA IN lines will be clocked into the FIFO on subsequent transitions of WCLK. After the first write is performed, the Output Ready ($\overline{OR}$) flag will go LOW. Subsequent writes will continue to fill up the FIFO. $\overline{PAE}$ will go HIGH after n + 2 words have been loaded into the FIFO, where n is the empty offset value. The default setting for these values are listed in Table 3. This parameter is also user programmable. See section on Programmable Flag Offset Loading.

Continuing to write data into the FIFO without performing read operations will cause the Programmable Almost-Full flag ($\overline{PAF}$) to go LOW. Again, if no reads are performed, the $\overline{PAF}$ will go LOW after (16,385-m) writes for the IDT72T4088, (32,769-m) writes for the IDT72T4098, (65,537-m) writes for the IDT72T40108 and (131,073-m) writes for the IDT72T40118. The offset "m" is the full offset value. The default setting for these values are listed in Table 3. This parameter is also user programmable. See the section on Programmable Flag Offset Loading.

When the FIFO is full, the Input Ready ($\overline{IR}$) will go LOW, inhibiting further write operations. If no reads are performed after a reset, $\overline{IR}$ will go LOW after D writes to the FIFO. D = 16,385 writes for the IDT72T4088, 32,769 writes for the IDT72T4098, 65,537 writes for the IDT72T40108 and 131,073 writes for the IDT72T40118, respectively. Note that the additional word in FWFT mode is due to the capacity of the memory plus output register.

If the FIFO is full, the first read operation will cause $\overline{IR}$ to go HIGH. Subsequent read operations will cause $\overline{PAF}$ to go HIGH at the conditions described in Table 5. If further read operations occur, without write operations, $\overline{PAE}$ will go LOW when there are n words in the FIFO, where n is the empty offset value. Continuing read operations will cause the FIFO to become empty. Then the last word has been read from the FIFO, the $\overline{OR}$ will go HIGH inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty.

When configured in FWFT mode, the $\overline{OR}$ flag output is triple register-buffered and the $\overline{IR}$ flag output is double register-buffered. FWFT mode is only available when the device is configured in Single Data Rate mode.

Relevant timing diagrams for IDT Standard mode can be found in Figure 19, 20, 21, 22 and 24.

TABLE 3 — DEFAULT PROGRAMMABLE FLAG OFFSETS

IDT72T4088, 72T4098, 72T40108, 72T40118		
FSEL1	FSEL0	Offsets n,m
H	H	255
L	H	127
H	L	63
L	L	7

NOTES:
1. n = empty offset for $\overline{PAE}$.
2. m = full offset for $\overline{PAF}$.

PROGRAMMING FLAG OFFSETS

Full and Empty Flag offset values are user programmable. The IDT72T4088/72T4098/72T40108/72T40118 have internal registers for these offsets. There are four selectable default offset values during Master Reset. These offset values are shown in Table 3. The offset values can also be programmed serially into the FIFO. To load offset values, set $\overline{SEN}$ LOW and the rising edge of SCLK will load data from the SI input into the offset registers. SCLK runs at a nominal speed of 10MHz at the maximum. The programming sequence starts with one bit for each SCLK rising edge, starting with the Empty Offset LSB and ending with the Full Offset MSB. The total number of bits per device is listed in Figure 3, *Programmable Flag Offset Programming Sequence*. See Figure 25, *Loading of Programmable Flag Registers*, for the timing diagram for this mode. The $\overline{PAE}$ and $\overline{PAF}$ can show a valid status only after the complete set of bits (for all offset registers) has been entered. The registers can be reprogrammed as long as the complete set of new offset bits is entered.

In addition to loading offset values into the FIFO, it is also possible to read the current offset values. Similar to loading offset values, set $\overline{SREN}$ LOW and the rising edge of SCLK will send data from the offset registers out to the SO output port. When initializing a read to the offset registers, data will be read starting from the first location in the register, regardless of where it was last read.

Figure 3, *Programmable Flag Offset Programming Sequence*, summarizes the control pins and sequence for programming offset registers and reading and writing into the FIFO.

The offset registers may be programmed (and reprogrammed) any time after Master Reset. Valid programming ranges are from 0 to D-1.

TABLE 4 — STATUS FLAGS FOR IDT STANDARD MODE

	IDT72T4088	IDT72T4098	IDT72T40108	IDT72T40118	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
Number of Words in FIFO	0	0	0	0	H	H	L	L
	1 to n (1)	1 to n (1)	1 to n (1)	1 to n (1)	H	H	L	H
	(8,193) to (16,384-(m+1))	(16,385) to (32,768-(m+1))	(32,769) to (65,536-(m+1))	(65,537) to (131,072-(m+1))	H	H	H	H
	(16,384-m) to 16,383	(32,768-m) to 32,767	(65,536-m) to 65,535	(131,072-m) to 131,071	H	L	H	H
	16,384	32,768	65,536	131,072	L	L	H	H

NOTE:
1. See table 3 for values for n, m.

TABLE 5 — STATUS FLAGS FOR FWFT MODE

	IDT72T4088	IDT72T4098	IDT72T40108	IDT72T40118	$\overline{IR}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{OR}$
Number of Words in FIFO	0	0	0	0	L	H	L	H
	1 to n+1 (1)	1 to n+1 (1)	1 to n+1 (1)	1 to n+1 (1)	L	H	L	L
	(8,194) to (16,385-(m+1))	(16,386) to (32,769-(m+1))	(32,770) to (65,537-(m+1))	(65,538) to (131,073-(m+1))	L	H	H	L
	(16,385-m) to 16,384	(32,769-m) to 32,768	(65,537-m) to 65,536	(131,073-m) to 131,072	L	L	H	L
	16,385	32,769	65,537	131,073	H	L	H	L

5995 drw05

NOTE:
1. See table 3 for values for n, m.
2. FWFT mode available only in Single Data Rate mode.

$\overline{WSDR}$	$\overline{RSDR}$	$\overline{WEN}$	$\overline{REN}$	$\overline{SEN}$	$\overline{SREN}$	WCLK	RCLK	SCLK	IDT72T4088 IDT72T4098 IDT72T40108 IDT72T40118	
X	X	1	1	0	1	X	X	↑	Serial write to registers: In SDR Mode	Serial write to registers: In DDR Mode
									28 bits for the IDT72T4088 30 bits for the IDT72T4098 32 bits for the IDT72T40108 34 bits for the IDT72T40118 1 bit for each rising SCLK edge Starting with Empty Offset (LSB) Ending with Full Offset (MSB)	26 bits for the IDT72T4088 28 bits for the IDT72T4098 30 bits for the IDT72T40108 32 bits for the IDT 72T40118 1 bit for each rising SCLK edge Starting with Empty Offset (LSB) Ending with Full Offset (MSB)
X	X	1	1	1	0	X	X	↑	Serial read from registers: In SDR Mode	Serial read from registers: In DDR Mode
									28 bits for the IDT72T4088 30 bits for the IDT72T4098 32 bits for the IDT72T40108 34 bits for the IDT72T40118 1 bit for each rising SCLK edge Starting with Empty Offset (LSB) Ending with Full Offset (MSB)	26 bits for the IDT72T4088 28 bits for the IDT72T4098 30 bits for the IDT72T40108 32 bits for the IDT72T40118 1 bit for each rising SCLK edge Starting with Empty Offset (LSB) Ending with Full Offset (MSB)
1	1	0	1	X	X	↑↓	X	X	Write Memory (DDR)	
0	1	0	1	X	X	↑	X	X	Write Memory (SDR)	
1	1	1	0	X	X	X	↑↓	X	Read Memory (DDR)	
1	0	1	0	X	X	X	↑	X	Read Memory (SDR)	
X	X	1	1	X	X	X	X	X	No Operation	

5995 drw06

NOTES:

1. The programming sequence applies to both IDT Standard and FWFT modes.
2. When the input or output ports are in DDR mode, the depth is reduced by half but the overall density remains the same. For example, the IDT72T4088 in SDR mode is 16,384 x 40 = 655,360, in DDR mode the configuration becomes 8,192 x 80 = 655,360. In both cases, the total density are the same.

Figure 3. Programmable Flag Offset Programming Sequence

RETRANSMIT FROM MARK OPERATION

The Retransmit from Mark feature allows FIFO data to be read repeatedly starting at a user-selected position. The FIFO is first put into retransmit mode that will "mark" a beginning word and also set a pointer that will prevent ongoing FIFO write operations from over-writing retransmit data. The retransmit data can be read repeatedly any number of times from the "marked" position. The FIFO can be taken out of retransmit mode at any time to allow normal device operation. The "mark" position can be selected any number of times, each selection over-writing the previous mark location.

In Double Data Rate, data is always marked in pairs. That is, the unit of data read on the rising and falling edge of WCLK. If the data marked was read on the falling edge of RCLK, then the marked data will be the unit of data read from the rising and falling edge of that particular RCLK edge. Refer to Figure 23, *Retransmit from Mark in Double Data Rate Mode*, for the timing diagram in this mode. Retransmit operation is available in both IDT standard and FWFT modes.

During IDT standard mode the FIFO is put into retransmit mode by a Low-to-High transition on RCLK when the MARK input is HIGH and $\overline{EF}$ is HIGH. The rising RCLK edge marks the data present in the FIFO output register as the first retransmit data. Again, the data is marked in pairs. Thus if the data marked was read on the falling edge of RCLK, the first part of retransmit will read out the data read on the rising edge of RCLK, followed by the data on the falling edge (the marked data). The FIFO remains in retransmit mode until a rising edge on RCLK occurs while MARK is LOW.

Once a marked location has been set, a retransmit can be initiated by a rising edge on RCLK while the Retransmit input ($\overline{RT}$) is LOW. $\overline{REN}$ must be HIGH (reads disabled) before bringing $\overline{RT}$ LOW. The device indicates the start of retransmit setup by setting $\overline{EF}$ LOW, also preventing reads. When $\overline{EF}$ goes HIGH, retransmit setup is complete and read operations may begin starting with the first unit of data at the MARK location. Since IDT standard mode is selected, every word read including the first "marked" word following a retransmit setup requires a LOW on $\overline{REN}$.

Note, write operations may continue as normal during all retransmit functions, however write operations to the "marked" location will be prevented. See Figure 23, *Retransmit from Mark in Double Data Rate Mode*, for the relevant timing diagram.

During FWFT mode the FIFO is put into retransmit mode by a rising RCLK edge when the MARK input is HIGH and $\overline{OR}$ is LOW. The rising RCLK edge marks the data present in the FIFO output register as the first retransmit data. The data is marked in pairs. The FIFO remains in retransmit mode until a rising RCLK edge occurs while MARK is LOW.

Once a marked location has been set, a retransmit can be initiated by a rising RCLK edge while the Retransmit input ($\overline{RT}$) is LOW. $\overline{REN}$ must be HIGH (reads disabled) before bringing $\overline{RT}$ LOW. The device indicates the start of retransmit setup by setting $\overline{OR}$ HIGH, preventing read operations.

When $\overline{OR}$ goes LOW, retransmit setup is complete and on the next rising RCLK edge ($\overline{RT}$ goes HIGH), the contents of the first retransmit location are loaded onto the output register. Since FWFT mode is selected, the first word appears on the outputs regardless of $\overline{REN}$, a LOW on $\overline{REN}$ is not required for the first word. Reading all subsequent words requires a LOW on $\overline{REN}$ to enable the rising RCLK edge. See Figure 24, *Retransmit from Mark (FWFT mode)* for the relevant timing diagram.

Before a retransmit can be performed, there must be at least 1280 bits (or 160 bytes) of data between the write pointer and mark location. That is, 40 bits x32 for the x40 mode, 20 bits x64 for the x20 mode, and 10 bits x128 for the x10 mode. Also, once the Mark is set, the write pointer will not increment past the marked location, preventing overwrites of retransmit data.

HSTL/LVTTL I/O

This device supports both LVTTL and HSTL logic levels on the input and output signals. If LVTTL is desired, a LOW on the HSTL pin will set the inputs and outputs to LVTTL mode. If HSTL is desired, a HIGH on the HSTL pin will set the inputs and outputs to HSTL mode. VREF is the input voltage reference used in HSTL mode. Typically a logic HIGH in HSTL would be Vref + 0.2V and a logic LOW would be VREF – 0.2V. Table 6 illustrates which pins are and are not associated with this feature. Note that all "Static Pins" must be tied to Vcc or GND. These pins are LVTTL only and are purely device configuration pins.

TABLE 6 — I/O CONFIGURATION

HSTL SELECT					STATIC PINS
HIGH = HSTL LOW = LVTTL					LVTTL ONLY
Write Port	**Read Port**		**Signal Pins**		**Static Pins**
Dn (I/P) WCLK (I/P) $\overline{WEN}$ (I/P) $\overline{WCS}$ (I/P)	Qn (O/P) RCLK (I/P) $\overline{REN}$ (I/P) $\overline{RCS}$ (I/P) MARK (I/P) $\overline{OE}$ (I/P) $\overline{RT}$ (I/P)	$\overline{EF}$/$\overline{OR}$ (O/P) $\overline{PAF}$ (O/P) $\overline{PAE}$ (O/P) $\overline{FF}$/$\overline{IR}$ (O/P) ERCLK (O/P) $\overline{EREN}$ (O/P)	SCLK (I/P) SI (I/P) SO (O/P) $\overline{MRS}$ (I/P) $\overline{PRS}$ (I/P) TCK (I/P) TMS (I/P)	$\overline{TRST}$ (I/P) TDI (I/P) TDO (O/P) $\overline{SEN}$ (I/P) $\overline{SREN}$ (I/P)	IW (I/P) OW (I/P) BM ((I/P) HSTL (I/P) FSEL1 (I/P) FSEL0 (I/P) FWFT (I/P) $\overline{WSDR}$ (I/P) $\overline{RSDR}$ (I/P)

SIGNAL DESCRIPTION

INPUTS:

DATA IN (D0 – Dn)

(D_0 – D_{39}) are data inputs for the 40-bit wide data, (D_0 – D_{19}) are data inputs for the 20-bit wide data, or (D_0 – D_9) are data inputs for 10-bit wide data.

CONTROLS:

MASTER RESET ($\overline{MRS}$)

A Master Reset is accomplished whenever the $\overline{MRS}$ input is taken to a LOW state. This operation sets the internal read and write pointers to the first location of the RAM array. $\overline{PAE}$ will go LOW and $\overline{PAF}$ will go HIGH.

If FWFT is LOW during Master Reset then IDT Standard mode along with $\overline{EF}$ and $\overline{FF}$ are selected. $\overline{EF}$ will go LOW and $\overline{FF}$ will go HIGH, If FWFT is HIGH, then the First Word Fall Through (FWFT) mode, along with $\overline{IR}$ and $\overline{OR}$ are selected. $\overline{OR}$ will go HIGH and $\overline{IR}$ will go LOW.

All control settings such as OW, IW, BM, $\overline{WSDR}$, $\overline{RSDR}$, FSEL0 and FSEL1 are defined during the Master Reset cycle.

During a Master Reset the output register is initialized to all zeros. A Master Reset is required after power up before a write operation can take place. $\overline{MRS}$ is asynchronous.

See Figure 8, *Master Reset Timing*, for the relevant timing diagram.

PARTIAL RESET ($\overline{PRS}$)

A Partial Reset is accomplished whenever the $\overline{PRS}$ input is taken to a LOW state. As in the case of the Master Reset, the internal read and write pointers are set to the first location of the RAM array. $\overline{PAE}$ goes LOW and $\overline{PAF}$ goes HIGH.

Whichever mode was active at the time of Partial Reset will remain active after Partial Reset. If IDT Standard Mode is active, then $\overline{FF}$ will go HIGH and $\overline{EF}$ will go LOW. If the First Word Fall Through mode is active, then $\overline{OR}$ will go HIGH and $\overline{IR}$ will go LOW.

Following Partial Reset, all values held in the offset registers remain unchanged. The output register is initialized to all zeroes. $\overline{PRS}$ is asynchronous. Partial Reset is useful for resetting the read and write pointers to zero without affecting the values of the programmable flag offsets and the timing mode of the FIFO.

See Figure 9, *Partial Reset Timing*, for the relevant timing diagram.

RETRANSMIT ($\overline{RT}$)

The Retransmit ($\overline{RT}$) input is used in conjunction with the MARK input. Together they provide a means by which data previously read out of the FIFO can be reread any number of times. When the retransmit operation is selected (i.e. after data has been marked), a rising edge on RCLK while $\overline{RT}$ is LOW will reset the read pointer back to the memory location set by the user via the MARK input.

If IDT Standard mode has been selected, the $\overline{EF}$ flag will go LOW on the rising edge of RCLK that retransmit was initiated (i.e. rising edge of RCLK while $\overline{RT}$ is LOW). $\overline{EF}$ will go back to HIGH on the next rising edge of RCLK, which signifies that retransmit setup is complete. The next read operation will access data from the "marked" memory location.

Subsequent retransmit operations may be performed, each time the read pointer returning to the "marked" location. See Figure 23, *Retransmit from Mark in Double Data Rate Mode (IDT Standard Mode)* for the relevant timing diagram.

If FWFT mode has been selected, the $\overline{OR}$ flag will go HIGH on the rising edge of RCLK that retransmit was initiated. $\overline{OR}$ will return LOW on the next rising edge of RCLK, which signifies that retransmit setup is complete. Under FWFT mode, the contents in the marked memory location will be loaded onto the output register on the next rising edge of RCLK. To access all subsequent data, a read operation will be required.

Subsequent retransmit operations may be performed, each time the read pointer returning to the "marked" location. See Figure 24, *Retransmit from Mark (FWFT Mode)* for the relevant timing diagram.

MARK

The MARK input is used to select Retransmit mode of operation. On a rising edge of RCLK while MARK is HIGH will mark the memory location of the data currently present on the output register, in addition placing the device in retransmit mode. Note, there must be a minimum of 1280 bits (or 160 bytes) of data between the write pointer and mark location. That is, 40 bits x32 for the x40 mode, 20 bits x64 for the x20 mode, and 10 bits x128 for the x10 mode. Also, once the MARK is set, the write pointer will not increment past the "marked" location until the MARK is deasserted. This prevents "overwriting" of retransmit data.

The MARK input must remain HIGH during the whole period of retransmit mode, a falling edge of RCLK while MARK is LOW will take the device out of retransmit mode and into normal mode. Any number of MARK locations can be set during FIFO operation, only the last marked location taking effect. Once a mark location has been set the write pointer cannot be incremented past this marked location. During retransmit mode write operations to the device may continue without hindrance.

FIRST WORD FALL THROUGH (FWFT)

During Master Reset, the state of the FWFT input determines whether the device will operate in IDT Standard mode or First Word Fall Through (FWFT) mode.

If, at the time of Master Reset, FWFT is LOW, then IDT Standard mode will be selected. This mode uses the Empty Flag ($\overline{EF}$) to indicate whether or not there are any words present in the FIFO memory. It also uses the Full Flag function ($\overline{FF}$) to indicate whether or not the FIFO memory has any free space for writing. In IDT Standard mode, every word read from the FIFO, including the first, must be requested using the Read Enable ($\overline{REN}$) and RCLK.

If, at the time of Master Reset, FWFT is HIGH, then FWFT mode will be selected. This mode uses Output Ready ($\overline{OR}$) to indicate whether or not there is valid data at the outputs (Qn) to be read. It also uses Input Ready ($\overline{IR}$) to indicate whether or not the FIFO memory has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to Qn after three RCLK rising edges, bringing $\overline{REN}$ LOW is not necessary. Subsequent words must be accessed using the Read Enable ($\overline{REN}$) and RCLK. Note that FWFT mode can only be used when the device is configured to Single Data Rate (SDR) mode.

WRITE CLOCK (WCLK)

A write cycle is initiated on the rising and/or falling edge of the WCLK input. If the Write Single Data Rate ($\overline{WSDR}$) pin is selected, data will be written only on the rising edge of WCLK, provided that $\overline{WEN}$ and $\overline{WCS}$ are LOW. If the $\overline{WSDR}$ is not selected, data will be written on both the rising and falling edge of WCLK, provided that $\overline{WEN}$ and $\overline{WCS}$ are LOW. Data setup and hold times must be met with respect to the LOW-to-HIGH transition of the WCLK. It is permissible to stop the WCLK. Note that while WCLK is idle, the $\overline{FF}$, $\overline{IR}$, and $\overline{PAF}$ flags will not be updated. The write and read clocks can either be independent or coincident.

WRITE ENABLE ($\overline{WEN}$)

When the $\overline{WEN}$ input is LOW, data may be loaded into the FIFO RAM array on the rising edge of every WCLK cycle if the device is not full. Data is stored in the RAM array sequentially and independently of any ongoing read operation.

When $\overline{WEN}$ is HIGH, no new data is written in the RAM array on each WCLK cycle.

To prevent data overflow in the IDT Standard mode, $\overline{FF}$ will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, $\overline{FF}$ will go HIGH, allowing a write to occur. The $\overline{FF}$ is updated by two WCLK cycles + t_{SKEW} after the RCLK cycle.

To prevent data overflow in the FWFT mode, $\overline{IR}$ will go HIGH, inhibiting further write operations. Upon the completion of a valid read cycle, $\overline{IR}$ will go LOW, allowing a write to occur. The $\overline{IR}$ flag is updated by two WCLK cycles + t_{SKEW} after the valid RCLK cycle.

$\overline{WEN}$ is ignored when the FIFO is full in either IDT Standard mode or FWFT.

WRITE SINGLE DATA RATE ($\overline{WSDR}$)

When the Write Single Data Rate pin is LOW, the write port will be set to Single Data Rate mode. In this mode, all write operations are based only on the rising edge of WCLK, provided that $\overline{WEN}$ and $\overline{WCS}$ are LOW. When $\overline{WSDR}$ is HIGH, the read port will be set to Double Data Rate mode. In this mode, all write operations are based on both the rising and falling edge of WCLK, provided that $\overline{WEN}$ and $\overline{WCS}$ are LOW, on the rising edge of WCLK.

READ CLOCK (RCLK)

A read cycle is initiated on the rising and/or falling edge of the RCLK input. If the Read Single Data Rate ($\overline{RSDR}$) pin is selected, data will be read only on the rising edge of RCLK, provided that $\overline{REN}$ and $\overline{RCS}$ are LOW. If the $\overline{RSDR}$ is not selected, data will be read on both the rising and falling edge of WCLK, provided that $\overline{REN}$ and $\overline{RCS}$ are LOW, on the rising edge of RCLK. Setup and hold times must be met with respect to the LOW-to-HIGH transition of the RCLK. It is permissible to stop the RCLK. Note that while RCLK is idle, the $\overline{EF}$/$\overline{OR}$ and $\overline{PAE}$ flags will not be updated. Write and Read Clocks can be independent or coincident.

READ ENABLE ($\overline{REN}$)

When Read Enable is LOW, data is loaded from the RAM array into the output register on the rising edge of every RCLK cycle if the device is not empty.

When the $\overline{REN}$ input is HIGH, the output register holds the previous data and no new data is loaded into the output register. The data outputs Q0-Qn maintain the previous data value.

In IDT Standard mode, every word accessed at Qn, including the first word written to an empty FIFO, must be requested using $\overline{REN}$ provided that the Read Chip Select ($\overline{RCS}$) is LOW. When the last word has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty. Once a write is performed, $\overline{EF}$ will go HIGH allowing a read to occur. Both $\overline{RCS}$ and $\overline{REN}$ must be active LOW for data to be read out on the rising edge of RCLK.

In FWFT mode, the first word written to an empty FIFO automatically goes to the outputs Qn, on the third valid LOW-to-HIGH transition of RCLK + t_{SKEW} after the first write. $\overline{REN}$ and $\overline{RCS}$ do not need to be asserted LOW for the First Word to fall through to the output register. All subsequent words require that a read operation to be executed using $\overline{REN}$ and $\overline{RCS}$. The LOW-to-HIGH transition of RCLK after the last word has been read from the FIFO will make Output Ready ($\overline{OR}$) go HIGH with a true read (RCLK with $\overline{REN}$ and $\overline{RCS}$ LOW), inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty.

READ SINGLE DATA RATE ($\overline{RSDR}$)

When the Read Single Data Rate pin is LOW, the read port will be set to Single Data Rate mode. In this mode, all read operations are based only on the rising edge of RCLK, provided that $\overline{REN}$ and $\overline{RCS}$ are LOW. When $\overline{RSDR}$ is HIGH, the read port will be set to Double Data Rate mode. In this mode, all read operations are based on both the rising and falling edge of RCLK, provided that $\overline{REN}$ and $\overline{RCS}$ are LOW, on the rising edge of RCLK.

SERIAL CLOCK (SCLK)

The serial clock is used to load and read data in the programmable offset registers. Data from the Serial Input (SI) can be loaded into the offset registers on the rising edge of SCLK provided that $\overline{SEN}$ is LOW. Data can be read from the offset registers via the Serial Output (SO) on the rising edge of SCLK provided that $\overline{SREN}$ is LOW. The serial clock can operate at a maximum frequency of 10MHz and its parameters are different than the FIFO system clock.

SERIAL ENABLE ($\overline{SEN}$)

The $\overline{SEN}$ input is an enable used for serial programming of the programmable offset registers. It is used in conjunction with SI and SCLK when programming the offset registers. When $\overline{SEN}$ is LOW, data at the Serial In (SI) input can be loaded into the offset register, one bit for each LOW-to-HIGH transition of SCLK.

When $\overline{SEN}$ is HIGH, the offset registers retain the previous settings and no offsets are loaded. $\overline{SEN}$ functions the same way in both IDT Standard and FWFT modes.

SERIAL READ ENABLE ($\overline{SREN}$)

The $\overline{SREN}$ output is an enable used for reading the value of the programmable offset registers. It is used in conjunction with SI and SCLK when reading from the offset registers. When $\overline{SREN}$ is LOW, data can be read out of the offset register from the SO output, one bit for each LOW-to-HIGH transition of SCLK.

When $\overline{SREN}$ is HIGH, the reading of the offset registers will stop. Whenever $\overline{SREN}$ is activated values in the offset registers are read starting from the first location in the offset registers and not from where the last offset value was read. $\overline{SREN}$ functions the same way in both IDT Standard and FWFT modes.

SERIAL IN (SI)

This pin acts as a serial input for loading $\overline{PAE}$ and $\overline{PAF}$ offsets into the programmable offset registers. It is used in conjunction with the Serial Clock (SCLK) and the Serial Enable ($\overline{SEN}$). Data from this input can be loaded into the offset register, one bit for each LOW-to-HIGH transition of SCLK provided that $\overline{SEN}$ is LOW.

SERIAL OUT (SO)

This pin acts as a serial output for reading the values of the $\overline{PAE}$ and $\overline{PAF}$ offsets in the programmable offset registers. It is used in conjunction with the Serial Clock (SCLK) and the Serial Enable Output ($\overline{SREN}$). Data from the offset register can be read out using this pin, one-bit for each LOW-to-HIGH transition of SCLK provided that $\overline{SREN}$ is LOW.

OUTPUT ENABLE ($\overline{OE}$)

When Output Enable is LOW, the parallel output buffers receive data from the output register. When $\overline{OE}$ is HIGH, the output data bus (Qn) goes into a high-impedance state. During Master or Partial Reset the $\overline{OE}$ is the only input that can place the output data bus into high-impedance. During reset the $\overline{RCS}$ input can be HIGH or LOW and has no effect on the output data bus.

READ CHIP SELECT ($\overline{RCS}$)

The Read Chip Select input provides synchronous control of the Read output port. When $\overline{RCS}$ goes LOW, the next rising edge of RCLK causes the Qn outputs to go to the low-impedance state. When $\overline{RCS}$ goes HIGH, the next RCLK rising edge causes the Qn outputs to return to high-impedance. During a Master or Partial Reset the $\overline{RCS}$ input has no effect on the Qn output bus, $\overline{OE}$ is the only input that provides high-impedance control of the Qn outputs. If $\overline{OE}$ is LOW, the Qn data outputs will be low-impedance regardless of $\overline{RCS}$ until the first rising edge of RCLK after a reset is complete. Then if $\overline{RCS}$ is HIGH the data outputs will go to high-impedance.

The $\overline{RCS}$ input does not effect the operation of the flags. For example, when the first word is written to an empty FIFO, the $\overline{EF}$ will still go from LOW to HIGH based on a rising edge of RCLK, regardless of the state of the $\overline{RCS}$ input.

Also, when operating the FIFO in FWFT mode the first word written to an empty FIFO will still be clocked through to the output register based on RCLK, regardless of the state of $\overline{RCS}$. For this reason the user should pay extra attention when a data word is written to an empty FIFO in FWFT mode. If $\overline{RCS}$ is HIGH when an empty FIFO is written into, the first word will fall through to the output register but will not be available on the Qn outputs because they are in high-impedance. The user must take $\overline{RCS}$ active LOW to access this first word, placing the output bus in low-impedance. $\overline{REN}$ must remain HIGH for at least one cycle after $\overline{RCS}$ has gone LOW. A rising edge of RCLK with $\overline{RCS}$ and $\overline{REN}$ LOW will read out the next word. Care must be taken so as not to lose the first word written to an empty FIFO when $\overline{RCS}$ is HIGH. Refer to Figure 22, *$\overline{RCS}$ and $\overline{REN}$ Read Operation (FWFT Mode).* The $\overline{RCS}$ pin must also be active (LOW) in order to perform a Retransmit. See Figure 18 for *Read Cycle and Read Chip Select Timing (IDT Standard Mode).* See Figure 21 for *Read Cycle and Read Chip Select Timing (FWFT Mode).*

WRITE CHIP SELECT ($\overline{WCS}$)

The $\overline{WCS}$ disables all Write Port inputs (data only) if it is held HIGH. To perform normal operations on the write port, the $\overline{WCS}$ must be enabled.

HSTL SELECT (HSTL)

The inputs that were listed in Table 6 can be setup to be either HSTL or LVTTL. If HSTL is HIGH, then HSTL operation of those signals will be selected. If HSTL is LOW , then LVTTL will be selected.

BUS-MATCHING (BM, IW, OW)

The pins BM, IW, and OW are used to define the input and output bus widths. During Master Reset, the state of these pins is used to configure the device bus sizes. See Table 1 for control settings. All flags will operate on the word/byte size boundary as defined by the selection of bus width. See Table 7 for Bus-Matching Write to Read Ratio.

FLAG SELECT BITS (FSEL0 and FSEL1)

These pins will select the four default offset values for the $\overline{PAE}$ and $\overline{PAF}$ flags during Master Reset. The four possible settings are listed on Table 3. Note that the status of these inputs should not change after Master Reset.

OUTPUTS:

DATA OUT (Q0-Q39)

(Q0 – Q39) are data outputs for 40-bit wide data, (Q0 – Q19) are data outputs for 20-bit wide data, or (Q0 – Q9) are data outputs for 10-bit wide data.

FULL FLAG ($\overline{FF}$/$\overline{IR}$)

This is a dual-purpose pin. In IDT Standard mode, the Full Flag ($\overline{FF}$) function is selected. When the FIFO is full, $\overline{FF}$ will go LOW, inhibiting further write operations. When $\overline{FF}$ is HIGH, the FIFO is not full. If no reads are performed after a reset (either $\overline{MRS}$ or $\overline{PRS}$), $\overline{FF}$ will go LOW after D writes to the FIFO (D = 16,384 for the IDT72T4088, 32,768 for the IDT72T4098, 65,536 for the IDT72T40108, 131,072 for the IDT72T40118. See Figure 10, *Write Cycle and Full Flag Timing (IDT Standard Mode*), for the relevant timing information.

In FWFT mode, the Input Ready ($\overline{IR}$) function is selected. $\overline{IR}$ goes LOW when memory space is available for writing in data. When there is no longer any free space left, $\overline{IR}$ goes HIGH, inhibiting further write operations. If no reads are performed after a reset (either $\overline{MRS}$ or $\overline{PRS}$), $\overline{IR}$ will go HIGH after D writes to the FIFO (D = 16,385 for the IDT72T4088, 32,769 for the IDT72T4098, 65,537 for the IDT72T40108, 131,073 for the IDT72T40118). See Figure 19, *Write Timing (FWFT Mode*), for the relevant timing information.

The $\overline{IR}$ status not only measures the contents of the FIFO memory, but also counts the presence of a word in the output register. Thus, in FWFT mode, the total number of writes necessary to deassert $\overline{IR}$ is one greater than needed to assert $\overline{FF}$ in IDT Standard mode.

$\overline{FF}$/$\overline{IR}$ is synchronous and updated on the rising edge of WCLK. $\overline{FF}$/$\overline{IR}$ are double register-buffered outputs.

Note, when the device is in Retransmit mode, this flag is a comparison of the write pointer to the "marked" location. This differs from normal mode where this flag is a comparison of the write pointer to the read pointer.

EMPTY FLAG ($\overline{EF}$/$\overline{OR}$)

This is a dual-purpose pin. In the IDT Standard mode, the Empty Flag ($\overline{EF}$) function is selected. When the FIFO is empty, $\overline{EF}$ will go LOW, inhibiting further read operations. When $\overline{EF}$ is HIGH, the FIFO is not empty. See Figure 12, *Read Cycle, Empty Flag and First Word Latency Timing (IDT Standard Mode*), for the relevant timing information.

In FWFT mode, the Output Ready ($\overline{OR}$) function is selected. $\overline{OR}$ goes LOW at the same time that the first word written to an empty FIFO appears valid on the outputs. $\overline{OR}$ stays LOW after the RCLK LOW to HIGH transition that shifts the last word from the FIFO memory to the outputs. $\overline{OR}$ goes HIGH only with a true read (RCLK with $\overline{REN}$ = LOW). The previous data stays at the outputs, indicating the last word was read. Further data reads are inhibited until $\overline{OR}$ goes LOW again. See Figure 20, *Read Timing (FWFT Mode*), for the relevant timing information.

$\overline{EF}$/$\overline{OR}$ is synchronous and updated on the rising edge of RCLK.

In IDT Standard mode, $\overline{EF}$ is a double register-buffered output. In FWFT mode, $\overline{OR}$ is a triple register-buffered output.

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

The Programmable Almost-Full flag ($\overline{PAF}$) will go LOW when the FIFO reaches the almost-full condition. In IDT Standard mode, if no reads are performed after reset ($\overline{MRS}$), $\overline{PAF}$ will go LOW after (D - m) words are written to the FIFO. The $\overline{PAF}$ will go LOW after (16,384-m) writes for the IDT72T4088, (32,768-m) writes for the IDT72T4098, (65,536-m) writes for the IDT72T40108,

(131,072-m) writes for the IDT72T40118. The offset "m" is the full offset value. The default setting for this value is listed in Table 3.

In FWFT mode, the $\overline{PAF}$ will go LOW after (16,385-m) writes for the IDT72T4088, (32,769-m) writes for the IDT72T4098, (65,537-m) writes for the IDT72T40108, (131,073-m) writes for the IDT72T40118. where m is the full offset value. The default setting for this value is listed in Table 3.

See Figure 29, *Programmable Almost-Full Flag Timing (IDT Standard and FWFT Mode*), for the relevant timing information.

Note, when the device is in Retransmit mode, this flag is a comparison of the write pointer to the "marked" location. This differs from normal mode where this flag is a comparison of the write pointer to the read pointer.

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}$)

The Programmable Almost-Empty flag ($\overline{PAE}$) will go LOW when the FIFO reaches the almost-empty condition. In IDT Standard mode, $\overline{PAE}$ will go LOW when there are n words or less in the FIFO. The offset "n" is the empty offset value. The default setting for this value is stated in the footnote of Table 3.

In FWFT mode, the $\overline{PAE}$ will go LOW when there are n+1 words or less in the FIFO. The default setting for this value is stated in Table 3.

See Figure 30, *Programmable Almost-Empty Flag Timing (IDT Standard and FWFT Mode*), for the relevant timing information.

ECHO READ CLOCK (ERCLK)

The Echo Read Clock output is provided in both HSTL and LVTTL mode, selectable via HSTL. The ERCLK is a free-running clock output, it will always follow the RCLK input regardless of $\overline{REN}$ and $\overline{RCS}$.

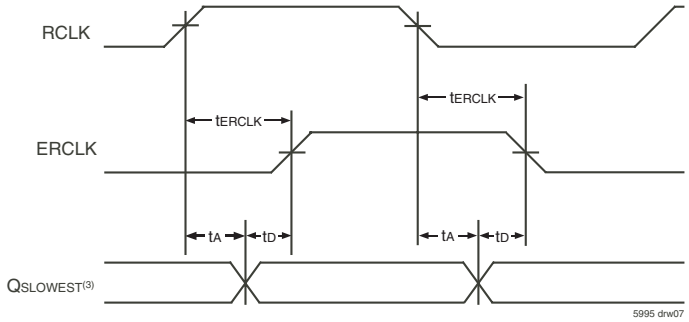
The ERCLK output follows the RCLK input with an associated delay. This delay provides the user with a more effective read clock source when reading data from the Qn outputs. This is especially helpful at high speeds when variables within the device may cause changes in the data access times. These variations in access time maybe caused by ambient temperature, supply voltage, or device characteristics. The ERCLK output also compensates for any trace length delays between the Qn data outputs and receiving devices inputs.

Any variations effecting the data access time will also have a corresponding effect on the ERCLK output produced by the FIFO device, therefore the ERCLK output level transitions should always be at the same position in time relative to the data outputs. Note, that ERCLK is guaranteed by design to be slower than the slowest Qn, data output. Refer to Figure 4, *Echo Read Clock and Data Output Relationship*, Figure 27, *Echo Read Clock & Read Enable Operation in Double Data Rate Mode* and Figure 28, *Echo RCLK & Echo $\overline{REN}$ Operation* for timing information.

ECHO READ ENABLE ($\overline{EREN}$)

The Echo Read Enable output is provided in both HSTL and LVTTL mode, selectable via HSTL.

The $\overline{EREN}$ output is provided to be used in conjunction with the ERCLK output and provides the reading device with a more effective scheme for reading data from the Qn output port at high speeds. The $\overline{EREN}$ output is controlled by internal logic that behaves as follows: The $\overline{EREN}$ output is active LOW for the RCLK cycle that a new word is read out of the FIFO. That is, a rising edge of RCLK will cause $\overline{EREN}$ to go active, LOW if both $\overline{REN}$ and $\overline{RCS}$ are active, LOW and the FIFO is NOT empty.



NOTES:
1. $\overline{REN}$ is LOW.
2. $t_{ERCLK} > t_A$, guaranteed by design.
3. Qslowest is the data output with the slowest access time, t_A.
4. Time, t_D is greater than zero, guaranteed by design.
5. $\overline{REN} = \overline{RCS} = \overline{OE} = 0$.

Figure 4. Echo Read Clock and Data Output Relationship

TABLE 7 — BUS-MATCHING WRITE TO READ RATIO

ONE WRITE TO ONE READ (1:1)

x40 DDR Input to x40 DDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
H	H	L	L	L

DDR Write Clock	x40 Data In	DDR Read Clock	x40 Data Out
Positive Edge 1 Negative Edge 1	D[39:0] <= LW1 D[39:0] <= LW2	Positive Edge 1 Negative Edge 1	Q[39:0] <= LW1 Q[39:0] <= LW2

x40 SDR Input to x40 SDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
L	L	L	L	L

SDR Write Clock	x40 Data In	SDR Read Clock	x40 Data Out
Positive Edge 1	D[39:0] <= LW1	Positive Edge 1	Q[39:0] <= LW1

x40 SDR Input to x20 DDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
L	H	H	L	L

SDR Write Clock	x40 Data In	DDR Read Clock	x20 Data Out
Positive Edge 1	D[39:20] <= W1 D[19:0] <= W2	Positive Edge 1 Negative Edge 1	Q[19:0] <= W1 Q[19:0] <= W2

x20 DDR Input to x40 SDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
H	L	H	H	L

DDR Write Clock	x20 Data In	SDR Read Clock	x40 Data Out
Positive Edge 1 Negative Edge 1	D[19:0] <= W1 D[19:0] <= W2	Positive Edge 1	Q[39:20] <= W1 Q[19:0] <= W2

ONE WRITE TO TWO READ (1:2)

x40 DDR Input to x40 SDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
H	L	L	L	L

DDR Write Clock	x40 Data In	SDR Read Clock	x40 Data Out
Positive Edge 1 Negative Edge 1	D[39:0] <= LW1 D[39:0] <= LW2	Positive Edge 1 Positive Edge 2	Q[39:0] <= LW1 Q[39:0] <= LW1

x40 SDR Input to x20 SDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
L	L	H	L	L

SDR Write Clock	x40 Data In	SDR Read Clock	x20 Data Out
Positive Edge 1	D[39:20] <= LW1 D[19:0] <= LW2	Positive Edge 1 Positive Edge 2	Q[19:0] <= LW1 Q[19:0] <= LW2

x40 DDR Input to x20 DDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
H	H	H	L	L

DDR Write Clock	x40 Data In	DDR Read Clock	x20 Data Out
Positive Edge 1	D[39:20] <= LW1 D[19:0] <= LW2	Positive Edge 1 Negative Edge 1	Q[19:0] <= LW1 Q[19:0] <= LW2
Negative Edge 1	D[39:20] <= LW3 D[19:0] <= LW4	Positive Edge 2 Negative Edge 2	Q[19:0] <= LW3 Q[19:0] <= LW4

x40 SDR Input to x10 DDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
L	H	H	L	H

SDR Write Clock	x40 Data In	DDR Read Clock	x10 Data Out
Positive Edge 1	D[39:30] <= B1 D[29:20] <= B2 D[19:10] <= B3 D[9:0] <= B4	Positive Edge 1 Negative Edge 1 Positive Edge 2 Negative Edge 2	Q[9:0] <= B1 Q[9:0] <= B2 Q[9:0] <= B3 Q[9:0] <= B4

TABLE 7 — BUS-MATCHING WRITE TO READ RATIO (CONTINUED)

ONE WRITE TO FOUR READ (1:4)

x40 DDR Input to x20 SDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
H	L	H	L	L

DDR Write Clock	x40 Data In	SDR Read Clock	x20 Data Out
Positive Edge 1	D[39:20] <= LW1 D[19:0] <= LW2	Positive Edge 1 Positive Edge 2	Q[19:0] <= LW1 Q[19:0] <= LW2
Negative Edge 1	D[39:20] <= LW3 D[19:0] <= LW4	Positive Edge 3 Positive Edge 4	Q[19:0] <= LW3 Q[19:0] <= LW4

x40 SDR Input to x10 SDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
L	L	H	L	H

SDR Write Clock	x40 Data In	SDR Read Clock	x10 Data Out
Positive Edge 1	D[39:30] <= B1 D[29:20] <= B2 D[19:10] <= B3 D[9:0] <= B4	Positive Edge 1 Positive Edge 2 Positive Edge 3 Positive Edge 4	Q[9:0] <= B1 Q[9:0] <= B2 Q[9:0] <= B3 Q[9:0] <= B4

x40 DDR Input to x10 DDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
H	H	H	L	H

DDR Write Clock	x40 Data In	SDR Read Clock	x10 Data Out
Positive Edge 1	D[39:30] <= B1 D[29:20] <= B2 D[19:10] <= B3 D[9:0] <= B4	Positive Edge 1 Negaitive Edge 1 Positive Edge 2 Negaitive Edge 2	Q[9:0] <= B1 Q[9:0] <= B2 Q[9:0] <= B3 Q[9:0] <= B4
Negative Edge 1	D[39:30] <= B5 D[29:20] <= B6 D[19:10] <= B7 D[9:0] <= B8	Positive Edge 3 Negaitive Edge 3 Positive Edge 4 Negaitive Edge 4	Q[9:0] <= B5 Q[9:0] <= B6 Q[9:0] <= B7 Q[9:0] <= B8

ONE WRITE TO EIGHT READ (1:8)

x40 DDR Input to x10 SDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
H	L	H	L	H

DDR Write Clock	x40 Data In	SDR Read Clock	x10 Data Out
Positive Edge 1	D[39:30] <= B1 D[29:20] <= B2 D[19:10] <= B3 D[9:0] <= B4	Positive Edge 1 Positive Edge 2 Positive Edge 3 Positive Edge 4	Q[9:0] <= B1 Q[9:0] <= B2 Q[9:0] <= B3 Q[9:0] <= B4
Negative Edge 1	D[39:30] <= B5 D[29:20] <= B6 D[19:10] <= B7 D[9:0] <= B8	Positive Edge 5 Positive Edge 6 Positive Edge 7 Positive Edge 8	Q[9:0] <= B5 Q[9:0] <= B6 Q[9:0] <= B7 Q[9:0] <= B8

TABLE 7 — BUS-MATCHING WRITE TO READ RATIO (CONTINUED)

TWO WRITE TO ONE READ (2:1)

x40 SDR Input to x40 DDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
L	H	L	L	L

SDR Write Clock	x40 Data In	DDR Read Clock	x40 Data Out
Positive Edge 1	D[39:0] <= LW1	Positive Edge 1	Q[39:0] <= LW1
Positive Edge 2	D[39:0] <= LW2	Negative Edge 1	Q[39:0] <= LW2

x20 DDR Input to x40 DDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
H	H	H	H	L

DDR Write Clock	x20 Data In	DDR Read Clock	x40 Data Out
Positive Edge 1	D[19:0] <= W1	Positive Edge 1	Q[39:20] <= W1
Negative Edge 1	D[19:0] <= W2		Q[19:0] <= W2
Positive Edge 2	D[19:0] <= W3	Negative Edge 1	Q[39:20] <= W3
Negative Edge 2	D[19:0] <= W4		Q[19:0] <= W4

x20 SDR Input to x40 SDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
L	L	H	H	L

SDR Write Clock	x20 Data In	SDR Read Clock	x40 Data Out
Positive Edge 1	D[19:0] <= W1	Positive Edge 1	Q[39:20] <= W1
Positive Edge 2	D[19:0] <= W2		Q[19:0] <= W2

x10 DDR Input to x40 SDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
H	L	H	H	H

DDR Write Clock	x10 Data In	SDR Read Clock	x40 Data Out
Positive Edge 1	D[9:0] <= B1	Positive Edge 1	Q[39:30] <= B1
Negative Edge 1	D[9:0] <= B2		Q[29:20] <= B2
Positive Edge 2	D[9:0] <= B3		Q[19:10] <= B3
Negative Edge 2	D[9:0] <= B4		Q[9:0] <= B4

FOUR WRITE TO ONE READ (4:1)

x20 SDR Input to x40 DDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
L	H	H	H	L

SDR Write Clock	x20 Data In	DDR Read Clock	x40 Data Out
Positive Edge 1	D[19:0] <= W1	Positive Edge 1	Q[39:20] <= W1
Positive Edge 2	D[19:0] <= W2		Q[19:0] <= W2
Positive Edge 3	D[19:0] <= W3	Negative Edge 1	Q[39:20] <= W3
Positive Edge 4	D[19:0] <= W4		Q[19:0] <= W4

x10 SDR Input to x40 SDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
L	L	H	H	H

SDR Write Clock	x10 Data In	SDR Read Clock	x40 Data Out
Positive Edge 1	D[9:0] <= B1	Positive Edge 1	Q[39:30] <= B1
Positive Edge 2	D[9:0] <= B2		Q[29:20] <= B2
Positive Edge 3	D[9:0] <= B3		Q[19:10] <= B3
Positive Edge 4	D[9:0] <= B4		Q[9:0] <= B4

x10 DDR Input to x40 DDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
H	H	H	H	H

DDR Write Clock	x10 Data In	DDR Read Clock	x40 Data Out
Positive Edge 1	D[9:0] <= B1	Positive Edge 1	Q[39:30] <= B1
Negative Edge 1	D[9:0] <= B2		Q[29:20] <= B2
Positive Edge 2	D[9:0] <= B3		Q[19:10] <= B3
Negative Edge 2	D[9:0] <= B4		Q[9:0] <= B4
Positive Edge 3	D[9:0] <= B5	Negative Edge 2	Q[39:30] <= B5
Negative Edge 3	D[9:0] <= B6		Q[29:20] <= B6
Positive Edge 4	D[9:0] <= B7		Q[19:10] <= B7
Negative Edge 4	D[9:0] <= B8		Q[9:0] <= B8

TABLE 7 — BUS-MATCHING WRITE TO READ RATIO (CONTINUED)

EIGHT WRITE TO ONE READ (8:1)

x10 SDR Input to x40 DDR Output

Configuration				
$\overline{WSDR}$	$\overline{RSDR}$	BM	IW	OW
L	H	H	H	H

SDR Write Clock	x10 Data In	DDR Read Clock	x40 Data Out
Positive Edge 1	D[9:0] <= B1	Positive Edge	Q[39:30] <= B1
Positive Edge 2	D[9:0] <= B2		Q[29:20] <= B2
Positive Edge 3	D[9:0] <= B3		Q[19:10] <= B3
Positive Edge 4	D[9:0] <= B4		Q[9:0] <= B4
Positive Edge 5	D[9:0] <= B5	Negative Edge	Q[39:30] <= B5
Positive Edge 6	D[9:0] <= B6		Q[29:20] <= B6
Positive Edge 7	D[9:0] <= B7		Q[19:10] <= B7
Positive Edge 8	D[9:0] <= B8		Q[9:0] <= B8

TABLE 8 — T_{SKEW} MEASUREMENT

Data Port Configuration	Status Flags	T_{SKEW} Measurement
DDR Input to DDR Output	$\overline{EF}$ & $\overline{PAE}$	Negative Edge WCLK to Positive Edge RCLK
	$\overline{FF}$ & $\overline{PAF}$	Negative Edge RCLK to Positive Edge WCLK
DDR Input to SDR Output	$\overline{EF}$ & $\overline{PAE}$	Negative Edge WCLK to Positive Edge RCLK
	$\overline{FF}$ & $\overline{PAF}$	Positive Edge RCLK to Positive Edge WCLK
SDR Input to DDR Output	$\overline{EF}$ & $\overline{PAE}$	Positive Edge WCLK to Positive Edge RCLK
	$\overline{FF}$ & $\overline{PAF}$	Negative Edge RCLK to Positive Edge WCLK
SDR Input to SDR Output	$\overline{EF}$ & $\overline{PAE}$	Positive Edge WCLK to Positive Edge RCLK
	$\overline{FF}$ & $\overline{PAF}$	Positive Edge RCLK to Positive Edge WCLK

JTAG TIMING SPECIFICATION

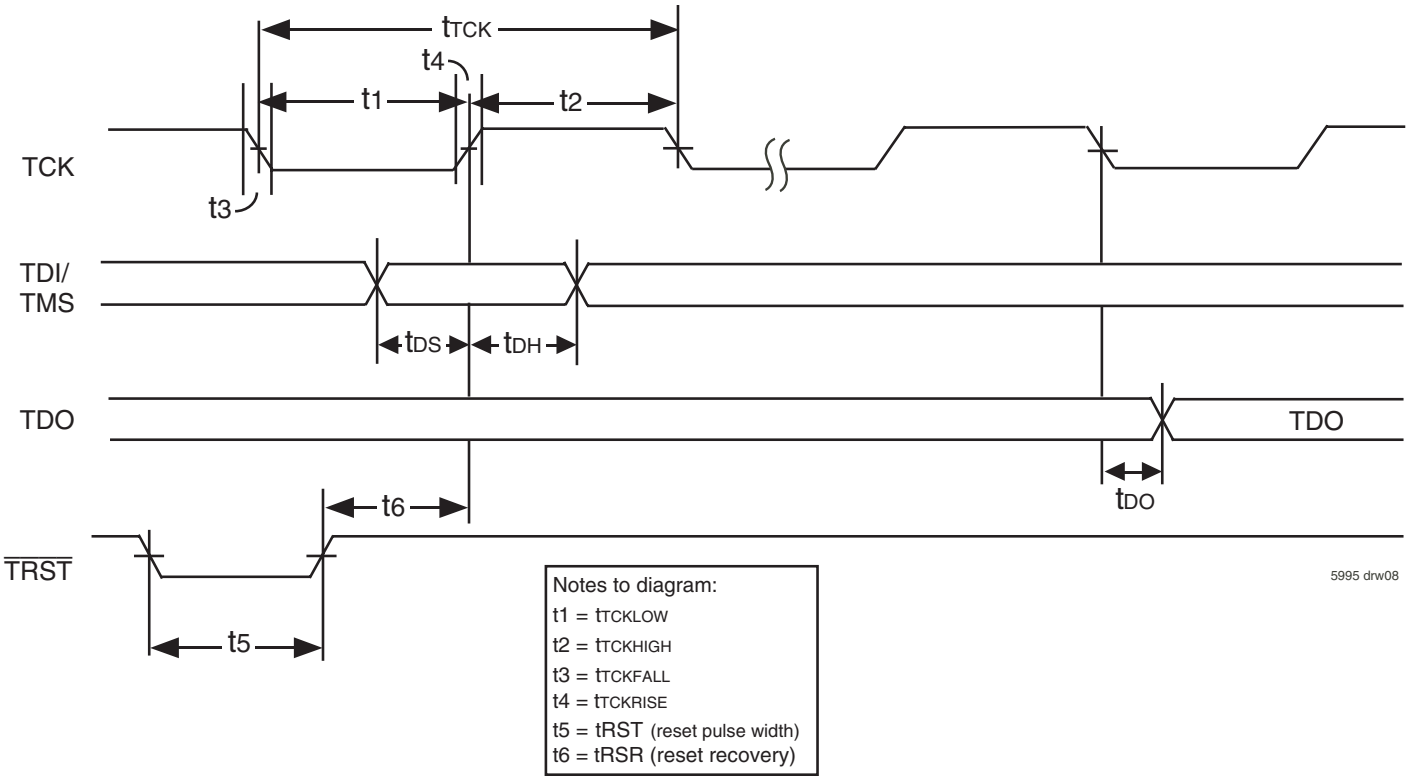


Figure 5. Standard JTAG Timing

SYSTEM INTERFACE PARAMETERS

Parameter	Symbol	Test Conditions	IDT72T4088 IDT72T4098 IDT72T40108 IDT72T40118		
			Min.	Max.	Units
Data Output	t_{DO}[1]		-	20	ns
Data Output Hold	t_{DOH}[1]		0	-	ns
Data Input	t_{DS}	trise=3ns	10	-	ns
	t_{DH}	tfall=3ns	10	-	

NOTE:
1. 50pf loading on external output signals.

JTAG AC ELECTRICAL CHARACTERISTICS

(Vcc = 2.5V ± 5%; Tcase = 0°C to +85°C)

Parameter	Symbol	Test Conditions			
			Min.	Max.	Units
JTAG Clock Input Period	t_{TCK}	-	100	-	ns
JTAG Clock HIGH	$t_{TCKHIGH}$	-	40	-	ns
JTAG Clock Low	t_{TCKLOW}	-	40	-	ns
JTAG Clock Rise Time	$t_{TCKRISE}$	-	-	5[1]	ns
JTAG Clock Fall Time	$t_{TCKFALL}$	-	-	5[1]	ns
JTAG Reset	t_{RST}	-	50	-	ns
JTAG Reset Recovery	t_{RSR}	-	50	-	ns

NOTE:
1. Guaranteed by design.

JTAG INTERFACE

Five additional pins (TDI, TDO, TMS, TCK and $\overline{TRST}$) are provided to support the JTAG boundary scan interface. The IDT72T4088/72T4098/72T40108/72T40118 incorporates the necessary tap controller and modified pad cells to implement the JTAG facility.

Note that IDT provides appropriate Boundary Scan Description Language program files for these devices.

The Standard JTAG interface consists of four basic elements:

- *Test Access Port (TAP)*
- *TAP controller*
- *Instruction Register (IR)*
- *Data Register Port (DR)*

The following sections provide a brief description of each element. For a complete description refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

The Figure below shows the standard Boundary-Scan Architecture

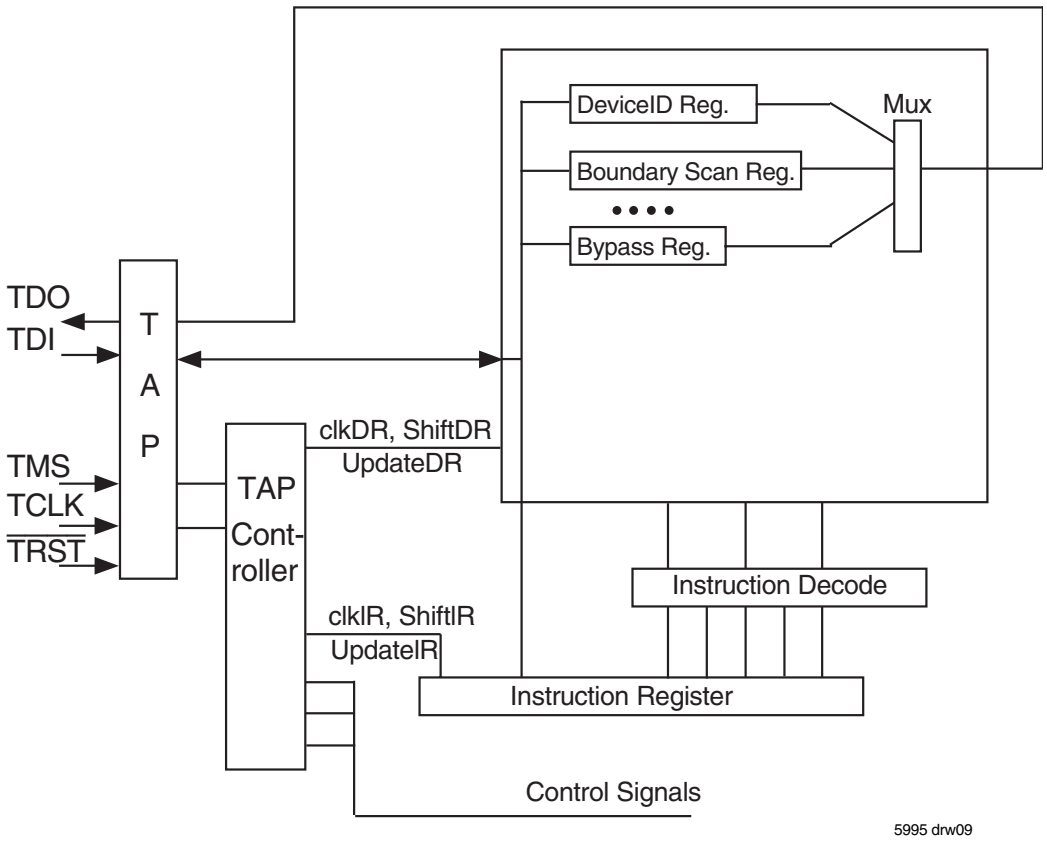


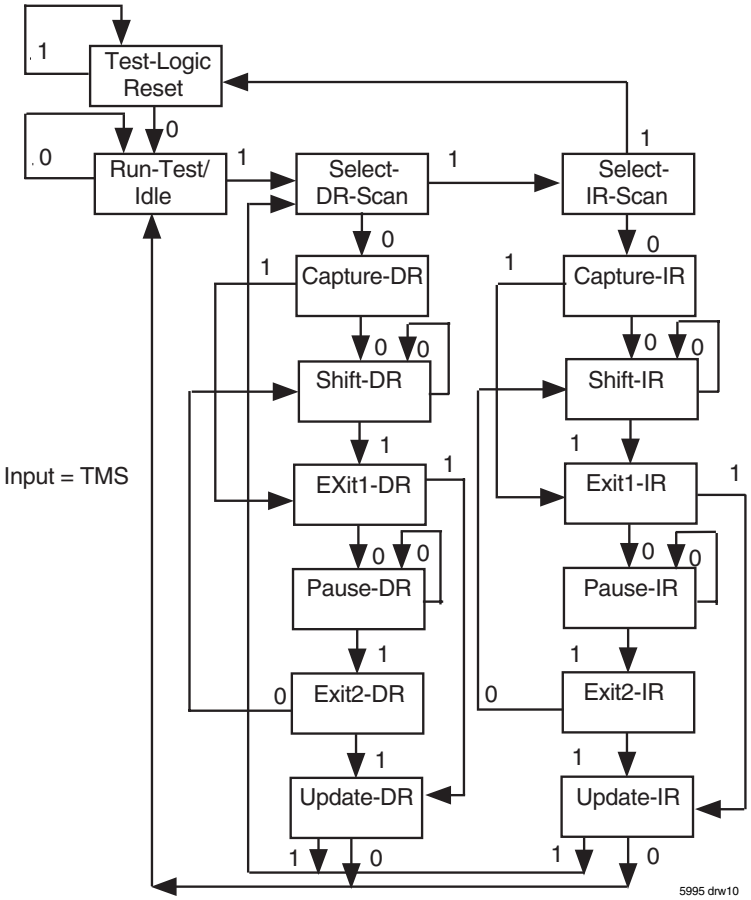
Figure 6. Boundary Scan Architecture

TEST ACCESS PORT (TAP)

The Tap interface is a general-purpose port that provides access to the internal of the processor. It consists of four input ports (TCLK, TMS, TDI, $\overline{TRST}$) and one output port (TDO).

THE TAP CONTROLLER

The Tap controller is a synchronous finite state machine that responds to TMS and TCLK signals to generate clock and control signals to the Instruction and Data Registers for capture and update of data.



NOTES:
1. Five consecutive TCK cycles with TMS = 1 will reset the TAP.
2. TAP controller does not automatically reset upon power-up. The user must provide a reset to the TAP controller (either by $\overline{TRST}$ or TMS).
3. TAP controller must be reset before normal FIFO operations can begin.

Figure 7. TAP Controller State Diagram

Refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1) for the full state diagram

All state transitions within the TAP controller occur at the rising edge of the TCLK pulse. The TMS signal level (0 or 1) determines the state progression that occurs on each TCLK rising edge. The TAP controller takes precedence over the FIFO memory and must be reset after power up of the device. See $\overline{TRST}$ description for more details on TAP controller reset.

Test-Logic-Reset All test logic is disabled in this controller state enabling the normal operation of the IC. The TAP controller state machine is designed in such a way that, no matter what the initial state of the controller is, the Test-Logic-Reset state can be entered by holding TMS at high and pulsing TCK five times. This is the reason why the Test Reset (TRST) pin is optional.

Run-Test-Idle In this controller state, the test logic in the IC is active only if certain instructions are present. For example, if an instruction activates the self test, then it will be executed when the controller enters this state. The test logic in the IC is idles otherwise.

Select-DR-Scan This is a controller state where the decision to enter the Data Path or the Select-IR-Scan state is made.

Select-IR-Scan This is a controller state where the decision to enter the Instruction Path is made. The Controller can return to the Test-Logic-Reset state other wise.

Capture-IR In this controller state, the shift register bank in the Instruction Register parallel loads a pattern of fixed values on the rising edge of TCK. The last two significant bits are always required to be "01".

Shift-IR In this controller state, the instruction register gets connected between TDI and TDO, and the captured pattern gets shifted on each rising edge of TCK. The instruction available on the TDI pin is also shifted in to the instruction register.

Exit1-IR This is a controller state where a decision to enter either the Pause-IR state or Update-IR state is made.

Pause-IR This state is provided in order to allow the shifting of instruction register to be temporarily halted.

Exit2-DR This is a controller state where a decision to enter either the Shift-IR state or Update-IR state is made.

Update-IR In this controller state, the instruction in the instruction register is latched in to the latch bank of the Instruction Register on every falling edge of TCK. This instruction also becomes the current instruction once it is latched.

Capture-DR In this controller state, the data is parallel loaded in to the data registers selected by the current instruction on the rising edge of TCK.

Shift-DR, Exit1-DR, Pause-DR, Exit2-DR and Update-DR These controller states are similar to the Shift-IR, Exit1-IR, Pause-IR, Exit2-IR and Update-IR states in the Instruction path.

THE INSTRUCTION REGISTER

The Instruction register allows an instruction to be shifted in serially into the processor at the rising edge of TCLK.

The Instruction is used to select the test to be performed, or the test data register to be accessed, or both. The instruction shifted into the register is latched at the completion of the shifting process when the TAP controller is at Update-IR state.

The instruction register must contain 4 bit instruction register-based cells which can hold instruction data. These mandatory cells are located nearest the serial outputs they are the least significant bits.

TEST DATA REGISTER

The Test Data register contains three test data registers: the Bypass, the Boundary Scan register and Device ID register.

These registers are connected in parallel between a common serial input and a common serial data output.

The following sections provide a brief description of each element. For a complete description, refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

TEST BYPASS REGISTER

The register is used to allow test data to flow through the device from TDI to TDO. It contains a single stage shift register for a minimum length in serial path. When the bypass register is selected by an instruction, the shift register stage is set to a logic zero on the rising edge of TCLK when the TAP controller is in the Capture-DR state.

The operation of the bypass register should not have any effect on the operation of the device in response to the BYPASS instruction.

THE BOUNDARY-SCAN REGISTER

The Boundary Scan Register allows serial data TDI be loaded in to or read out of the processor input/output ports. The Boundary Scan Register is a part of the IEEE 1149.1-1990 Standard JTAG Implementation.

THE DEVICE IDENTIFICATION REGISTER

The Device Identification Register is a Read Only 32-bit register used to specify the manufacturer, part number and version of the processor to be determined through the TAP in response to the IDCODE instruction.

IDT JEDEC ID number is 0xB3. This translates to 0x33 when the parity is dropped in the 11-bit Manufacturer ID field.

For the IDT72T4088/72T4098/72T40108/72T40118, the Part Number field contains the following values:

Device	Part# Field
IDT72T4088	04A3
IDT72T4098	04A2
IDT72T40108	04A1
IDT72T40118	04A0

31(MSB) 28	27 12	11 1	0(LSB)
Version (4 bits) 0X0	Part Number (16-bit)	Manufacturer ID (11-bit) 0X33	1

IDT72T4088/4098/40108/40118 JTAG Device Identification Register

JTAG INSTRUCTION REGISTER

The Instruction register allows instruction to be serially input into the device when the TAP controller is in the Shift-IR state. The instruction is decoded to perform the following:

- Select test data registers that may operate while the instruction is current. The other test data registers should not interfere with chip operation and the selected data register.
- Define the serial test data register path that is used to shift data between TDI and TDO during data register scanning.

The Instruction Register is a 4 bit field (i.e.IR3, IR2, IR1, IR0) to decode 16 different possible instructions. Instructions are decoded as follows.

Hex Value	Instruction	Function
0x02	IDCODE	Select Chip Identification data register
0x01	SAMPLE/PRELOAD	Select Boundary Scan Register
0x03	HI-IMPEDANCE	JTAG
0x0F	BYPASS	Select Bypass Register

Table 8. JTAG Instruction Register Decoding

The following sections provide a brief description of each instruction. For a complete description refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

IDCODE

The optional IDCODE instruction allows the IC to remain in its functional mode and selects the optional device identification register to be connected between TDI and TDO. The device identification register is a 32-bit shift register containing information regarding the IC manufacturer, device type, and version code. Accessing the device identification register does not interfere with the operation of the IC. Also, access to the device identification register should be immediately available, via a TAP data-scan operation, after power-up of the IC or after the TAP has been reset using the optional $\overline{TRST}$ pin or by otherwise moving to the Test-Logic-Reset state.

SAMPLE/PRELOAD

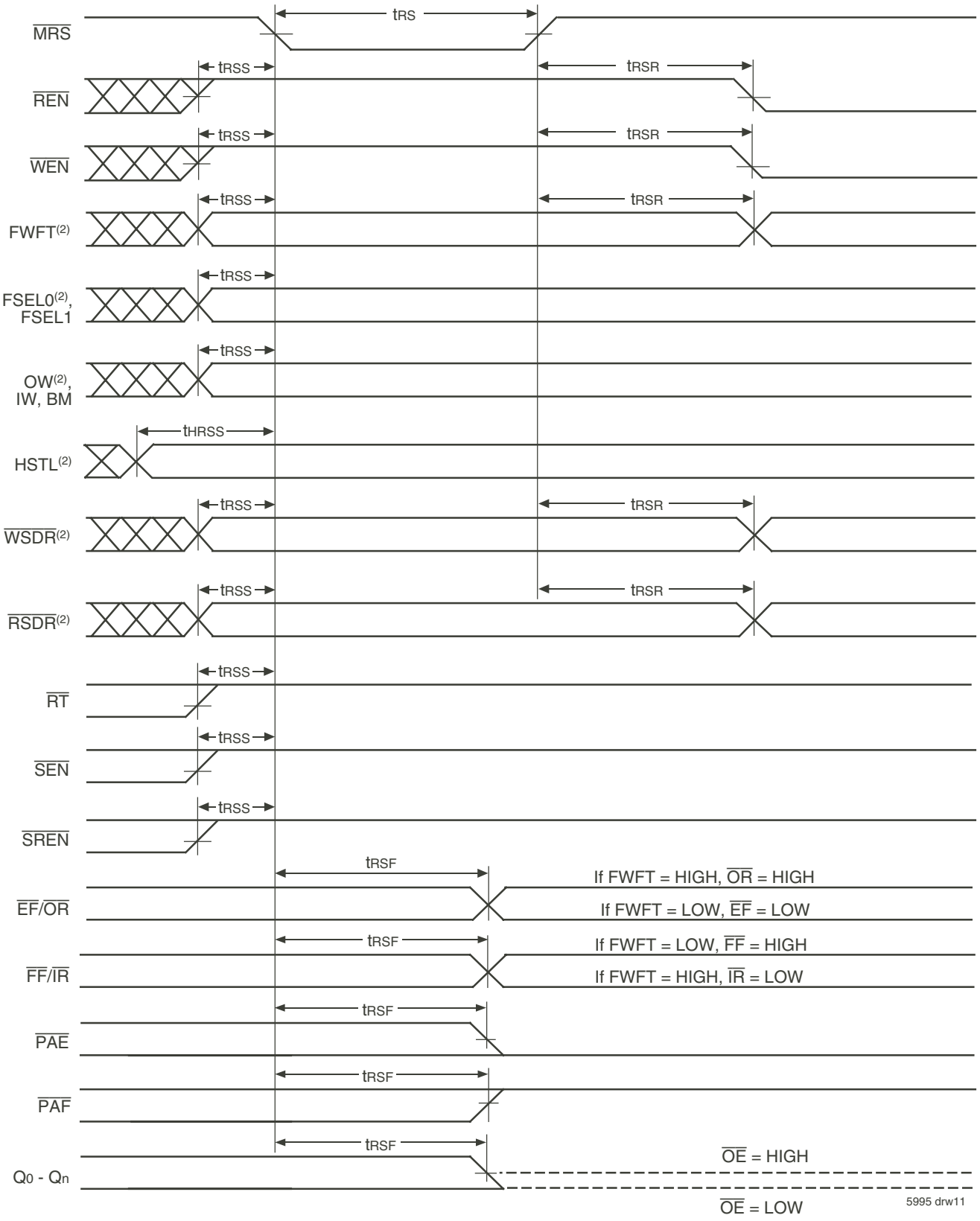
The required SAMPLE/PRELOAD instruction allows the IC to remain in a normal functional mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register can be accessed via a date scan operation, to take a sample of the functional data entering and leaving the IC.

HIGH-IMPEDANCE

The optional High-Impedance instruction sets all outputs (including two-state as well as three-state types) of an IC to a disabled (high-impedance) state and selects the one-bit bypass register to be connected between TDI and TDO. During this instruction, data can be shifted through the bypass register from TDI to TDO without affecting the condition of the IC outputs.

BYPASS

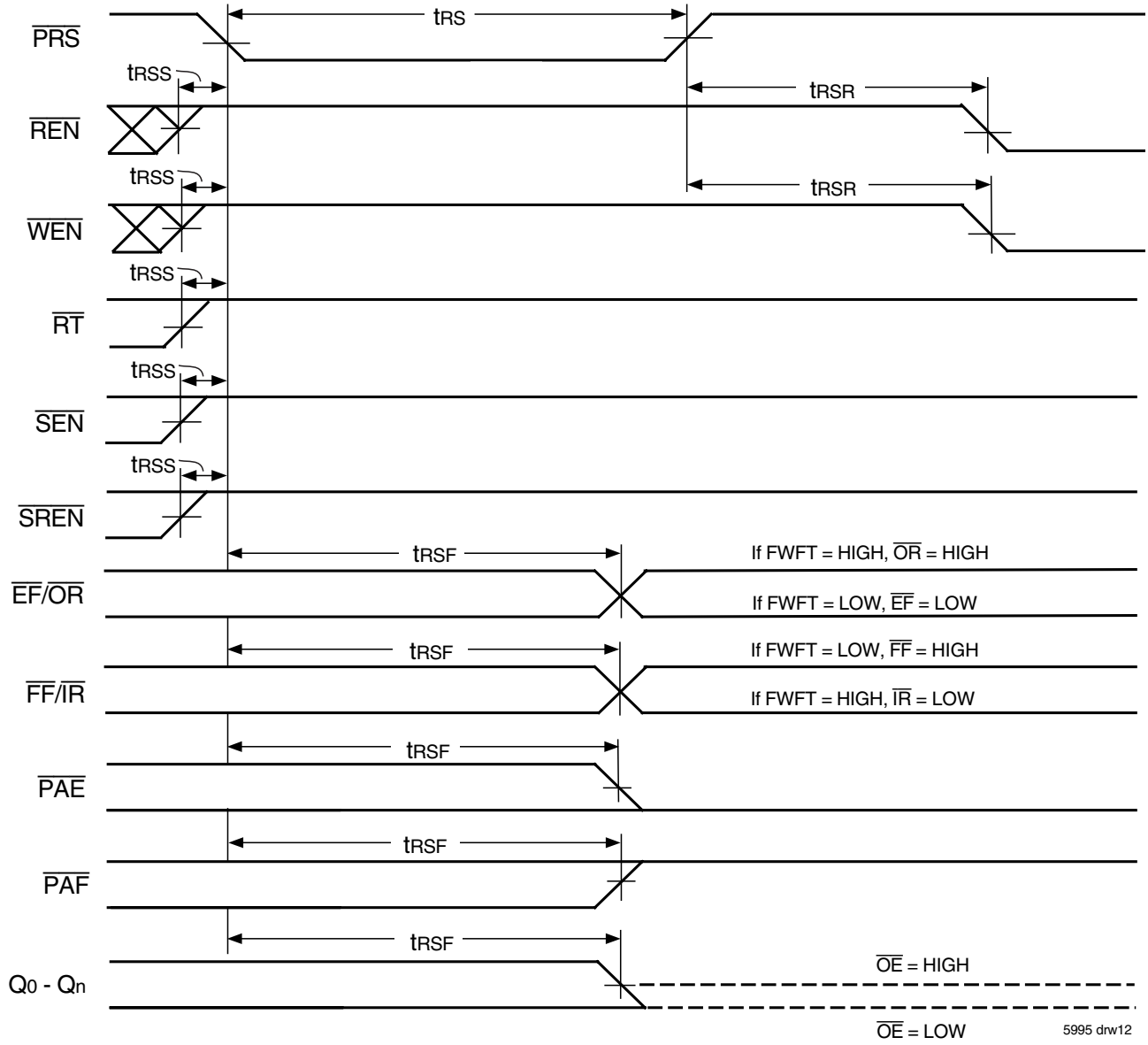
The required BYPASS instruction allows the IC to remain in a normal functional mode and selects the one-bit bypass register to be connected between TDI and TDO. The BYPASS instruction allows serial data to be transferred through the IC from TDI to TDO without affecting the operation of the IC.



NOTES:

1. During Master Reset the High-Impedance control of the Qn data outputs is provided by $\overline{OE}$ only, $\overline{RCS}$ can be HIGH or LOW until the first rising edge of RCLK after Master Reset is complete.
2. The status of these pins are latched in when the Master Reset pulse is LOW.

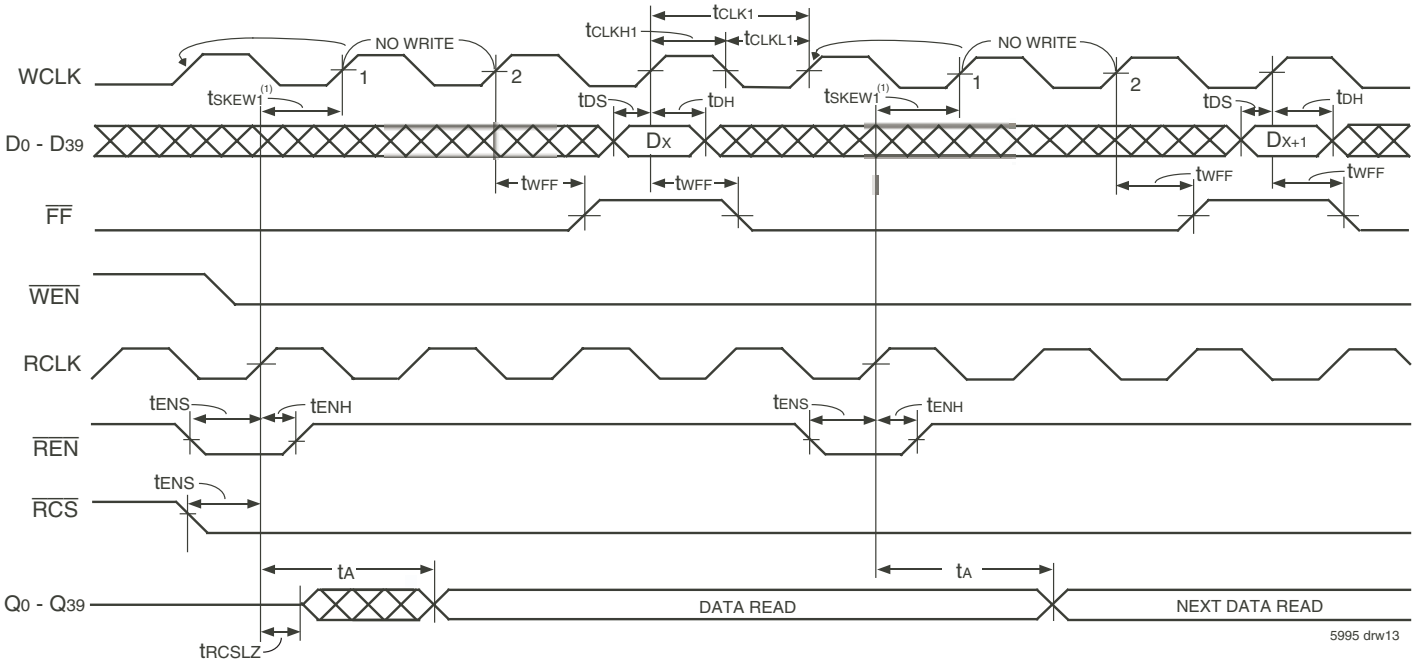
Figure 8. Master Reset Timing



NOTE:

1. During Partial Reset the High-Impedance control of the Qn data outputs is provided by $\overline{OE}$ only, $\overline{RCS}$ can be HIGH or LOW until the first rising edge of RCLK after Master Reset is complete.

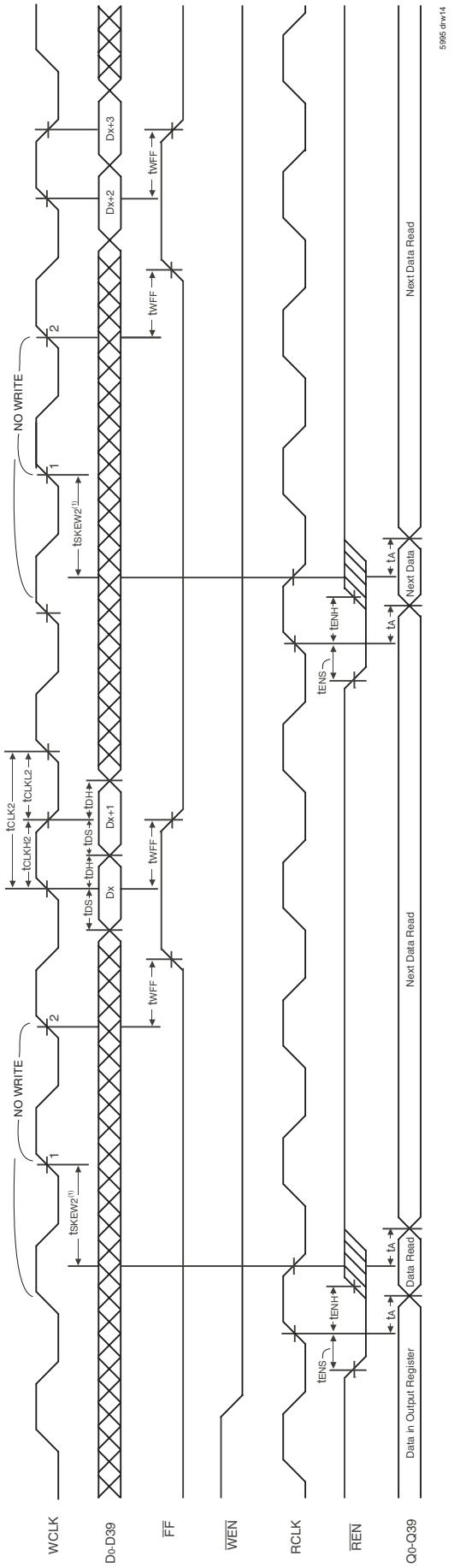
Figure 9. Partial Reset Timing



NOTES:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH (after one WCLK cycle plus t_{WFF}). If the time between the rising edge of the RCLK and the rising edge of the WCLK is less than t_{SKEW1}, then the $\overline{FF}$ deassertion may be delayed one extra WCLK cycle.
2. $\overline{OE}$ = LOW, $\overline{EF}$ = HIGH.
3. $\overline{WCS}$ = LOW.
4. WCLK must be free running for $\overline{FF}$ to update.

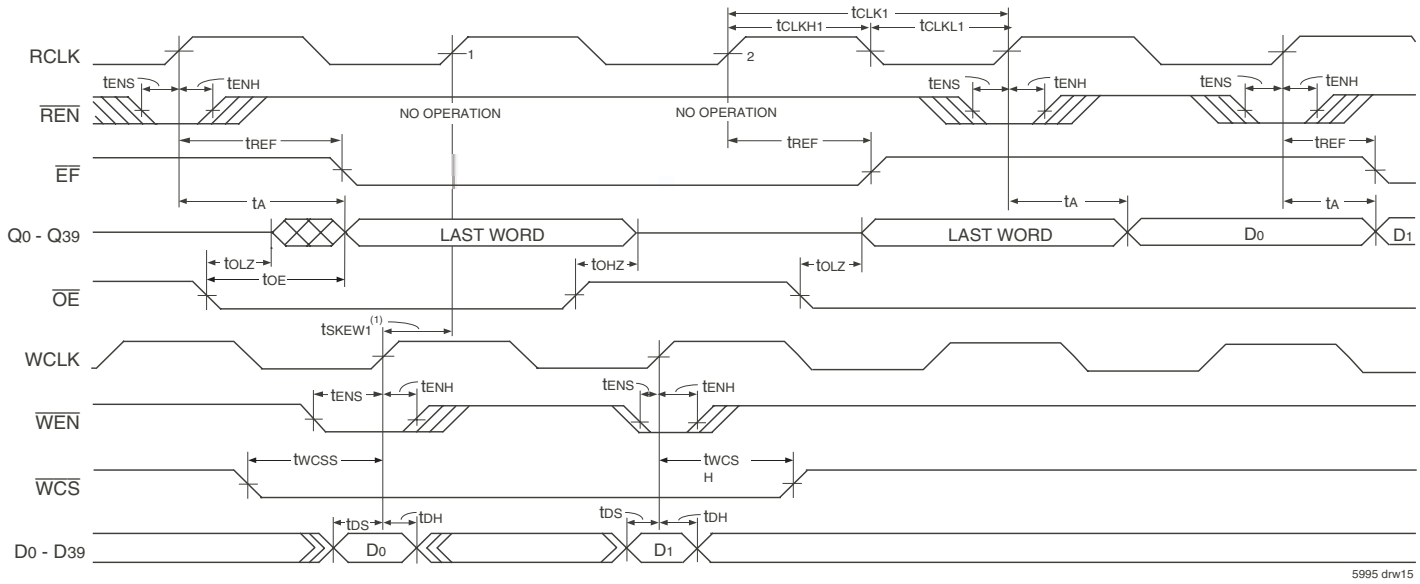
Figure 10. Write Cycle and Full Flag Timing (IDT Standard Mode)



NOTES:

1. t_{SKEW2} is the minimum time between a falling RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH (after one WCLK cycle plus t_{WFF}). If the time between the falling edge of the RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{FF}$ deassertion may be delayed one extra WCLK cycle.
2. $\overline{OE}$ = LOW, $\overline{EF}$ = HIGH.
3. $\overline{WCS}$ = LOW, $\overline{RCS}$ = LOW, $\overline{WSDR}$ = HIGH and $\overline{RSDR}$ = HIGH.
4. WCLK must be free running for $\overline{FF}$ to update.

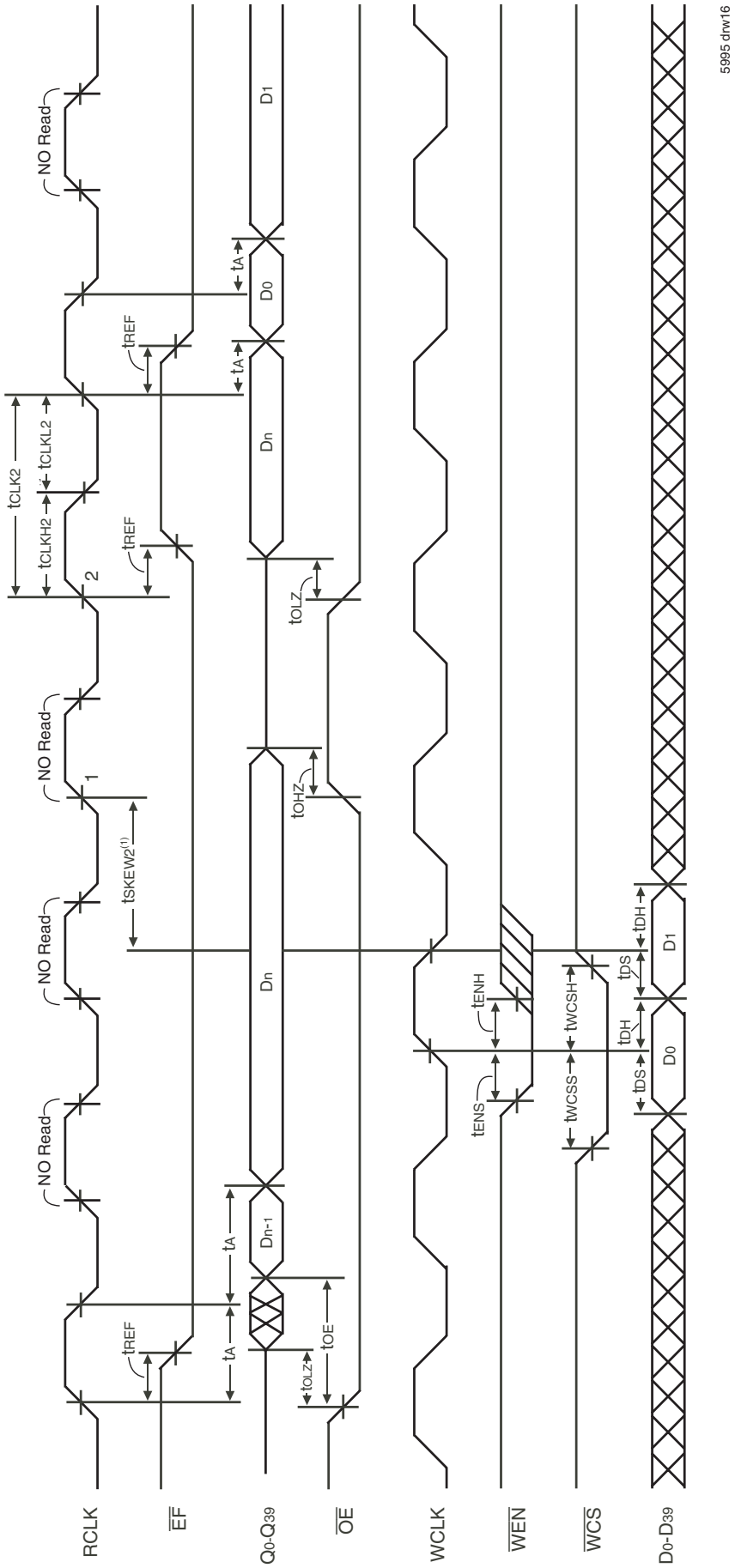
Figure 11. Write Cycle and Full Flag Timing in Double Data Rate Mode (IDT Standard Mode)



NOTES:

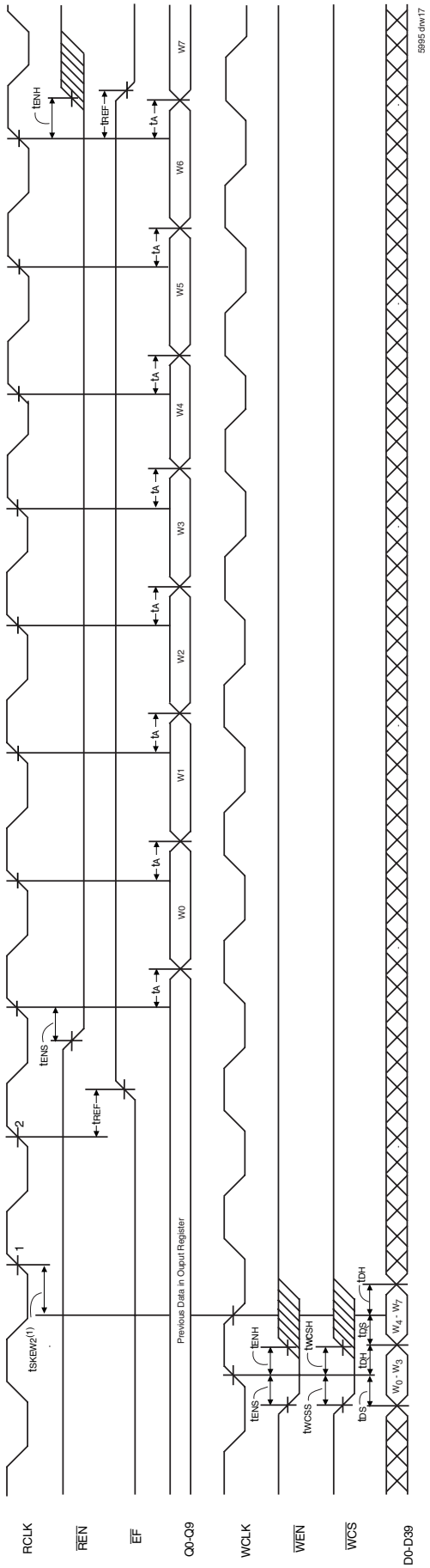
1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH (after one RCLK cycle plus t_{REF}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then $\overline{EF}$ deassertion may be delayed one extra RCLK cycle.
2. First data word latency = t_{SKEW1} + 1*T_{RCLK} + t_{REF}.
3. $\overline{RCS}$ is LOW.
4. RCLK must be free running for $\overline{EF}$ to update.

Figure 12. Read Cycle, Output Enable, Empty Flag and First Data Word Latency (IDT Standard Mode)



NOTES:
1. t_{SKEW2} is the minimum time between a falling WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH (after one RCLK cycle plus t_{REF}). If the time between the falling edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ deassertion may be delayed one extra RCLK cycle.
2. $\overline{REN}$ = LOW.
3. First data word latency = t_{SKEW1} + 1*t_{RCLK} + t_{REF}.
4. $\overline{RCS}$ = LOW, $\overline{WSDR}$ = HIGH and $\overline{RSDR}$ = HIGH.
5. RCLK must be free running for $\overline{EF}$ to update.

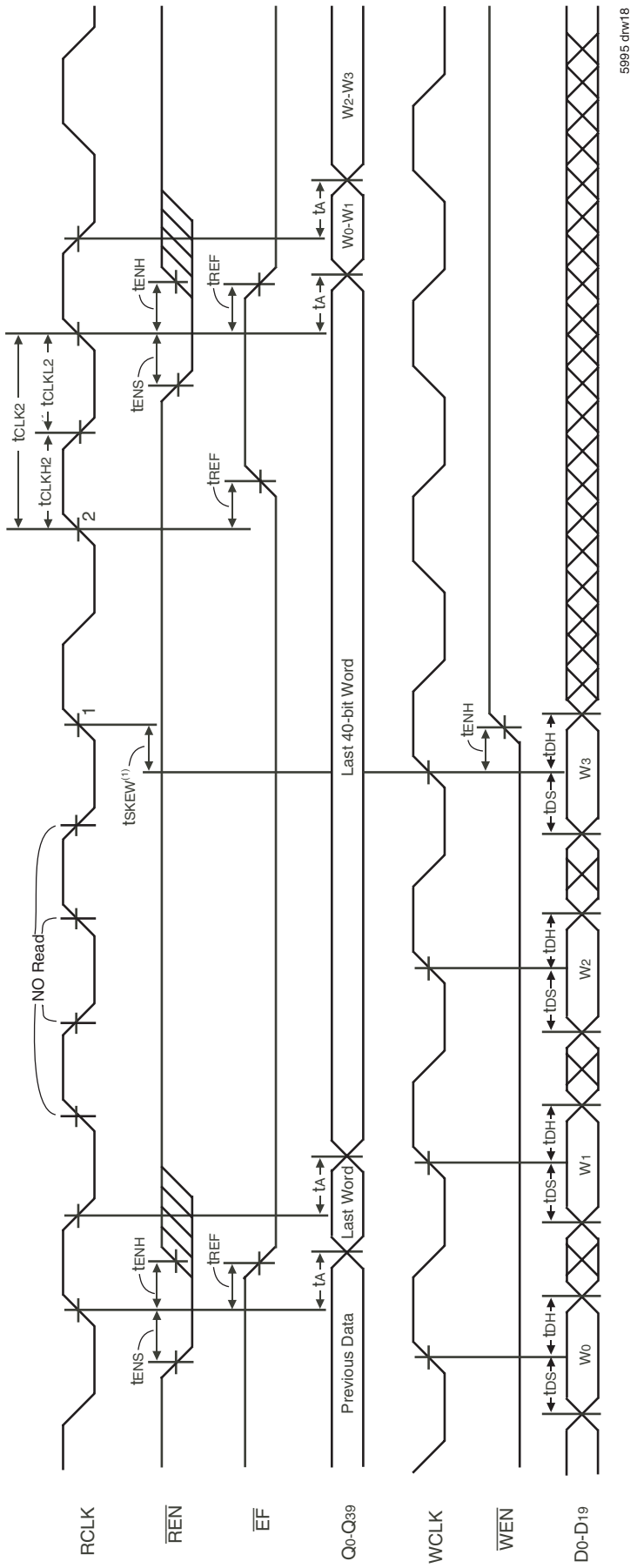
Figure 13. Read Cycle, Output Enable, Empty Flag and First Data Word Latency in Double Data Rate Mode (IDT Standard Mode)



NOTES:

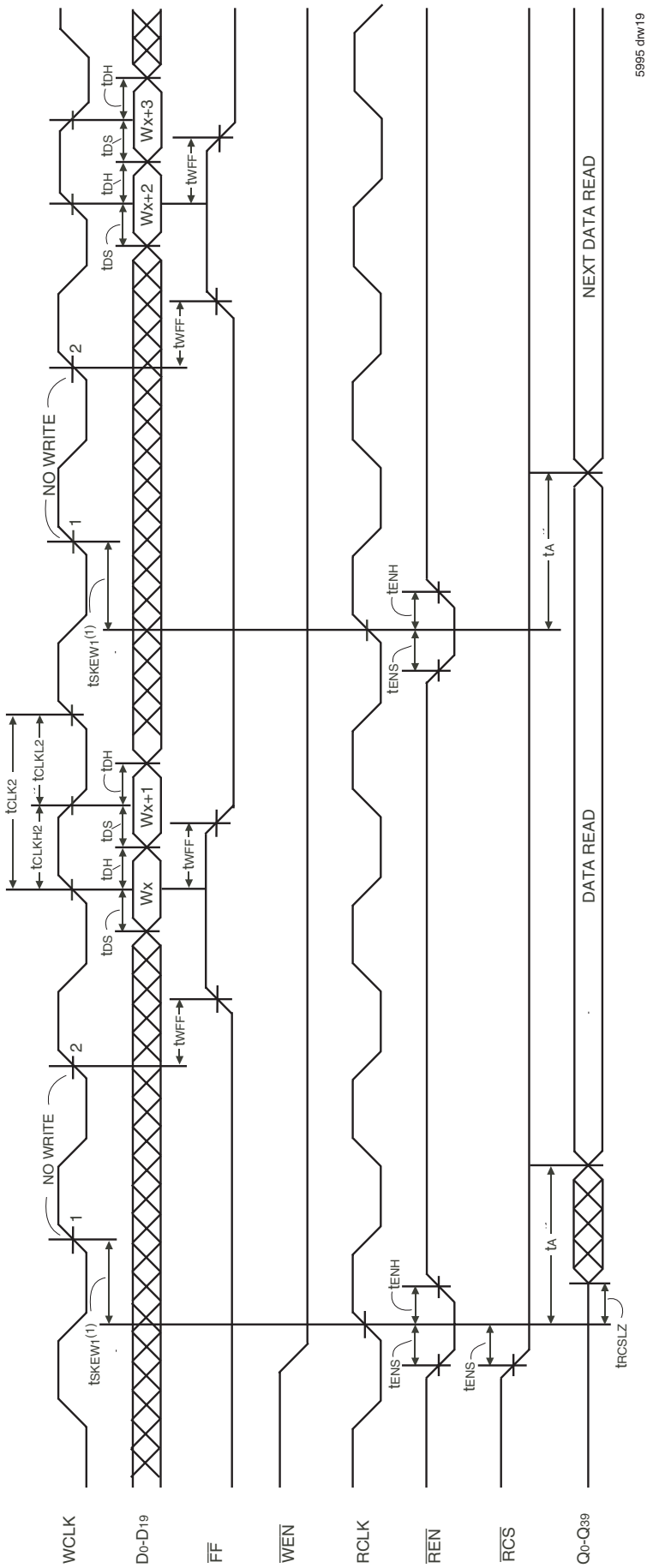
1. t_{SKEW2} is the minimum time between a falling WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH (after one RCLK cycle plus t_{REF}). If the time between the falling edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ deassertion may be delayed one extra RCLK cycle.
2. $\overline{REN}$ = LOW.
3. First data word latency = t_{SKEW1} + 1*t_{RCLK} + t_{REF}.
4. $\overline{RCS}$ = LOW, $\overline{WSDR}$ = HIGH and $\overline{RSDR}$ = HIGH.
5. RCLK must be free running for $\overline{EF}$ to update.

Figure 14. Read Cycle, Empty Flag and First Data Word Latency in x40DDR to x10SDR with Bus-Matching and Rate-Matching (IDT Standard Mode)



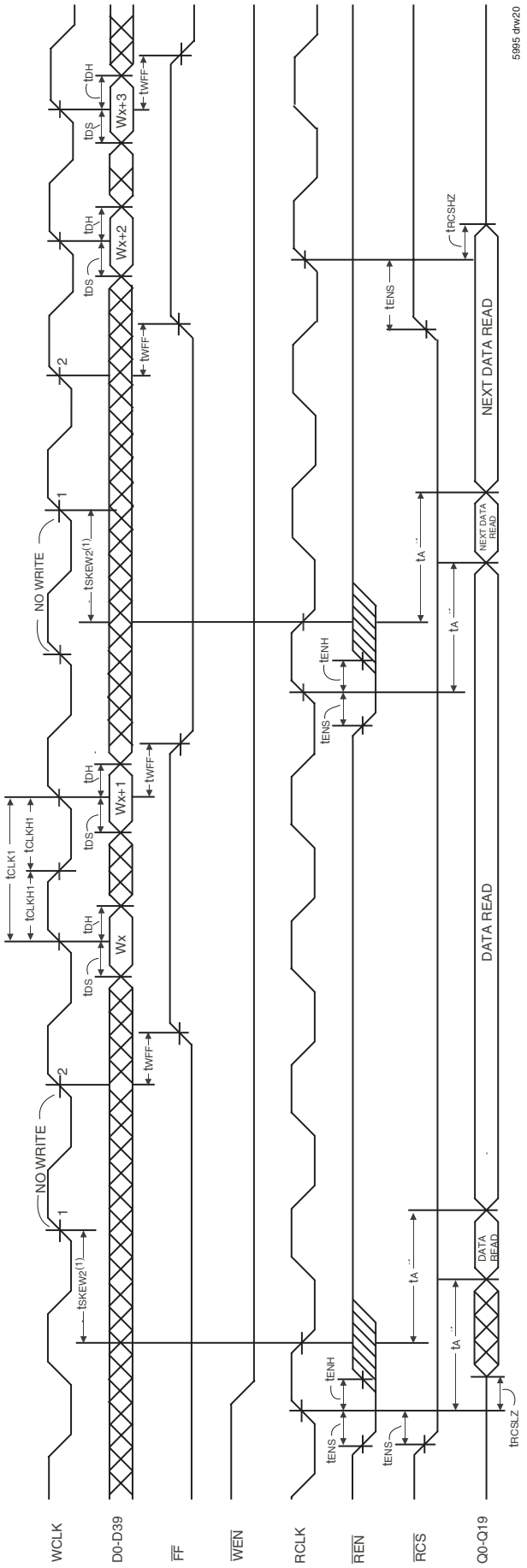
NOTES:
1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH (after one RCLK cycle plus t_{REF}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then $\overline{EF}$ deassertion may be delayed one extra RCLK cycle.
2. $\overline{OE}$ = LOW.
3. First data word latency = t_{SKEW1} + 1*t_{RCLK} + t_{REF}.
4. $\overline{RCS}$ = LOW, $\overline{WCS}$ = LOW, $\overline{WSDR}$ = LOW and $\overline{RSDR}$ = HIGH.
5. RCLK must be free running for $\overline{EF}$ to update.

Figure 15. Read Cycle and Empty Flag in x20SDR to x40DDR with Bus-Matching and Rate-Matching (IDT Standard Mode)



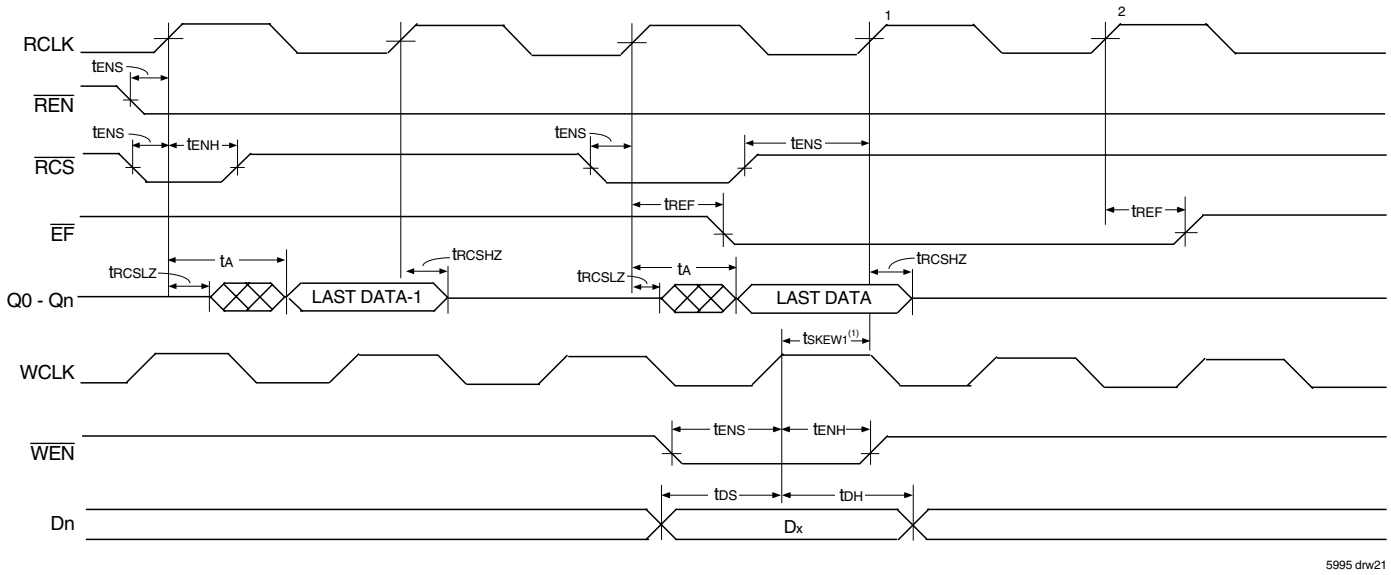
NOTES:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH (after one WCLK cycle plus t_{WFF}). If the time between the rising edge of the RCLK and the rising edge of the WCLK is less than t_{SKEW1}, then the $\overline{FF}$ deassertion may be delayed one extra WCLK cycle.
2. $\overline{LD}$ = HIGH, $\overline{OE}$ = LOW, $\overline{EF}$ = HIGH.
3. $\overline{WCS}$ = LOW.
4. WCLK must be free running for $\overline{FF}$ to update.

Figure 16. Write Cycle and Full Flag Timing in x20DDR to x40SDR with Bus-Matching and Rate-Matching (IDT Standard Mode)



NOTES:
1. t_{SKEW2} is the minimum time between a falling RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH (after one WCLK cycle plus t_{WFF}). If the time between the falling edge of the RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{FF}$ deassertion may be delayed one extra WCLK cycle.
2. $\overline{OE}$ = LOW, $\overline{EF}$ = HIGH.
3. $\overline{WCS}$ = LOW, $\overline{RCS}$ = LOW, $\overline{WSDR}$ = HIGH and $\overline{RSDR}$ = HIGH.
4. WCLK must be free running for $\overline{FF}$ to update.

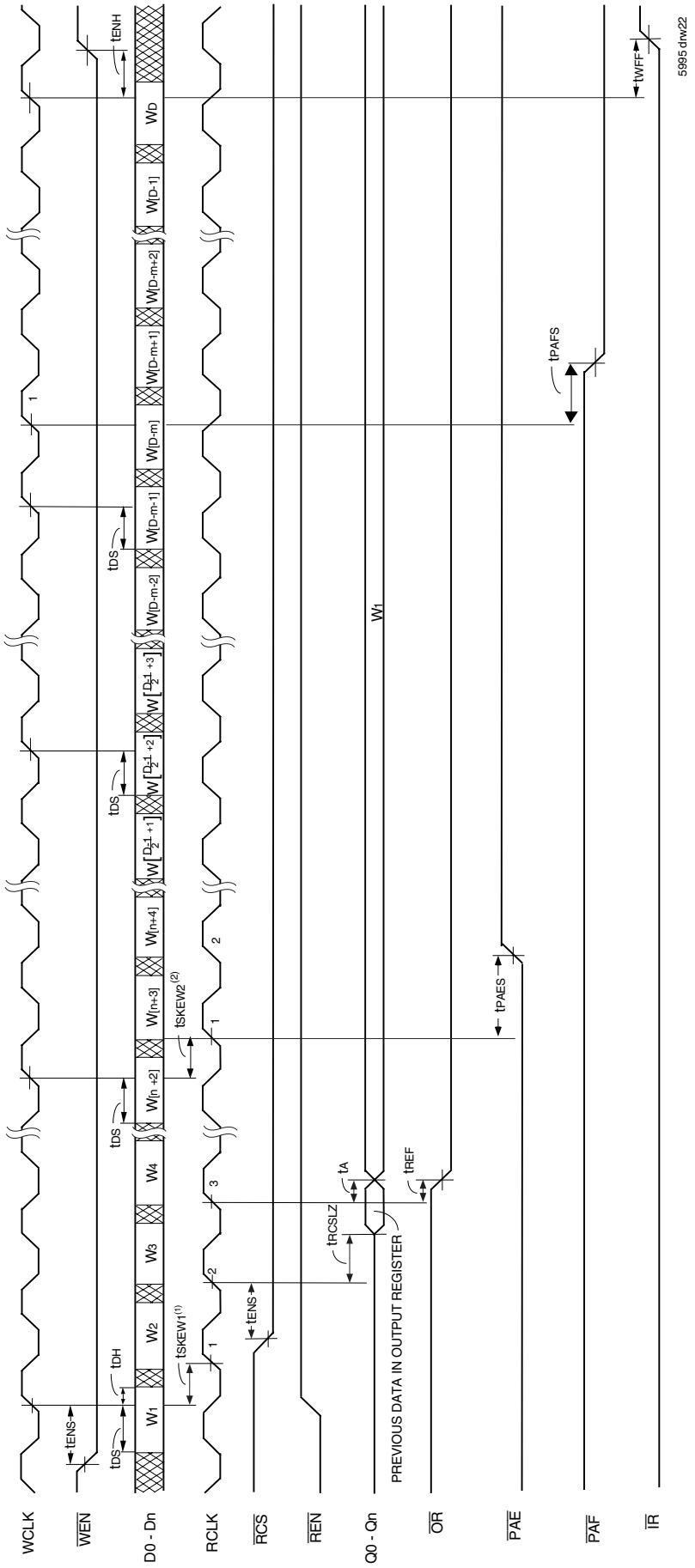
Figure 17. Write Cycle and Full Flag in x40SDR to x20DDR with Bus-Matching and Rate-Matching (IDT Standard Mode)



NOTES:

1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH (after one RCLK cycle plus t_{REF}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then $\overline{EF}$ deassertion may be delayed one extra RCLK cycle.
2. First data word latency = t_{SKEW1} + 1*T_{RCLK} + t_{REF}.
3. $\overline{OE}$ is LOW.
4. RCLK must be free running for $\overline{EF}$ to update.

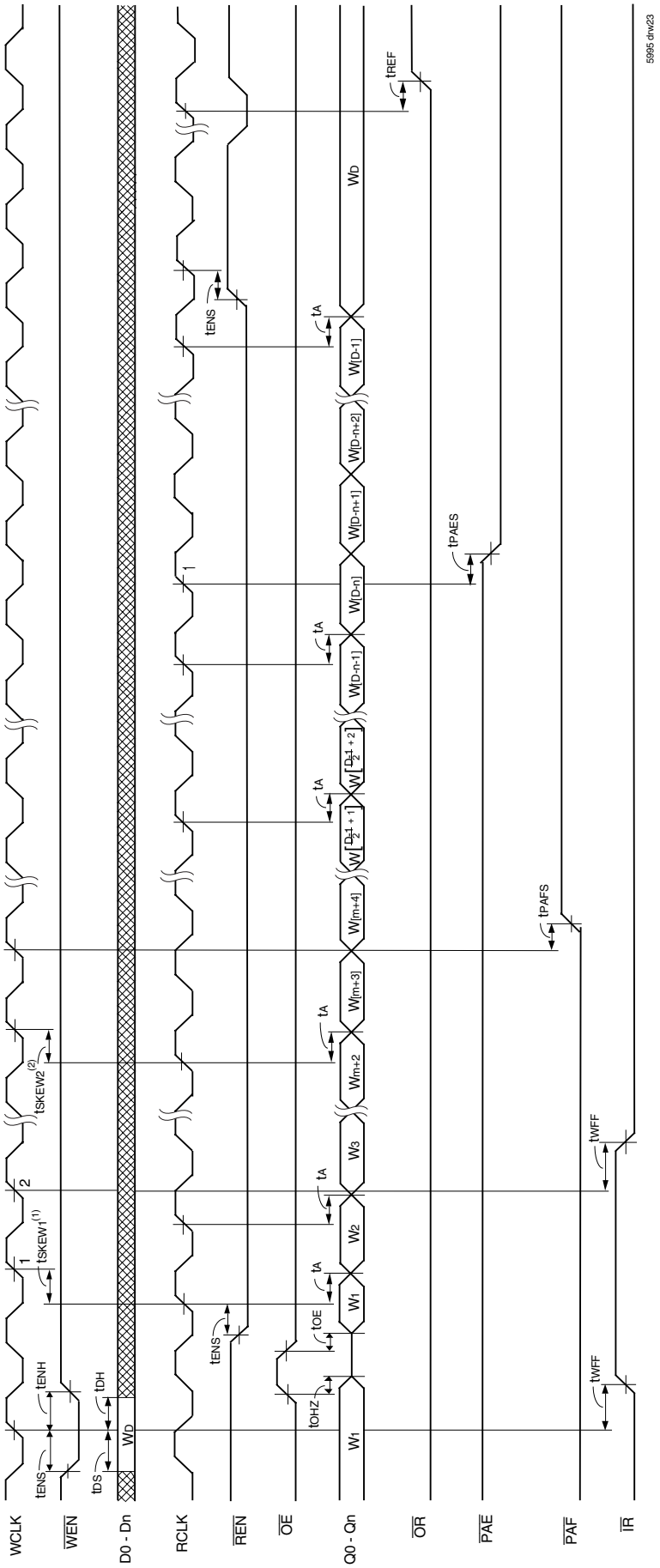
Figure 18. Read Cycle and Read Chip Select (IDT Standard Mode)



NOTES:

1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{OR}$ will go LOW after two RCLK cycles plus t_{REF}. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then $\overline{OR}$ assertion may be delayed one extra RCLK cycle.
2. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{PAE}$ will go HIGH after one RCLK cycle plus t_{PAES}. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then the $\overline{PAE}$ deassertion may be delayed one extra RCLK cycle.
3. $\overline{OE}$ = LOW
4. n = $\overline{PAE}$ offset, m = $\overline{PAF}$ offset and D = maximum FIFO depth.
5. D = 16,385 for IDT72T4088, 32,769 for IDT72T4098, 65,537 for IDT72T40108, 131,073 for IDT72T40118.
6. First data word latency = $t_{SKEW1} + 2*T_{RCLK} + t_{REF}$.

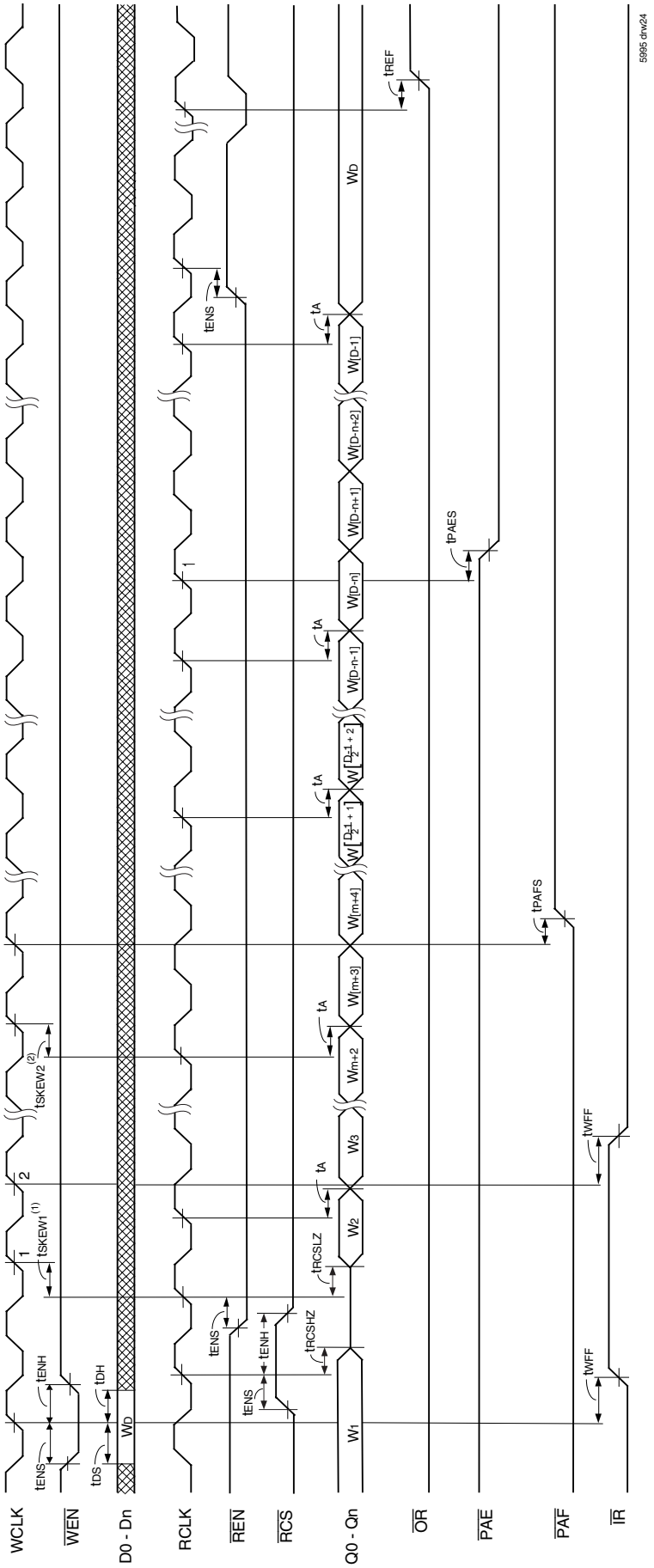
Figure 19. Write Timing (FWFT Mode)



NOTES:

1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{OR}$ will go LOW after two RCLK cycles plus t_{REF}. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then $\overline{OR}$ assertion may be delayed one extra RCLK cycle.
2. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{PAE}$ will go HIGH after one RCLK cycle plus t_{PAES}. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then the $\overline{PAE}$ deassertion may be delayed one extra RCLK cycle.
3. $\overline{OE}$ = LOW
4. n = $\overline{PAE}$ offset, m = $\overline{PAF}$ offset and D = maximum FIFO depth.
5. D = 16,385 for IDT72T4088, 32,769 for IDT72T4098, 65,537 for IDT72T40108, 131,073 for IDT72T40118.
6. First data word latency = t_{SKEW1} + 2*T_{RCLK} + t_{REF}.

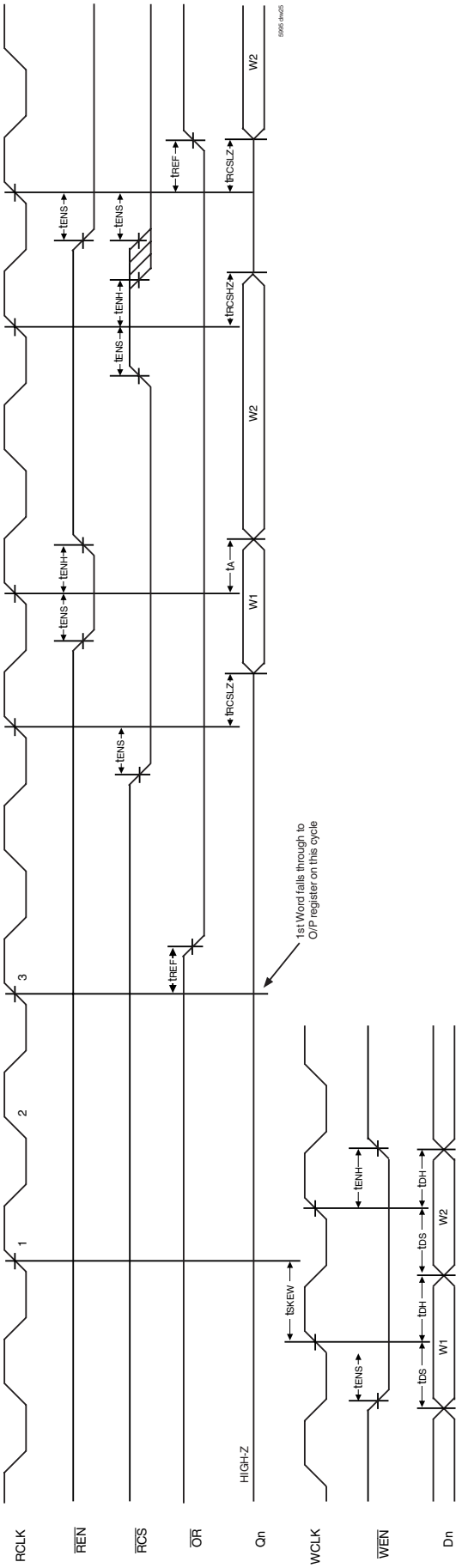
Figure 20. Read Timing (FWFT Mode)



NOTES:

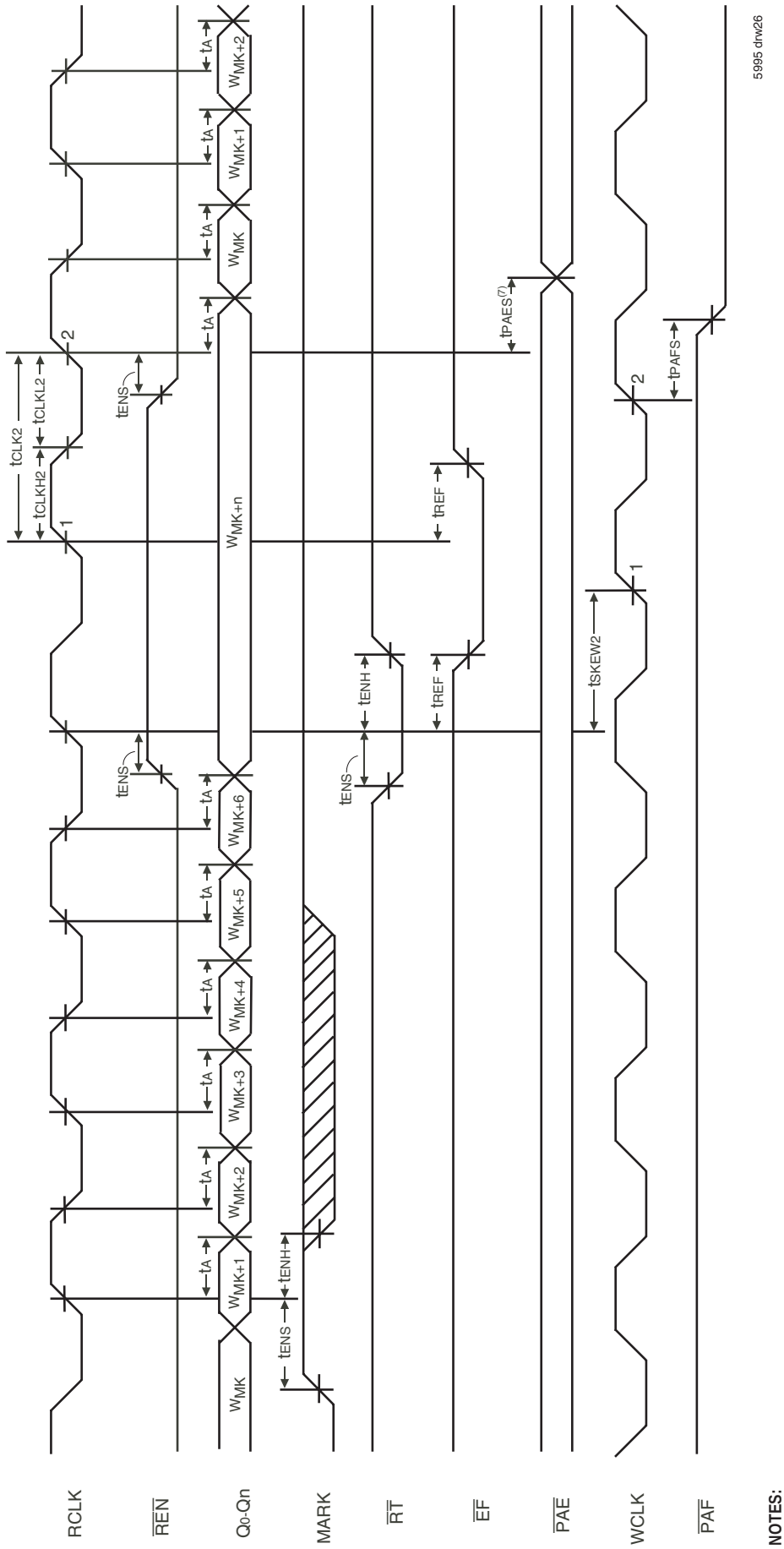
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{IR}$ will go LOW after one WCLK cycle plus t_{WFF}. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then the $\overline{IR}$ assertion may be delayed one extra WCLK cycle.
2. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{PAF}$ will go HIGH after one WCLK cycle plus t_{PAFS}. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then the $\overline{PAF}$ deassertion may be delayed one extra WCLK cycle.
3. n = $\overline{PAE}$ Offset, m = $\overline{PAF}$ offset and D = maximum FIFO depth.
4. D = 16,385 for IDT72T4088, 32,769 for IDT72T4098, 65,537 for IDT72T40108, 131,073 for IDT72T40118.
5. $\overline{OE}$ = LOW.
6. RCLK must be free running for $\overline{EF}$ to update.

Figure 21. Read Cycle and Read Chip Select Timing (FWFT Mode)



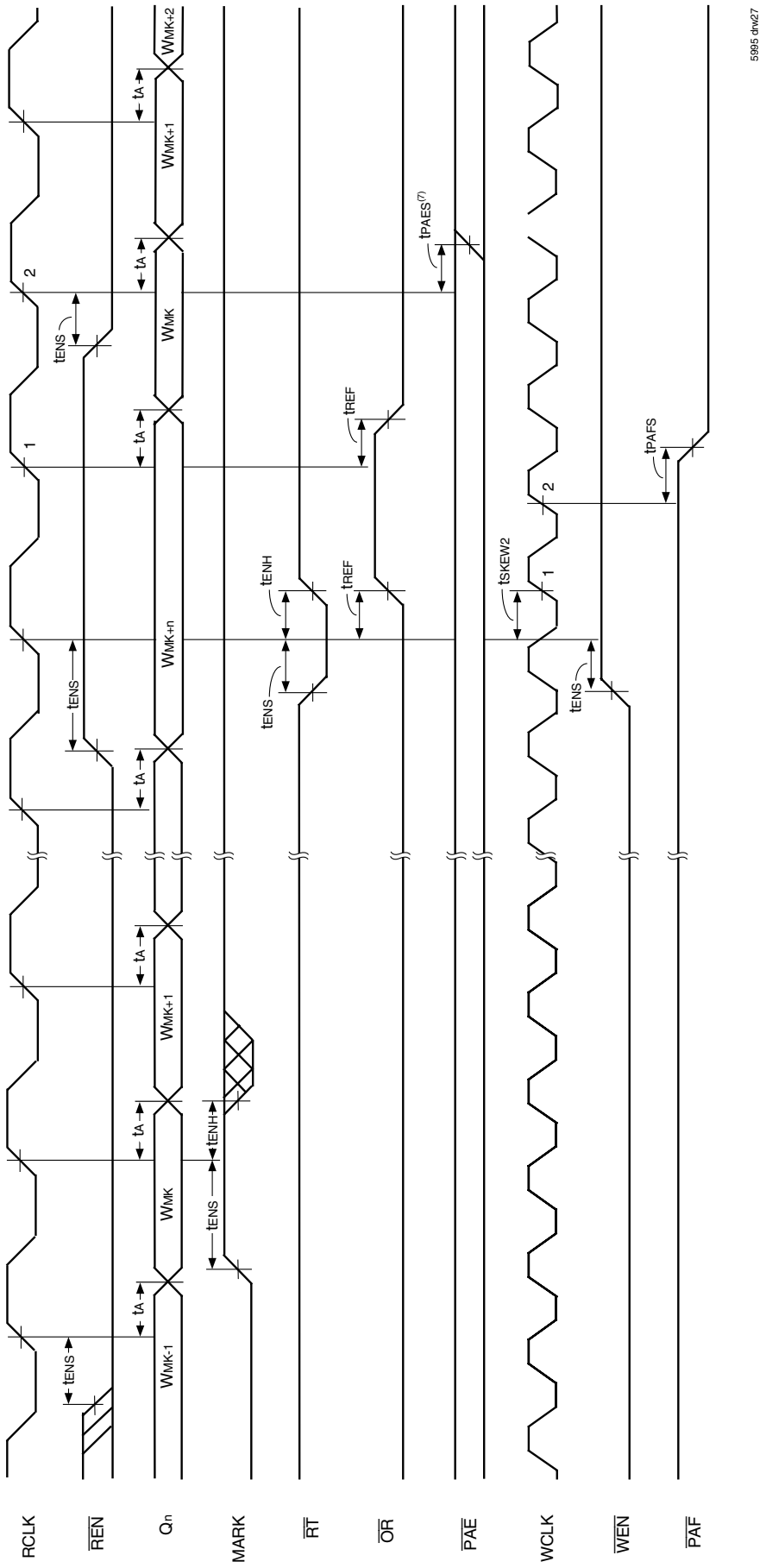
NOTES:
1. It is very important that the $\overline{REN}$ be held HIGH for at least one cycle after $\overline{RCS}$ has gone LOW. If $\overline{REN}$ goes LOW on the same cycle as $\overline{RCS}$ or earlier, then Word, W1 will be lost, Word, W2 will be read on the output when the bus goes to LOW-Z.
2. The 1st Word will fall through to the output register regardless of $\overline{REN}$ and $\overline{RCS}$. However, subsequent reads require that both $\overline{REN}$ and $\overline{RCS}$ be active, LOW.
3. $\overline{RCS}$ functions similarly to $\overline{OE}$, when $\overline{RCS}$ is HIGH the read pointer will not increment.

Figure 22 . $\overline{RCS}$ and $\overline{REN}$ Read Operation (FWFT Mode)



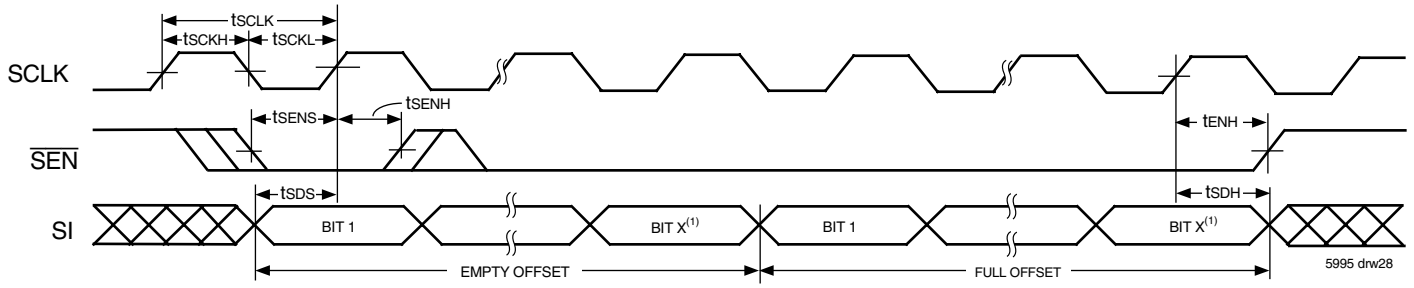
NOTES:
1. Retransmit setup is complete when $\overline{EF}$ returns HIGH.
2. $\overline{OE}$ = LOW;$\overline{RCS}$ = LOW.
3. $\overline{RT}$ must be HIGH when reading from FIFO.
4. Once MARK is set, the write pointer will not increment past the 'marked' location, preventing overwrites of Retransmit data.
5. Before a "MARK" can be set there must be at least 160 bytes of data between the Write Pointer and Read Pointer locations. (160 bytes = 16 words = 8 long words).
6. RCLK must be free running for $\overline{EF}$ to update.
7. A transition in the $\overline{PAE}$ flag may not occur until one RCLK cycle later than shown.
8. In DDR mode the MARK function will "MARK" words only on even word boundaries (i.e. Rising edge of RCLK).

Figure 23 . Retransmit from MARK in Double Data Rate Mode (IDT Standard Mode)



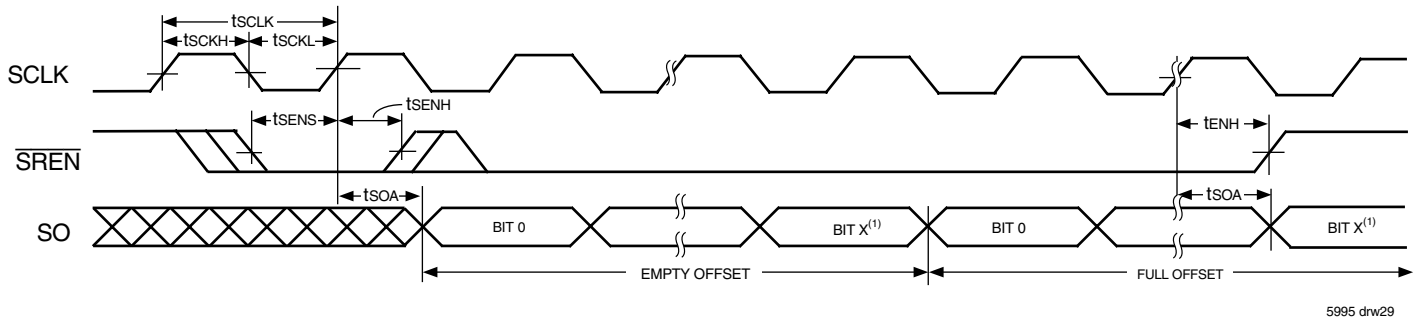
NOTES:
1. Retransmit setup is complete when OR returns LOW.
2. OE = LOW,RCS = LOW.
3. RT must be HIGH when reading from FIFO.
4. Once MARK is set, the write pointer will not increment past the 'marked' location, preventing ovenwrites of Retransmit data.
5. Before a "MARK" can be set there must be at least 160 bytes of data between the Write Pointer and Read Pointer locations. (160 bytes = 16 words = 8 long words).
6. RCLK must be free running for EF to update.
7. A transition in the PAE flag may not occur until one RCLK cycle later than shown.

Figure 24. Retransmit from Mark (FWFT Mode)



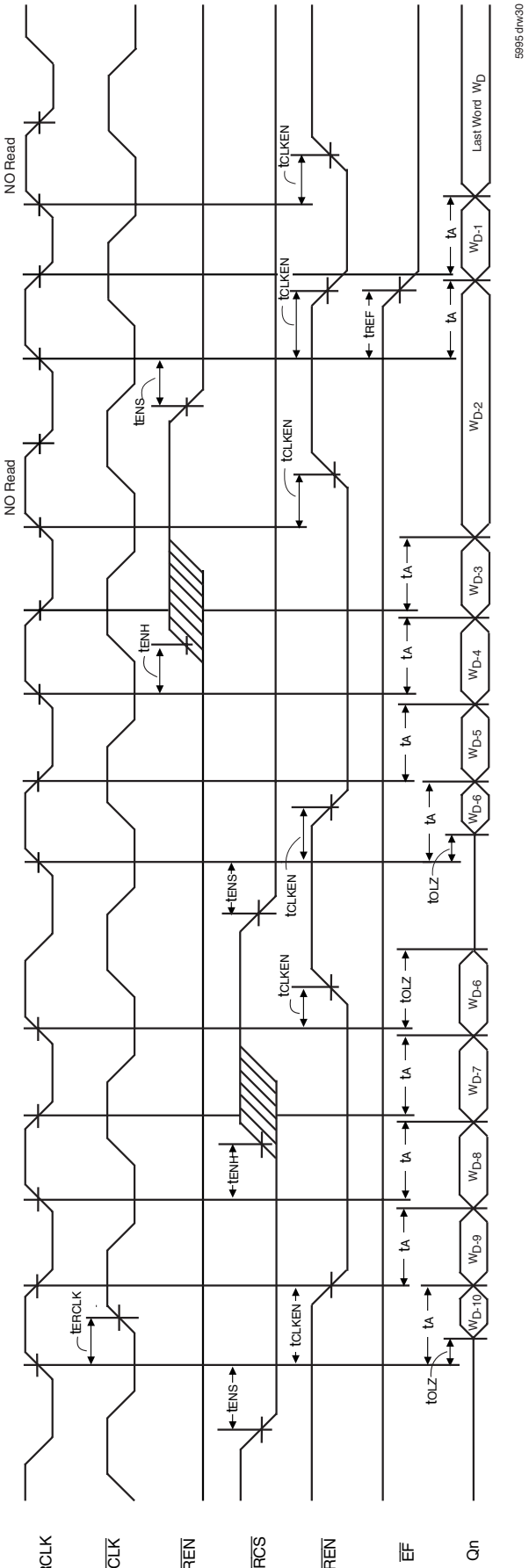
NOTE:
1. In SDR mode, X = 14 for the IDT72T4088, X = 15 for the IDT72T4098, X = 16 for the IDT72T40108, X = 17 for the IDT72T40118.
2. In DDR mode, X = 13 for the IDT72T4088, X = 14 for the IDT72T4098, X = 15 for the IDT72T70108, X = 16 for the IDT72T40118.

Figure 25. Loading of Programmable Flag Registers (IDT Standard and FWFT Modes)



NOTE:
1. In SDR mode, X = 14 for the IDT72T4088, X = 15 for the IDT72T4098, X = 16 for the IDT72T40108, X = 17 for the IDT72T40118.
2. In DDR mode, X = 13 for the IDT72T4088, X = 14 for the IDT72T4098, X = 15 for the IDT72T40108, X = 16 for the IDT72T40118.
3. Offset register values are always read starting from the first location in the offset register upon initiating $\overline{\text{SREN}}$.

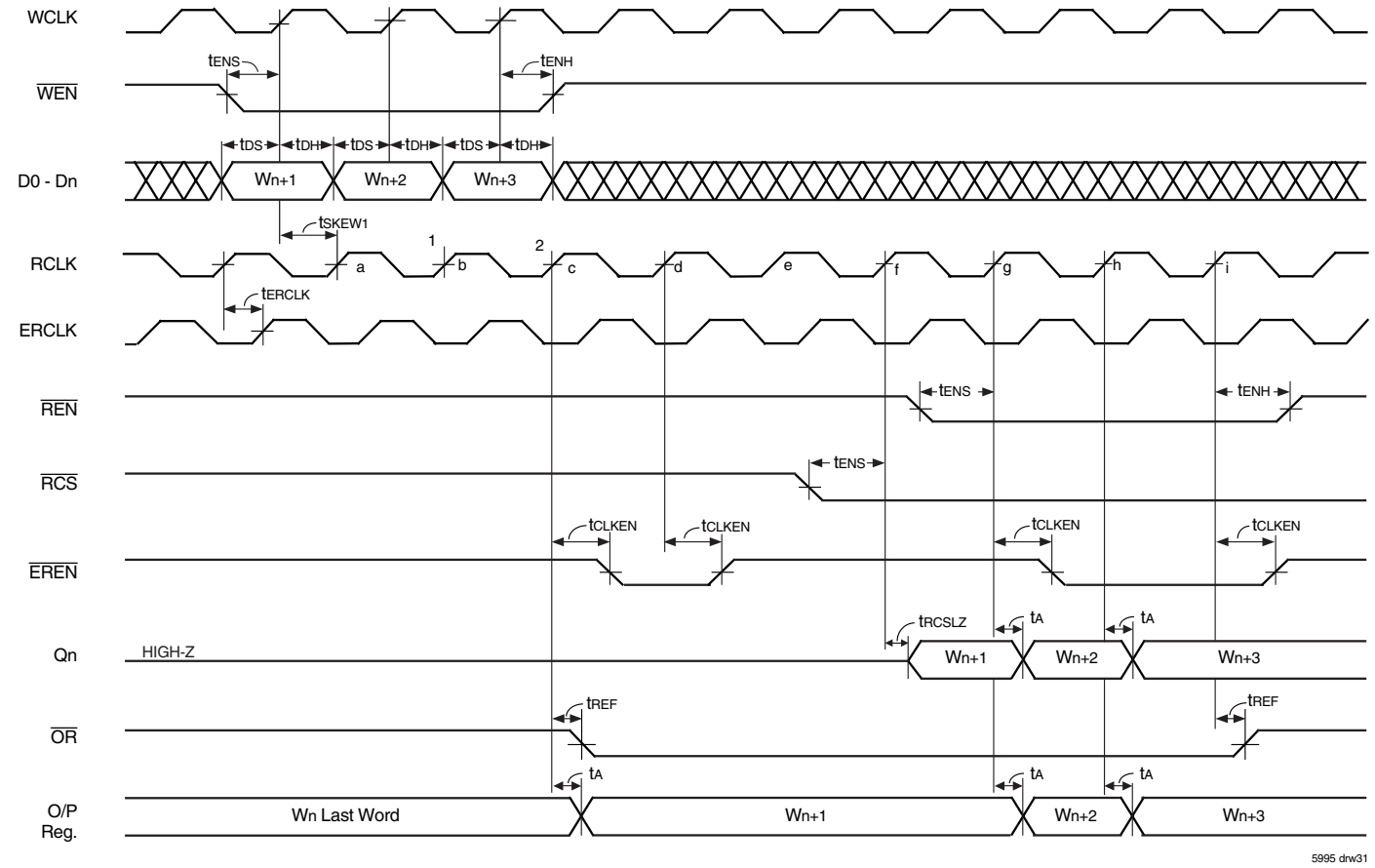
Figure 26. Reading of Programmable Flag Registers (IDT Standard and FWFT Modes)



NOTES:
1. The $\overline{EREN}$ output is "or gated" to $\overline{RCS}$ and $\overline{REN}$ and will follow these inputs provided that the FIFO is not empty. If the FIFO is empty, $\overline{EREN}$ will go HIGH to indicate that there is no new word available.
2. The $\overline{EREN}$ output is synchronous to RCLK.
3. $\overline{OE}$ = LOW.
4. The truth table for $\overline{EREN}$ is shown below:

RCLK	$\overline{EF}$	$\overline{RCS}$	$\overline{REN}$	$\overline{EREN}$
↑	1	0	0	0
↑	1	0	1	1
↑	1	1	0	1
↑	1	1	1	1
↑	0	X	X	1

Figure 27. Echo Read Clock & Read Enable Operation in Double Data Rate Mode (IDT Standard Mode Only)



NOTE:

1. The O/P Register is the internal output register. Its contents are available on the Qn output bus only when $\overline{RCS}$ and $\overline{OE}$ are both active, LOW, that is the bus is not in High-Impedance state.
2. $\overline{OE}$ is LOW.

Cycle:

a&b. At this point the FIFO is empty, $\overline{OR}$ is HIGH.
$\overline{RCS}$ and $\overline{REN}$ are both disabled, the output bus is High-Impedance.

c. Word Wn+1 falls through to the output register, $\overline{OR}$ goes active, LOW.
$\overline{RCS}$ is HIGH, therefore the Qn outputs are High-Impedance. $\overline{EREN}$ goes LOW to indicate that a new word has been placed on the output register.

d. $\overline{EREN}$ goes HIGH, no new word has been placed on the output register on this cycle.

e. No Operation.

f. $\overline{RCS}$ is LOW on this cycle, therefore the Qn outputs go to Low-Impedance and the contents of the output register (Wn+1) are made available.
NOTE: In FWFT mode is important to take $\overline{RCS}$ active LOW at least one cycle ahead of $\overline{REN}$, this ensures the word (Wn+1) currently in the output register is made available for at least one cycle.

g. $\overline{REN}$ goes active LOW, this reads out the second word, Wn+2.
$\overline{EREN}$ goes active LOW to indicate a new word has been placed into the output register.

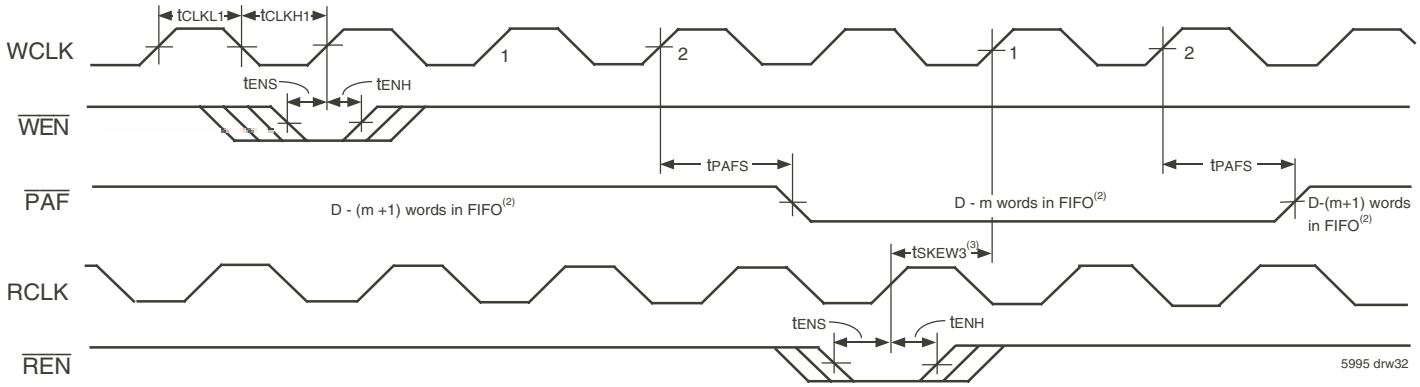
h. Word Wn+3 is read out, $\overline{EREN}$ remains active, LOW indicating a new word has been read out.
NOTE: Wn+3 is the last word in the FIFO.

i. This is the next enabled read after the last word, Wn+3 has been read out. $\overline{OR}$ flag goes HIGH and $\overline{EREN}$ goes HIGH to indicate that there is no new word available.

3. $\overline{OE}$ is LOW.
4. The truth table for $\overline{EREN}$ is shown below:

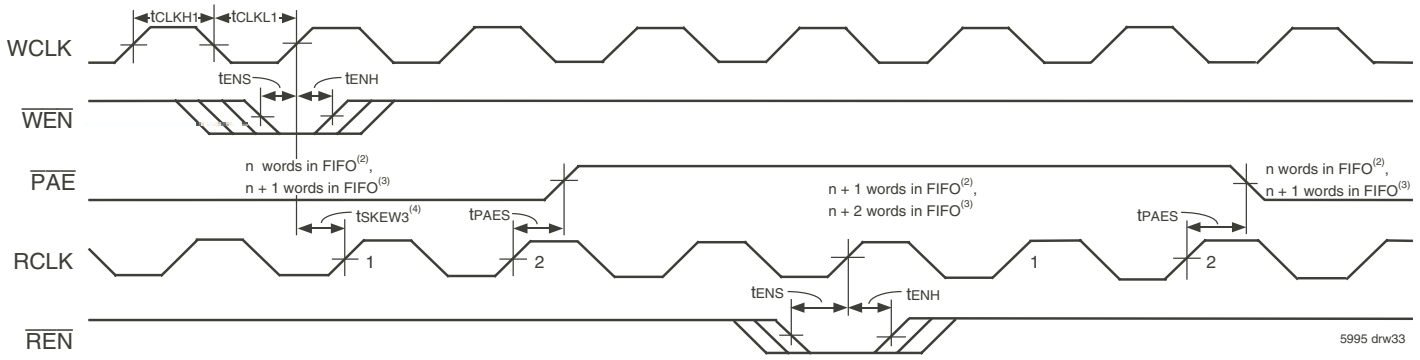
RCLK	$\overline{OR}$	$\overline{RCS}$	$\overline{REN}$	$\overline{EREN}$
↑	0	0	0	0
↑	0	0	1	1
↑	0	1	0	1
↑	0	1	1	1
↑	1	X	X	1

Figure 28. Echo RCLK and Echo $\overline{REN}$ Operation (FWFT Mode Only)



NOTES:
1. m = $\overline{PAF}$ offset.
2. D = maximum FIFO Depth.
   In IDT Standard Mode: D=16,384 for the IDT72T4088, 32,768 for the IDT72T4098, 65,536 for the IDT72T40108, 131,072 for the IDT72T40118.
   In FWFT Mode: D=16,385 for the IDT72T4088, 32,769 for the IDT72T4098, 65,537 for the IDT72T40108, 131,073 for the IDT72T40118.
3. $\overline{PAF}$ is asserted and updated on the rising edge of WCLK only.
4. t_{SKEW3} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{PAF}$ will go HIGH (after one WCLK cycle plus t_{PAFS}). If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW3}, then the $\overline{PAF}$ deassertion time may be delayed one extra WCLK cycle.
5. $\overline{RCS}$ = LOW.

Figure 29. Programmable Almost-Full Flag Timing (IDT Standard and FWFT Modes)



NOTES:
1. n = $\overline{PAE}$ offset.
2. For IDT Standard Mode.
3. For FWFT Mode.
4. $\overline{PAE}$ is asserted and updated on the rising edge of RCLK only.
5. t_{SKEW3} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{PAE}$ will go HIGH (after one RCLK cycle plus t_{PAES}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW3}, then the $\overline{PAE}$ deassertion may be delayed one extra RCLK cycle.
5. $\overline{PAE}$ is asserted and updated on the rising edge of RCLK only.
6. $\overline{RCS}$ = LOW.

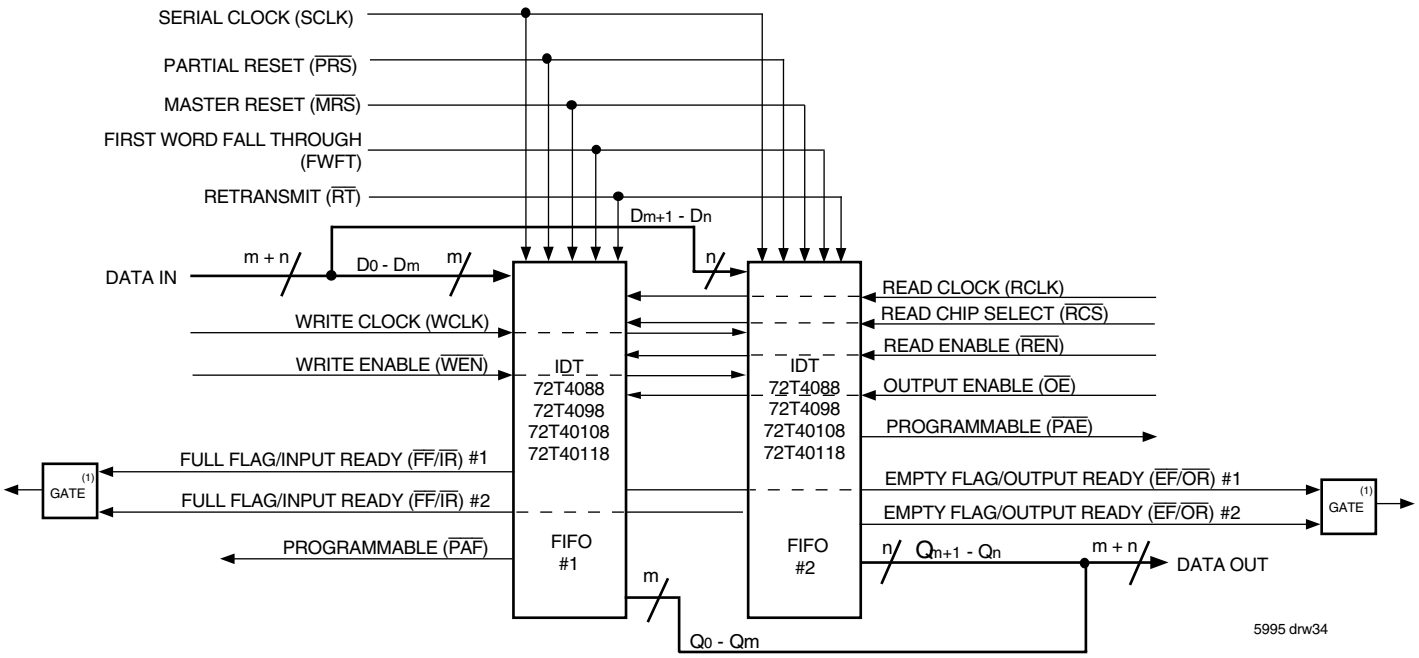
Figure 30. Programmable Almost-Empty Flag Timing (IDT Standard and FWFT Modes)

OPTIONAL CONFIGURATIONS

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting together the control signals of multiple devices. Status flags can be detected from any one device. The exceptions are the $\overline{EF}$ and $\overline{FF}$ functions in IDT Standard mode and the $\overline{IR}$ and $\overline{OR}$ functions in FWFT mode. Because of variations in skew between RCLK and WCLK, it is possible for $\overline{EF}$/$\overline{FF}$ deassertion and $\overline{IR}$/$\overline{OR}$ assertion to vary by one cycle between FIFOs. In IDT Standard mode, such problems can be avoided by creating composite flags, that is, ANDing $\overline{EF}$ of every FIFO, and separately ANDing $\overline{FF}$ of every FIFO. In FWFT mode, composite flags can be created by ORing $\overline{OR}$ of every FIFO, and separately ORing $\overline{IR}$ of every FIFO.

Figure 31 demonstrates a width expansion using two IDT72T4088/72T4098/72T40108/72T40118 devices. D_0 - D_{40} from each device form a 80-bit wide input bus and Q_0-Q_{39} from each device form a 80-bit wide output bus. Any word width can be attained by adding additional IDT72T4088/72T4098/72T40108/72T40118 devices.



NOTES:
1. Use an AND gate in IDT Standard mode, an OR gate in FWFT mode.
2. Do not connect any output control signals directly together.
3. FIFO #1 and FIFO #2 must be the same depth, but may be different word widths.

Figure 31. Block Diagram of 16,384 x 80, 32,768 x 80, 65,536 x 80, 131,072 x 80 Width Expansion

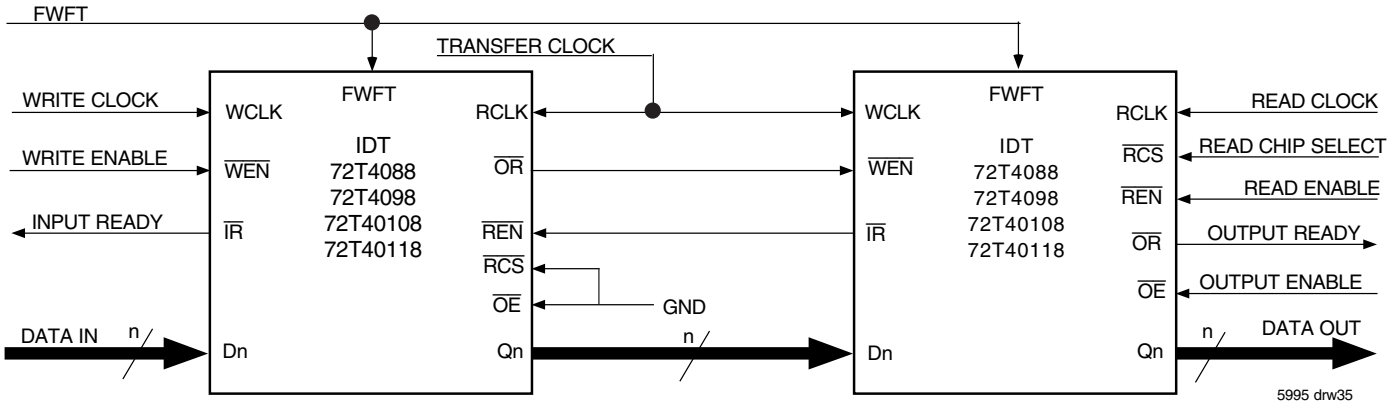


Figure 32. Block Diagram of 32,768 x 40, 65,536 x 40, 131,072 x 40, 262,144 x 40 Depth Expansion in Single Data Rate Mode

DEPTH EXPANSION CONFIGURATION IN SINGLE DATA RATE (FWFT MODE ONLY)

The IDT72T4088 can easily be adapted to applications requiring depths greater than 16,384, 32,768 for the IDT72T4098, 65,536 for the IDT72T40108, 131,072 for the IDT72T40118 with an 40-bit bus width. In FWFT mode, the FIFOs can be connected in series (the data outputs of one FIFO connected to the data inputs of the next) with no external logic necessary. The resulting configuration provides a total depth equivalent to the sum of the depths associated with each single FIFO. Figure 32 shows a depth expansion using two IDT72T4088/72T4098/72T40108/72T40118 devices.

Care should be taken to select FWFT mode during Master Reset for all FIFOs in the depth expansion configuration. Also, the devices must be operating in Single Data Rate mode since that is the only mode available in FWFT. The first word written to an empty configuration will pass from one FIFO to the next ("ripple down") until it finally appears at the outputs of the last FIFO in the chain – no read operation is necessary but the RCLK of each FIFO must be free-running. Each time the data word appears at the outputs of one FIFO, that device's $\overline{OR}$ line goes LOW, enabling a write to the next FIFO in line.

For an empty expansion configuration, the amount of time it takes for $\overline{OR}$ of the last FIFO in the chain to go LOW (i.e. valid data to appear on the last FIFO's outputs) after a word has been written to the first FIFO is the sum of the delays for each individual FIFO:

$$(N - 1)*(4*\text{transfer clock}) + 3*T_{RCLK}$$

where N is the number of FIFOs in the expansion and T_{RCLK} is the RCLK period. Note that extra cycles should be added for the possibility that the t_{SKEW1} specification is not met between WCLK and transfer clock, or RCLK and transfer clock, for the $\overline{OR}$ flag.

The "ripple down" delay is only noticeable for the first word written to an empty depth expansion configuration. There will be no delay evident for subsequent words written to the configuration.

The first free location created by reading from a full depth expansion configuration will "bubble up" from the last FIFO to the previous one until it finally moves into the first FIFO of the chain. Each time a free location is created in one FIFO of the chain, that FIFO's $\overline{IR}$ line goes LOW, enabling the preceding FIFO to write a word to fill it.

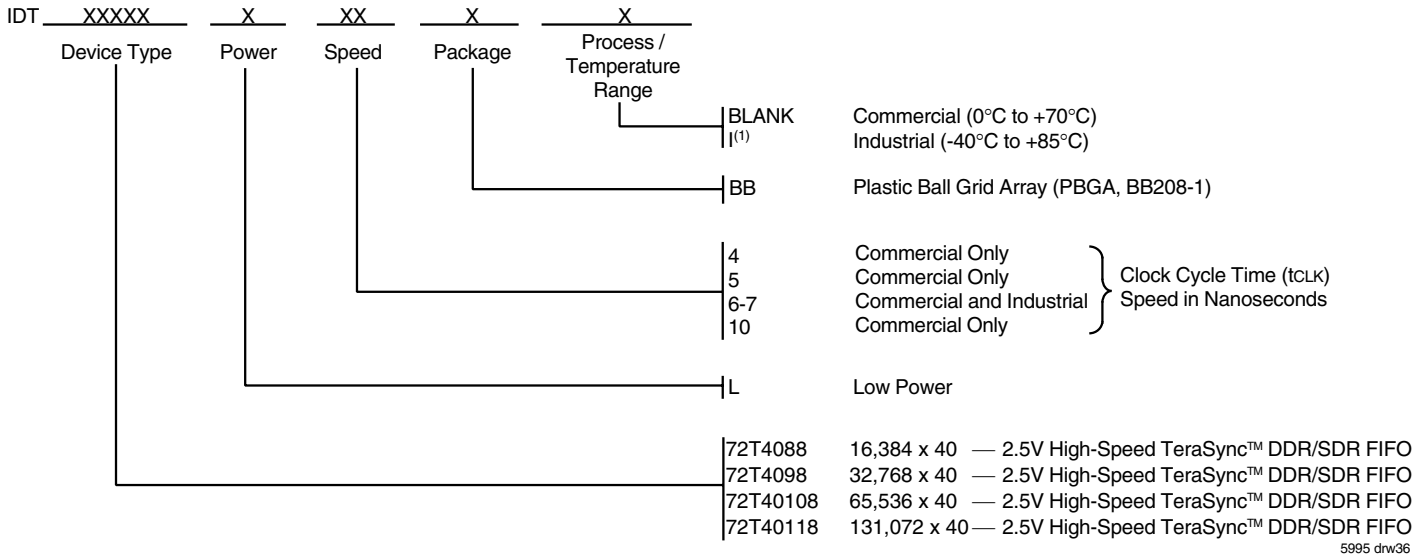
For a full expansion configuration, the amount of time it takes for $\overline{IR}$ of the first FIFO in the chain to go LOW after a word has been read from the last FIFO is the sum of the delays for each individual FIFO:

$$(N - 1)*(3*\text{transfer clock}) + 2\ T_{WCLK}$$

where N is the number of FIFOs in the expansion and T_{WCLK} is the WCLK period. Note that extra cycles should be added for the possibility that the t_{SKEW1} specification is not met between RCLK and transfer clock, or WCLK and transfer clock, for the $\overline{IR}$ flag.

The Transfer Clock line should be tied to either WCLK or RCLK, whichever is faster. Both these actions result in data moving, as quickly as possible, to the end of the chain and free locations to the beginning of the chain.

ORDERING INFORMATION



NOTE:

1. Industrial temperature range product is available for 6-7ns as a standard product. All other speed grades are available by special order.

DATASHEET DOCUMENT HISTORY

03/01/2002	pgs. 1, 4, 6, 8, 9, and 23.
04/08/2002	pgs. 1, 8, 9, 11, 33-37, 42, 46-48, and 51.
04/24/2002	pgs. 19, and 28.
05/24/2002	pgs. 6-9, and 12.
11/21/2002	pgs. 1, and 10.
02/11/2003	pgs. 7, 8, and 27.
03/20/2003	pgs. 25, 27, 28, and 44.
12/17/2003	pgs. 10, 31-34, 36-38, 44, and 49.

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