M65582AMF-XXXFP

NTSC TV Signal Processor with MCU

REJ03F0093-0100Z
Rev.1.0
Sep.19.2003

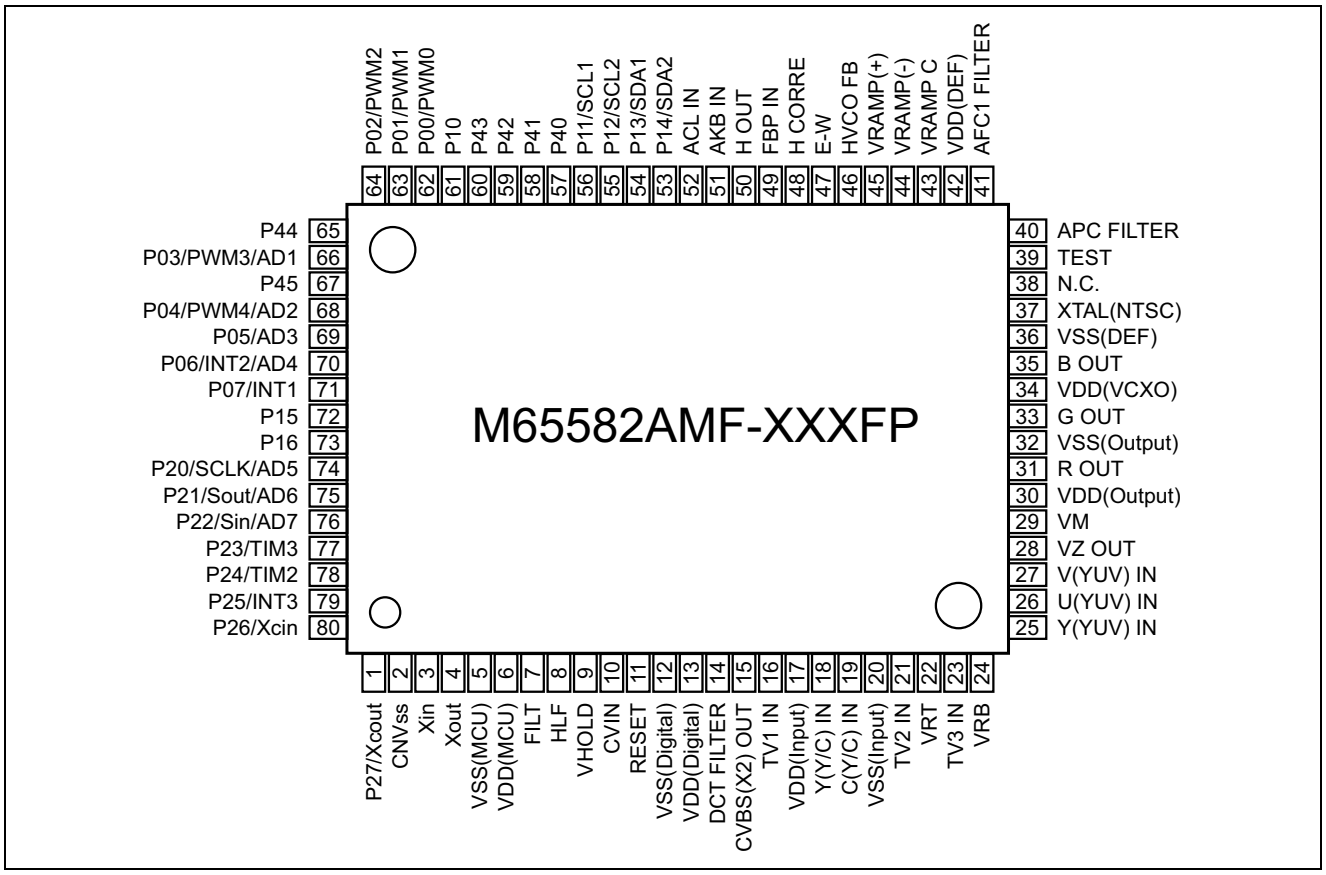
Features

- 1package solution with TV baseband signals (Video and Chroma) processor, deflection and 8bit MCU
- High quality picture by 2 Dimension Adaptive Y/C Separation of 3 Line type
- Built-in VM (Velocity Modulation) circuit emphasizing the picture outline by the changing of the Scanning Speed
- Built-in the correction circuits of the picture distortion which is EAST-WEST function etc. for Flat TV
- Available to use the software for best saled MCU M37272
- Available to input External Video signal, S Video signal and Component Video signal
- High performance OSD function with CCD and Half Tone Display
- Analog Video Switch with 5 Video Inputs Composite Video : 3ch, S Video : 1ch, Component Video : 1ch
- Built-in a high performance Blackstrech
- Built-in YNR
- Built-in 8bit MCU core M37272
  ROM : 60Kbyte, RAM : 2048byte

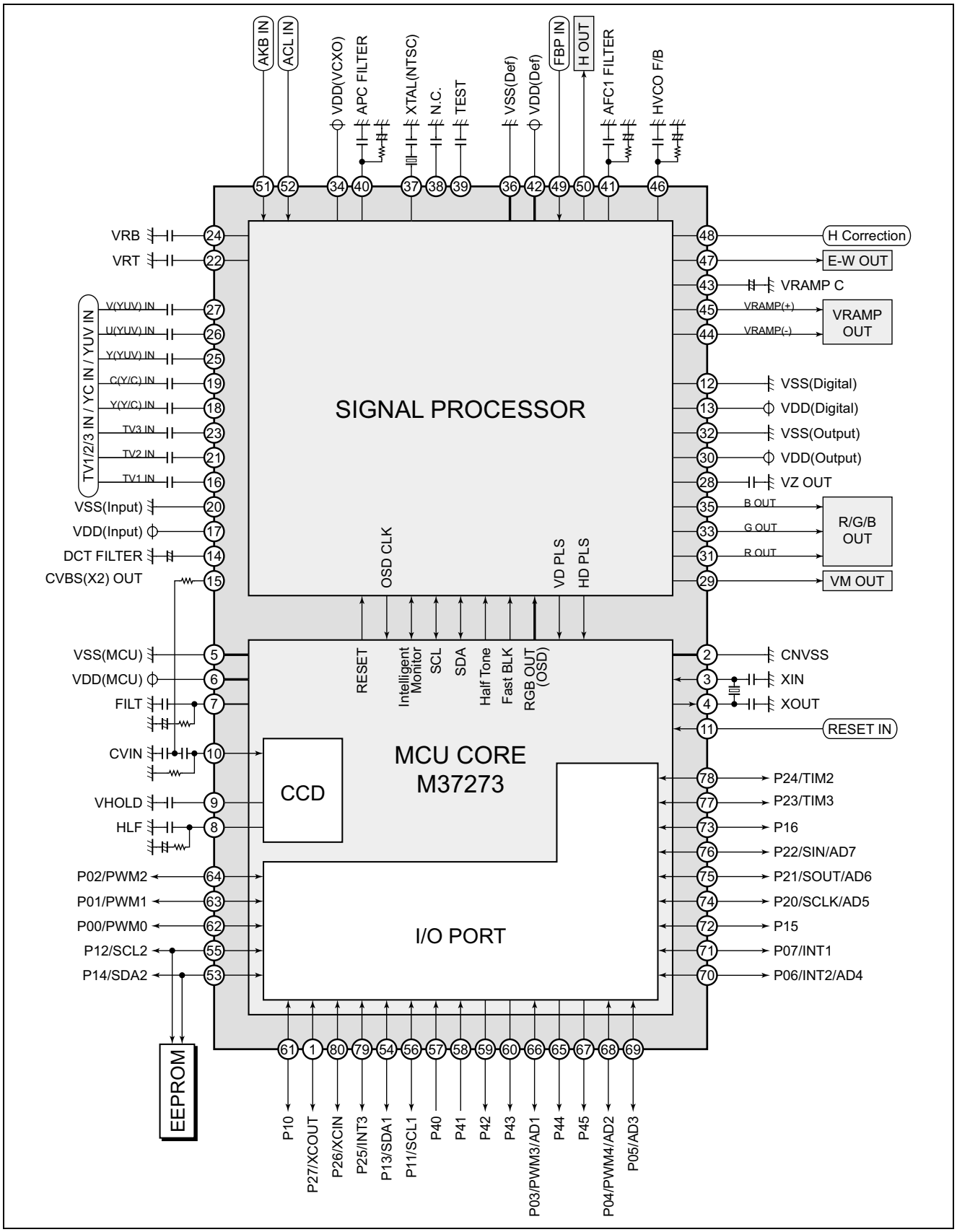
Applications

NTSC color television receivers

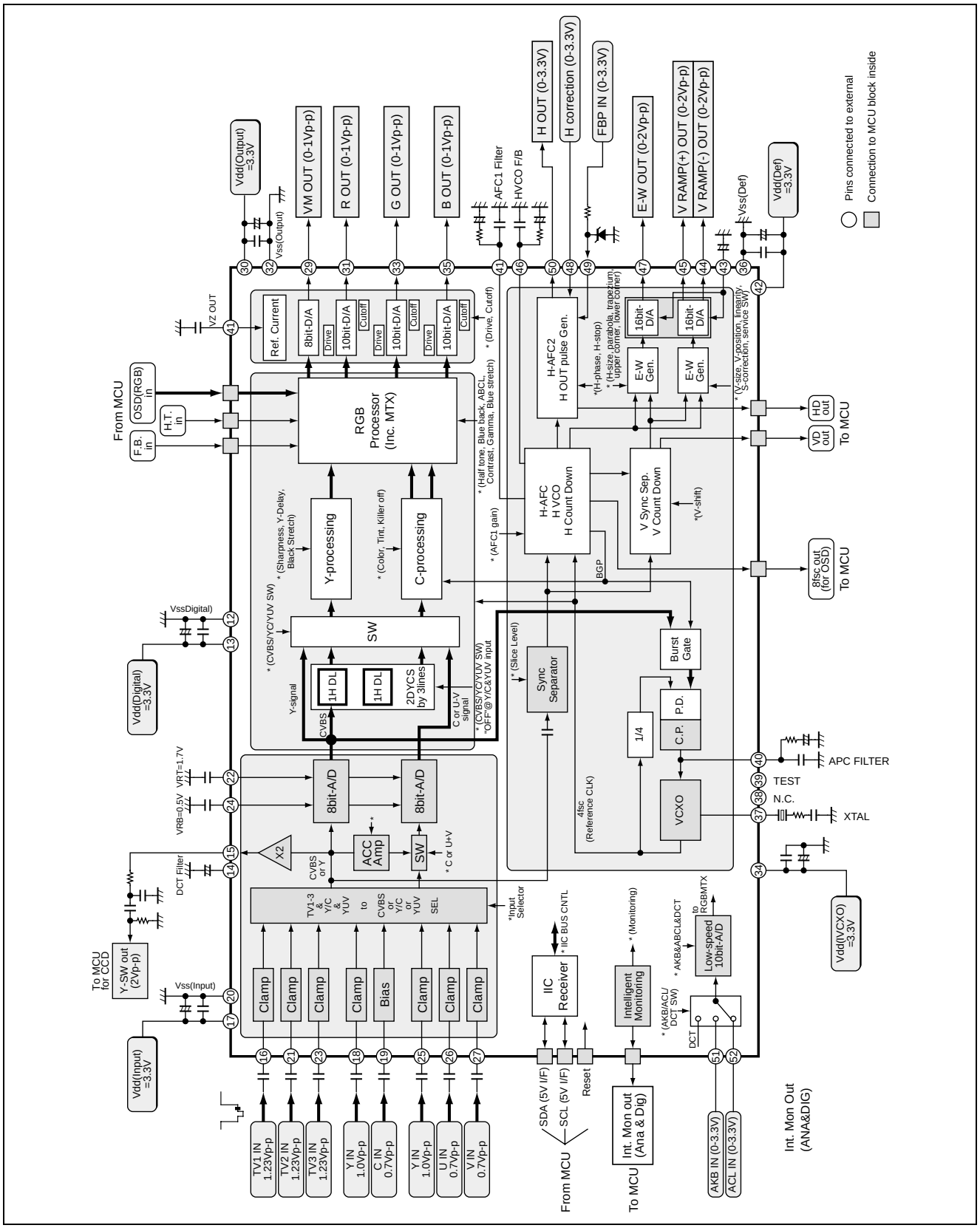
Pin Configuration



Block Diagram (Whole)



Block Diagram (ASIC)



Absolute maximum ratings

Parameter	Symbol	Ratings	Unit	Conditions
Supply voltage (MCU : 5V)	VDD (MCU)	–0.3 to 6.0	V	All voltage are based on Vss.Output transistors are cut off.
Supply voltage (ASIC : 3.3V)	VDD (ASIC)	–0.3 to 4.0	V	
Input Voltage (MCU)	VI (MCU)	–0.3 to Vcc+0.3	V	
Output Voltage (MCU)	VO (MCU)	–0.3 to Vcc+0.3	V	
Circuit current (MCU)	IOH (MCU)	0 to 1 (See note 1)	mA	
Circuit current (P00-P07, P10, P15, P16, P20-P27, P40-P45)	IOL1 (MCU)	0 to 2 (See note 2)	mA	
Circuit current (P11-P14)	IOL2 (MCU)	0 to 6 (See note 2)	mA	
Circuit current (P24-P27)	IOL3 (MCU)	10 (See note 3)	mA	
Digital input voltage	VID (ASIC)	–0.3 to Vcc+0.3	V	
Analog output current	IOUT (ASIC)	–30	mA	
Power dissipation	Pd	2000	mW	
Thermal derating	Kt	20.0	mW/°C	
Operating temperature	Topr	–20 to 70	°C	
Storage temperature	Tstg	–40 to 125	°C	

Recommended Conditions

(Ta=25 to 70°C, Unless otherwise noted)

		Limits			
Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (MCU) (See note 4)	VDD (MCU)	4.75	5.0	5.25	V
Supply voltage (Digital)	VDD (Digital)	3.13	3.3	3.47	V
Supply voltage (Input)	VDD (Input)	3.13	3.3	3.47	V
Supply voltage (Output)	VDD (Output)	3.13	3.3	3.47	V
Supply voltage (VCXO)	VDD (VCXO)	3.13	3.3	3.47	V
Supply voltage (DEF)	VDD (DEF)	3.13	3.3	3.47	V
Supply voltage (MCU)	VSS (MCU)	0	0	0	V
High Iutput voltage P00-P07, P10-P16, P20-P27, P40-P45, RESET, X IN	VIH1 (MCU)	0.8 VDD		VDD	V
High Iutput voltage SCL1, SCL2, SDA1, SDA2 (When using I2C -Bus)	VIH2 (MCU)	0.7 VDD		VDD	V
High Iutput voltage FBP IN	VIH3 (ASIC)	0.8 VDD		VDD	V
Low Iutput voltage P00-P07, P10-P16, P20-P27 P40-P45	VIL1 (MCU)	0		0.4 VDD	V
Low Iutput voltage SCL1, SCL2, SDA1, SDA2 (When using I2C-Bus)	VIL2 (MCU)	0		0.3 VDD	V
Low Iutput voltage (See note 6) RESETB, X IN, TIM2, TIM3, INT1, INT2, INT3, S IN, S CLK	VIL3 (MCU)	0		0.2 VDD	V
Low Iutput voltage FBP IN	VIL4 (ASIC)	0		0.2 VDD	V
High average output current (See note 1) P10-P16, P20-P27, P40-P45	IOH (MCU)			1	mA

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Low average output current (See note 2) P00-P07, P10, P15, P16, P20-P27, P40-P45	IOL1(MCU)			2	mA
Low average output current (See note 2) P11-P14	IOL2(MCU)			6	mA
Low average output current (See note 3) P24-P27	IOL3(MCU)			10	mA
Oscillation frequency (for CPU operation) X IN (See note 5)	f(XIN) (MCU)	7.9	8.0	8.1	MHz
Oscillation frequency (for sub-clock operation) X CIN	f(XCIN) (MCU)	29	32	35	kHz
Input frequency TIM2, TIM3, INT1, INT2, INT3	fhs1 (MCU)			100	kHz
Input frequency S CLK	fhs2 (MCU)			1	MHz
Input frequency SCL1, SCL2	fhs3 (MCU)			400	kHz
Input amplitude video signal CV IN	VI (MCU)	1.5	2.0	2.5	V

Note 1: The total current that flows out the MCU must be 20mA or less.

2: The total input current to MCU (IOL1+IOL2) must be 30mA or less.

3: The total average input current for ports P24-P27 to MCU must be 20mA or less.

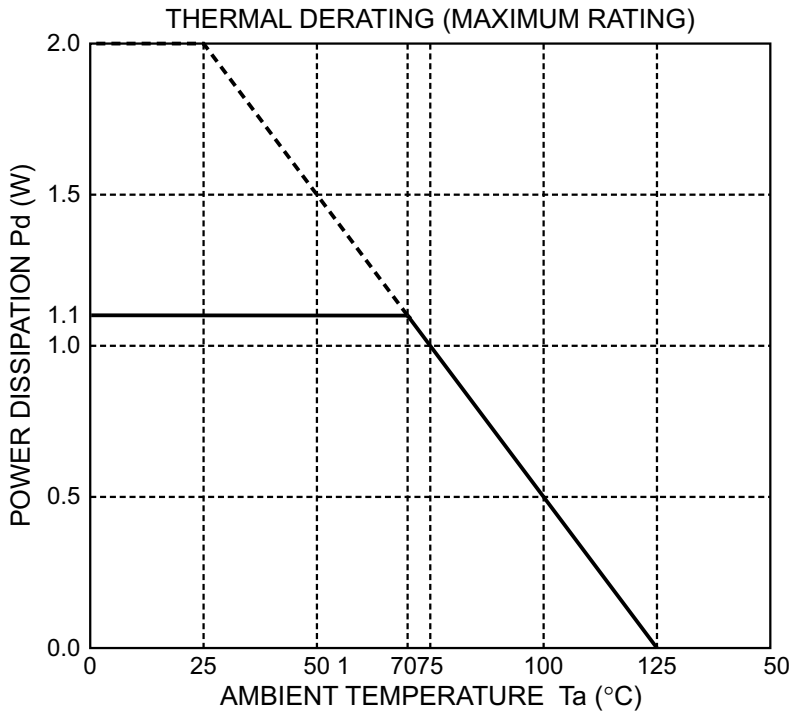
4: Connect 0.1µF or more capacitor externally between the power source pins VDD-VSS so as to reduce power source noise.

5: Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillator circuit. When using the data slicer, use 8MHz.

6: P06, P07, P23-P25 have the hysteresis when these pins are used as interrupt input pins or timer pins.
P11-P14 have the hysteresis when these pins are used as multi-master I^2C-Bus interface ports.
P20-P22 have the hysteresis when these pins are used as serial I/O pins.

7: Pin name in each parameter is described pin names.
(1) Dedicated pins: dedicated pin name.
(2) Double-/Triple-function ports.
When the same limits: I/O port name.
When the limits of function except ports are different from I/O port limits: function pin name.

Thermal derating



I²C bus

I²C bus table

Slave address	Sub address	D7	D6	D5	D4	D3	D2	D1	D0	Standard data
BAh	00h					V STOP	Power Down		H STOP	00h
BAh	01h	Input Video SW					SAW Filter		Line-delay Number	08h
BAh	02h	Pedestal Clamp			VRT Voltage					08h
BAh	04h			Aperture Frequency		Sharpness Noise Coring Level				10h
BAh	05h	EHT				Sharpness Max Gain				0Fh
BAh	06h		Y Delay		YNR SW	YNR Coring Level				6Fh
BAh	08h		Tint							40h
BAh	09h		Color							40h
BAh	0Ah		Contrast							40h
BAh	0Bh	Half Tone		OSD Level (R)						20h
BAh	0Ch	RGB MTX		OSD Level (G)						A0h
BAh	0Dh	OSD COMP		OSD Level (B)						20h
BAh	0Eh	Brightness								80h
BAh	0Fh	AFC Free Run	H AFC Gain	H AFC2 Phase						20h
BAh	10h	RGB P-ON Mute	Y THR 2D	R OUT Mute	Y 2D Fix	G OUT Mute	B OUT Mute	C BPF Fix	Y Mute	02h
BAh	11h					MANEXP		ALFA		02h
BAh	12h	RGB ON	FSC SEL	FSC ORG		Blue Stretch		Gamma		80h
BAh	13h							H OUT Duty	H Free Up	02h
BAh	14h	V BLK Stop		V Size						20h
BAh	15h			V Linearity						20h
BAh	16h	Cuttoff (R) L								00h
BAh	17h	Cutoff (R) H	Drive (R)							C0h
BAh	18h	Cuttoff (G) L								00h
BAh	19h	Cutoff (G) H	Drive (G)							C0h
BAh	1Ah	Cuttoff (B) L								00h
BAh	1Bh	Cutoff (B) H	Drive (B)							C0h
BAh	1Ch					Analog Monitoring Point				00h
BAh	1Dh			TEST I/O	Digital Monitoring Point					00h
BAh	30h	INV 14H CLK	14H CLK DLY		INV DS CLK	DS CLK DLY		A/D CLK DLY		03h
BAh	32h	VJP Width	VJP SW				ABL SEL	UV LPF ON		04h
BAh	33h	Black Stretch Time 1				Black Stretch Time 2				F4h
BAh	34h		DS D/A CLK CTL		DS D/ADither	ABL Speed				04h
BAh	35h	ABL SPE				ABL ASPE				92h
BAh	36h			ABL Time Constant		ABL Gain				05h
BAh	37h			UV Dither Test Enable			UV Dither ON	ABL ASPE2		02h
BAh	38h	AKB Mode	EHT Gain	AKB P						60h
BAh	39h						YCS HBPF Back		YCS HBPF Front	03h
BAh	3Ah			Sharpness Overshoot Gain						20h
BAh	3Bh			Sharpness Preshoot Gain						20h
BAh	3Dh		BS T2 IF ON	THR NZV 1		Black Stretch Depth			Black Stretch SW	34h
BAh	3Eh	THR NZV 2								FFh
BAh	3Fh	THR NZH 1								FFh
BAh	40h	THR NZH 2								FFh
BAh	41h		Killer Level							01h
BAh	42h	AMP CTL		RRAY						C0h
BAh	43h	AMP1 OFF L								5Ah
BAh	44h	AMP1 OFF H	AMP1 ON							04h
BAh	45h		ACC SW	MV2 SW	MV1 SW	MV				30h
BAh	46h	4FSC SW	HD SW	Killer SW	BGP POS					68h
BAh	47h	Force Killer	Clamp BITSEL		OSD Limit	C Delay		AVE SEL		42h
BAh	48h	AMP3 ACC	V Mask Time			AMP TIM		B2 AVE SEL		00h
BAh	49h	YUV MPX SEL	YUV CXUV	YUV UV Inv.	UV Gain	Free Run Offset				00h
BAh	4Bh							Killer Threshold		01h
BAh	4Ch	SWAP	Free Run	BG Start						90h
BAh	4Dh						BW SEL	BW DET		01h
BAh	4Eh	Skew Corrector			VCXO CTRL				Skew Co. Ini.	14h
BAh	4Fh	H Charge Pump			Ramp Slew Rate		Auto Slice Up	Auto Slice Down		78h
BAh	50h	Ref Charge Pump			AFC1 Pull-in		VCXO Free Run		Ref VCO	61h
BAh	51h	H VCO Free Run								00h
BAh	52h	I/M Test	LPF SYNC	V Ramp Filter OFF	Macro OFF	AFC2 Gain		V Sag	Sync Sep Mask	2Ch
BAh	53h	EWV V Reset	Sync Slice Level (V)		Sync Slice Level (H)		4FSC SEL 2	8FSC SEL	B PLL C.P.	67h
BAh	54h	V-Latch OFF	H BLK Stop	V CD Mode 2	BGP C	VD Delay	V Free	V CD Mode		29h

Note: Sub address 03h, 07h, 1Eh-2Fh, 31h, 3Ch, 4Ah and 5Eh-64h are not operational.

Slave address	Sub address	D7	D6	D5	D4	D3	D2	D1	D0	Standard data
BAh	55h	AMP CTRL EN	AMP2 ON							84h
BAh	56h		AMP3 ON							04h
BAh	57h	AMP2 OFF L								40h
BAh	58h								AMP2 OFF H	00h
BAh	59h	AMP3 OFF L								40h
BAh	5Ah					Weak Sig Det Vth			AMP3 OFF H	00h
BAh	5Bh		Weak Sig Chroma ATT			Weak Sig Video ATT			Spot Killer	00h
BAh	5Ch	TEST I/O Control								00h
BAh	5Dh	XTEST RST	LPF SYNC ON	Sync Slice Level (V/W)		MEM TEST	TEST SEL			80h
BAh	65h					V Aperture Coring Level				00h
BAh	66h	V Aperture Gain				V Aperture Max Gain				0Fh
BAh	67h		VM POL	VM Width		VM Coring Level				00h
BAh	68h	VM Gain				VM Max Gain				8Fh
BAh	69h	Black Stretch Start Point		Y Clamp ON	Y Clamp Fix	VM Delay				E6h
BAh	6Ah			S Correction						00h
BAh	6Bh			H Size						20h
BAh	6Ch			Parabola						20h
BAh	6Dh			Trapezium						20h
BAh	6Eh			Upper Corner						20h
BAh	6Fh			Lower Corner						20h
BAh	70h					LIM				0Fh
BAh	71h			V Position						20h
BAh	72h			AFC Bow						20h
BAh	73h			AFC Angle						20h
BAh	74h	V Free 2	AFC2 SEL		Angle OFF	AFC2 Ramp Pos				08h
BAh	75h	H BLK F Position							Clock SEL	81h
BAh	76h	H BLK R Position								80h
BAh	77h			FBP BLK	V BLK Pos		AKB Ref PLS Pos	V BLK Half Kill		02h
BAh	78h	VREF SEL		V Sync LPF 2		V Sync LPF 1		A/D Read Page		04h
BAh	79h		DCT Vth							1Eh
BAh	7Ah				DCT Gain					00h
BAh	7Bh	AKB LIM 1								04h
BAh	7Ch	AKB LIM 2								0Ch
BAh	7Dh	AKB LIM 3								15h
BAh	7Eh	AKB ADD 1								02h
BAh	7Fh	AKB ADD 2								06h
BAh	80h	AKB COMP (R) L								00h
BAh	81h	AKB COMP (G) L								00h
BAh	82h	AKB COMP (B) L								00h
BAh	83h	V EN OFF	AKB Enable	AKB COMP (B) H		AKB COMP (G) H		AKB COMP (R) H		2Ah
BAh	84h			A/D D/A Test EN						00h
BAh	85h			AXIS HYS						1Eh
BAh	86h	AVE SEL AV		ROM HYS						CAh
BAh	87h		B2 COMP							00h
BAh	88h	V In Offset				U In Offset				88h
BAh	89h	AKB SEL		AKB Speed		CLK SEL SAR A/D		ACL Gain	ACL ON	00h
BAh	8Ah		V PLS Width	VM Gain 2		DS CLK Latch Pol	DS CLK Latch ON	DS CLK DIV SEL		40h
BAh	8Bh	AKB SWERR								7Ch
BAh	8Ch	AKB ERRC								14h
BAh	8Dh	AKB SWPON								1Eh
BAh	8Eh	AKB PWERRC								02h

BBh	90h	H COIN	S Det	AKB END	AKB NG		DETNZ			
BBh	91h	B2 ROM <8>	Killer Status	V COIN	B/W Out	Still Det	MV 180		K MONI	
BBh	92h	B2 ROM <7:0>								
BBh	93h	AKB A/D (R) <7:0>								
BBh	94h	AKB A/D (R) <9:8>		AKB New (R)	C Gain					
BBh	95h	AKB A/D (G) <7:0>								
BBh	96h	AKB A/D (G) <9:8>		AKB New (G)						
BBh	97h	AKB A/D (B) <7:0>								
BBh	98h	AKB A/D (B) <9:8>		AKB New (B)						
BBh	99h	Y A/D <7:0>								
BBh	9Ah	C A/D <7:0>								
BBh	9Bh	0	0	1 0						

I²C bus function

Sub address	Data	Bit	Function	Description	Note
00h	D0	1	H STOP	H pulse stop	
	D1-D2	2	Power Down	Power Down control (0: normal, 1: PD0, 2: PD1, 3: PD2)	
	D3	1	V STOP	V output stop	
01h	D0	1	Line-delay Number	Y/C separation mode (0: 3-line mode, 1: 2-line mode)	
	D2	1	SAW Filter	Chroma BPF to high	
	D3-D7	5	Input Video SW	Input video SW (01: TV1 IN, 02: TV2 IN, 04: TV3 IN, 08: Y/C IN, 10: YUV IN)	
02h	D3-D4	2	VRT Voltage	A/D Reference (0: 1.1V, 1: 1.2V, 2: 1.3V, 3: 1.4V)	
	D7	1	Pedestal Clamp	Input clamp select (0: pedestal clamp, 1: sync-tip clamp)	
04h	D0-D3	4	Sharpness Noise coring level	Sharpness coring level (0: minimum —— F: maximum)	V Latch
	D4-D5	2	Aperture Frequency	Sharpness fo (0: 2-clk <—> 3: 5-clk)	V Latch
05h	D0-D3	4	Sharpness Max Gain	Sharpness limiter level (0: minimum —— F: maximum)	V Latch
	D4-D7	4	EHT	EHT gain control (0: minimum —— F: maximum)	V Latch
06h	D0-D3	4	YNR Coring Level	YNR limiter level (0: minimum —— F: maximum)	V Latch
	D4	1	YNR SW	YNR enable	V Latch
	D5-D6	2	Y Delay	Y delay time (0: 0nsec—— 3: 210nsec)	V Latch
08h	D0-D6	7	Tint	Tint level control (00: -45˚ —— 7F: +45˚)	V Latch
09h	D0-D6	7	Color	Color level control (00: 0% —— 7F: 200%)	V Latch
0Ah	D0-D6	7	Contrast	Contrast control (00: 0% —— 7F: 200%)	V Latch
0Bh	D0-D5	6	OSD Level (R)	R OSD level (00: 0% —— 7F: maximum)	V Latch
	D6-D7	2	Half Tone	Half tone level control (Picture/OSD ratio 0: 50%/50% —— 3: 12.5%/87.5%)	V Latch
0Ch	D0-D5	6	OSD Level (G)	G OSD level (00: 0% —— 7F: maximum)	V Latch
	D6-D7	2	RGB MTX	RGB matrix ratio (0: 12/8, 1: 13/8, 2: 14/8, 3: 14/8)	V Latch
0Dh	D0-D5	6	OSD Level (B)	B OSD level (00: 0% —— 7F: maximum)	V Latch
	D6-D7	2	OSD COMP	Contrast clip level for OSD (0: low —— 3: high)	V Latch
0Eh	D0-D7	8	Brightness	Brightness control (00: -50% —— 7F: +50%)	V Latch
0Fh	D0-D5	6	H AFC2 Phase	H position (00: +2.6µsec —— 7F: -2.6µsec)	
	D6	1	H AFC Gain	AFC1 Gain (0: low, 1: high)	
	D7	1	AFC Free Run	AFC1 Force free-run	
10h	D0	1	Y Mute	Y output mute	
	D1	1	C BPF Fix	Chroma signal generate from H/V BPF only	
	D2	1	B OUT Mute	B output mute	
	D3	1	G OUT Mute	G output mute	
	D4	1	Y 2D Fix	Y signal generate from 2DYCS	
	D5	1	R OUT Mute	R output mute	
	D6	1	Y THR 2D	Y signal through 2D YCS	
	D7	1	RGB P-ON Mute	RGB output mute	
11h	D0-D1	2	ALFA	Adaptive detection sensitivity (0: minimum —— 3: maximum)	
	D2-D3	1	MANEXP	Y/C separation force select (0: adaptive, 2: V, 3: H/V)	
12h	D0-D1	2	Gamma	Gamma control (0: none —— 3: deep)	
	D2-D3	2	Blue Stretch	Blue stretch control (0: none —— 3: deep)	
	D4-D5	2	FSC ORG	Chroma decoder phase select	
	D6	1	FSC SEL	Chroma decoder clock select	
	D7	1	RGB ON	RGB output (0: RGB mute except OSD, 1: RGB output)	
13h	D0	1	H Free Up	AFC1 Free-run frequency up (about 700Hz)	
	D1	1	H OUT Duty	H pulse width (0: 25µsec, 1: 19µsec)	
14h	D0-D5	6	V Size	V ramp amplitude (00: -20% —— 3F: +20%)	
	D7	1	V BLK Stop	V blanking off	
15h	D0-D5	6	V Linearity	V linearity (00: -3% —— 3F: +3%)	
16h	D0-D7	9	Cutoff (R)	R cutoff control (000: dark —— 1FF: light)	V Latch
17h	D7				
	D0-D6	7	Drive (R)	R drive control (00: -2.5dB —— 7F: +3.5dB)	V Latch
18h	D0-D7	9	Cutoff (G)	G cutoff control (000: dark —— 1FF: light)	V Latch
19h	D7				
	D0-D6	7	Drive (G)	G drive control (00: -2.5dB —— 7F: +3.5dB)	V Latch
1Ah	D0-D7	9	Cutoff (B)	B cutoff control (000: dark —— 1FF: light)	V Latch
1Bh	D7				
	D0-D6	7	Drive (B)	B drive control (00: -2.5dB —— 7F: +3.5dB)	V Latch
1Ch	D0-D3	4	Analog Monitoring Point	Intelligent monitoring output select (Analog)	
1Dh	D0-D4	5	Digital Monitoring Point	Intelligent monitoring output select (Digital)	
	D5	1	TEST I/O	Intelligent monitoring output enable (Digital)	
30h	D0-D1	2	A/D CLK DLY	A/D clock delay adjust (0: none —— 3: delay)	
	D2-D3	2	DS CLK DLY	ΔΣ D/A (for V-ramp and E-W) clock delay adjust (0: none —— 3: delay)	
	D4	1	INV DS CLK	ΔΣ D/A (for V-ramp and E-W) clock polarity (0: none —— 1: invert)	

Sub address	Data	Bit	Function	Description	Note
30h	D5-D6	2	14H CLK DLY	4fsc clock delay adjust (0: none —– 3: delay)	
	D7	1	INV 14H CLK	4fsc clock polarity (0: none, 1: invert)	
32h	D1	1	UV LPF ON	UV LPF (digital) enable	
	D2	1	ABL SEL	ABL function (0: enable, 1: disenable)	
	D6	1	VJP SW	Jump SW enable	
	D7	1	VJP Width	Jump pulse width (0: normal, 1: wide +2-line)	
33h	D0-D3	4	Black Stretch Time 2	Black stretch recover time (0: slow —– F: fast)	
	D4-D7	4	Black Stretch Time 1	Black stretch attack time (0: slow —– F fast)	
34h	D2-D3	2	ABL Speed	ABL processing speed (0: X1, 1: X2, 2: X4, 3: X8)	
	D4	1	DS D/A Dither	ΔΣ D/A (for V-Ramp and E-W) dither enable	
	D5-D6	2	DS D/A CLK CTL	ΔΣ D/A (for V-Ramp and E-W) clock select (0: 28M, 1: 24M, 2: 14M, 3: 16M)	
35h	D0-D3	4	ABL ASPE	ABL attack speed (0: slow —– 7: fast)	
	D4-D7	4	ABL SPE	ABL recover speed (0: slow —– 7: fast)	
36h	D0-D3	4	ABL Gain	ABL gain control (0: minimum —– 7: maximum)	
	D4-D6	3	ABL Time Constant	ABL time constant (0: slow —– 7: fast)	
37h	D0-D1	2	ABL ASPE 2	ABL attack speed 2 (0: slow —– 7: fast)	
	D2	1	UV Dither ON	UV dither enable	
	D3-D5	3	UV Dither Test Enable	UV dither test select	
38h	D0-D5	6	AKB P	AKB reference pulse height (00: minimum —– 3F: maximum)	
	D6	1	EHT Gain	EHT gain up (0: normal, 1: high)	
	D7	1	AKB Mode	AKB mode select (0: differential mode, 1: absolute mode)	
39h	D0	1	YCS HBPF Front	Y/C separation front BPF band width (0: wide, 1: narrow)	
	D1-D2	2	YCS HBPF Back	Y/C separation rear BPF band width (0: none, 1: wide —– 2 and 3: narrow)	
3Ah	D0-D5	6	Sharpness Overshoot Gain	Sharpness overshoot gain (00: soft —– 3F: sharp)	V Latch
3Bh	D0-D5	6	Sharpness Preshoot Gain	Sharpness preshoot gain (00: soft —– 3F: sharp)	V Latch
3Dh	D0	1	Black Stretch SW	Black stretch SW (0: disenable, 1: enable)	
	D1-D3	3	Black Stretch Depth	Black stretch depth (0: shallow —– 7: deep)	
	D6	1	BS T2 IF ON	Black stretch recover time constant (0: slow, 1: fast)	
	D4-D5	10	THR NZV	Noise detection threshold level in field (000: minimum —– 3FF: maximum)	
3Eh	D0-D7				
3Fh	D0-D7	16	THR NZH	Noise detection threshold level in line (0000: minimum —– FFFF: maximum)	
40h	D0-D7				
41h	D0-D6	7	Killer Level	Color Killer threshold level (00: deep —– 7F: shallow)	
42h	D0-D5	6	RRAY	R-Y phase offset (00: 0° —– 3F: 90°)	
	D6-D7	2	AMP CTL	Analog ACC amp maximum gain (0: 0dB —– 3: +30dB)	
43h	D0-D7	9	AMP1 OFF	Analog ACC amp #1 on –>off level (000: minimum —– 1FF: maximum)	
44h	D7				
	D0-D6	7	AMP1 ON	Analog ACC amp #1 off –>on level (00: minimum —– 7F: maximum)	
45h	D0-D3	4	MV	Macro vision (burst) detect level	
	D4	1	MV1 SW	Macro vision (burst) detect enable	
	D5	1	MV2 SW	Macro vision (burst) detect position	
	D6	1	ACC SW	ACC enable	
46h	D0-D4	5	BGP POS	BGP (for chroma decoder) position	
	D5	1	Killer SW	Killer detector mode select (0: synchronous detect, 1: amplitude detect)	
	D6	1	HD SW	HD out (for OSD) select (0: FBP, 1: AFC1 pulse)	
	D7	1	4FSC SW	A/D-LOGIC clock swap	
47h	D0-D1	2	AVE SEL	Chroma decoder time constant (0: 32H, 1: 16H, 2: 8H, 3: 1H)	
	D2-D3	2	C Delay	Chroma delay time (0: none —– 3: delay)	
	D4	1	OSD Limit	OSD limit select	
	D6	1	Clamp BITSEL	Y digital clamp time constant (0: fast, 1: slow)	
	D7	1	Force Killer	Forced killer	
48h	D0-D1	2	B2 AVE SEL	Accumulation time control of demodulation	
	D2-D3	2	AMP TIM	Analog ACC hysteresis select	
	D4-D6	3	V Mask Time	V masking time for demodulation	
	D7	1	AMP3 ACC	ACC maximum gain	
49h	D0-D3	4	Free Run Offset	VCXO free-run frequency adjust	
	D4	1	UV Gain	U/V gain up	
	D5	1	YUV UV Inv.	U/V invert	
	D6	1	YUV CXUV	YC/YUV select	
	D7	1	YUV MPX SEL	U/V multiplex select (0: 2fsc, 1: fsc)	
4Bh	D0-D1	2	Killer Threshold	PLL stop burst level	
4Ch	D0-D5	6	BG Start	BGP (for PLL) timing control	
	D6	1	Free Run	VCXO force free-run	
	D7	1	SWAP	Burst PLL polarity (0: reverse, 1: normal)	
4Dh	D0-D1	2	BW DET	PLL Killer threshold level	

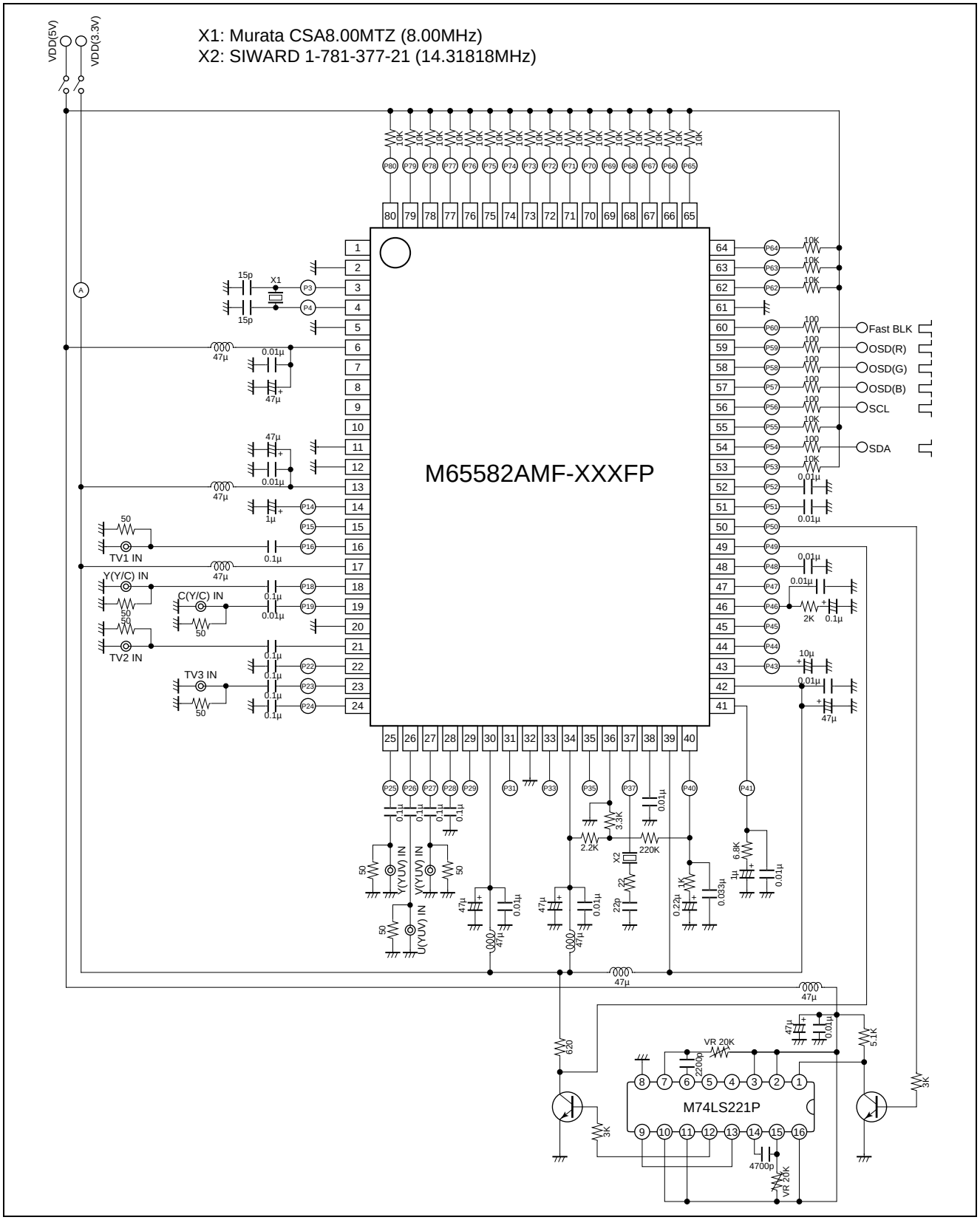
Sub address	Data	Bit	Function	Description	Note
4Dh	D2	1	BW SEL	ΔΣ D/A clock invert	
4Eh	D0	1	Skew Co Ini.	Skew corrector reference phase	
	D1-D4	4	VCXO CTRL	VCXO phase adjust	
	D5-D7	3	Skew Corrector	Skew corrector phase control	
4Fh	D0-D1	2	Auto Slice Down	Auto slicer level down (0: up —— 3: down)	
	D2	1	Auto Slice Up	Auto slicer level up	
	D3-D4	2	Ramp Slew Rate	AFC2 Ramp slew rate	
	D5-D7	3	H Charge Pump	AFC1 charge pump current (4: minimum – 5 – 6 – 7 – 0 – 1 – 2 – 3: maximum)	
50h	D0	1	Ref VCO	Ref PLL loop gain up	
	D1-D2	2	VCXO Free Run	VCXO f_0 adjust	
	D4	1	AFC1 Pull-in	AFC1 pull-in range wide	
	D5-D7	3	Ref Charge Pump	Ref PLL charge pump current (4: minimum – 5 – 6 – 7 – 0 – 1 – 2 – 3: maximum)	
51h	D0-D7	8	H VCO Free Run	H VCO f_0 adjust (In case of data is XYh, X decrease the f_0, and Y increase the f_0)	
52h	D0	1	Sync Sep Mask	Sync separator masking control	
	D1	1	V Sag	V sag prevent on	
	D2-D3	2	AFC2 Gain	AFC2 gain control (0: fast —— 3: slow)	
	D4	1	Macro OFF	Top vend (when macrovision) prevent off	
	D5	1	V Ramp Filter OFF	V Ramp and E-W output filter off	
	D6	1	LPF SYNC	Pre sync separation LPF f_0 becomes low	
	D7	1	I/M Test	Intelligent monitoring signal (Digital) enable to output to pin 51	
53h	D0	1	B PLL C.P.	Chroma APC charge pump current up (0: normal, 1: X5)	
	D1	1	8FSC SEL	H rate clock select (0: 12MHz, 1: 4fsc skew clock)	
	D2	1	4FSC SEL 2	4fsc skew force off (0: H rate clock, 1: Burst rate clock)	
	D3-D4	2	Sync Slice Level (H)	Sync slice level (H sync separation)	
	D5-D6	2	Sync Slice Level (V)	Sync slice level (V sync separation)	
	D7	1	EWV V Reset	ΔΣ D/A V reset on	
54h	D0-D1	2	V CD Mode	V detect window switch timing (0: 5H, 1: 3H, 2: 1H, 3: force 1 window)	
	D2	1	V Free	Force V free-run	
	D3	1	VD Delay	VD pulse delay	
	D4	1	BGP C	BGP (for deflection block) width (0: normal, 1: Don't use. Useful only test mode)	
	D5	1	V CD Mode 2	V sub-counter enable	
	D6	1	H BLK Stop	H blanking off	
	D7	1	V-Latch OFF	IIC V latch off (for test)	
55h	D0-D6	7	AMP2 ON	Analog ACC amp #2 off –>on level (00: minimum —— 7F: maximum)	
	D7	1	AMP CTRL EN	Analog ACC amp #1, #2 and #3 enable	
56h	D0-D6	7	AMP3 ON	Analog ACC amp #3 off –>on level (00: minimum —— 7F: maximum)	
57h	D0-D7	9	AMP2 OFF	Analog ACC amp #2 on –>off level (000: minimum —— 1FF: maximum)	
58h	D0				
59h	D0-D7	9	AMP3 OFF	Analog ACC amp #3 on –>off level (000: minimum —— 1FF: maximum)	
5Ah	D0				
	D1-D3	3	Weak Sig Det Vth	Noise detect level of RF weak signal (0: minimum —— 7: maximum)	
5Bh	D0	1	Spot Killer	Force spot Killer	
	D1-D3	3	Weak Sig Video ATT	Video attenuation control of RF weak signal (0: no attenuation —— 7: maximum)	
	D4-D6	3	Weak Sig Chroma ATT	Chroma attenuation control of RF weak signal (0: no attenuation —— 7: maximum)	
5Ch	D0-D7	8	TEST I/O Control	Test mode I/O control (only factory use)	
5Dh	D0-D2	3	TEST SEL	Test mode select (only factory use)	
	D3	1	MEM TEST	Memory test mode (only factory use)	
	D4-D5	2	Sync Slice Level (V/W)	Sync slice level (V sync separation within narrow window)	
	D6	1	LPF SYNC ON	Pre sync separation LPF enable	
	D7	1	XTEST RST	Test mode select (only factory use)	
65h	D0-D3	4	V Aperture Coring Level	V aperture coring level (0: minimum —— F: maximum)	V Latch
66h	D0-D3	4	V Aperture Max Gain	V aperture limit level (0: minimum —— F: maximum)	V Latch
	D4-D7	4	V Aperture Gain	V aperture gain (0: minimum —— F: maximum)	V Latch
67h	D0-D3	4	VM Coring Level	VM coring level (0: minimum —— F: maximum)	V Latch
	D4-D5	2	VM Width	VM width (0: minimum —— 3: maximum)	V Latch
	D6	1	VM POL	VM polarity	V Latch
68h	D0-D3	4	VM Max Gain	VM limit level (0: minimum —— F: maximum)	V Latch
	D4-D7	4	VM Gain	VM gain (0: minimum —— F: maximum)	V Latch
69h	D0-D3	4	VM Delay	VM output delay (0: forward —— F: delay)	V Latch
	D4	1	Y Clamp Fix	Y digital clamp control 1 (0: Y digital clamp enable, 1: Y digital clamp disenable)	
	D5	1	Y Clamp ON	Y digital clamp control 2 (0: clamp level is held, 1: clamp level is refleshed at all time)	
	D6-D7	2	Black Stretch Start Point	Black stretch start point (0: 25%, 1: 31%, 2: 38%, 3: 44%)	
6Ah	D0-D5	6	S Correction	V Ramp S correction (00: 0% —— 3F: +3%)	
6Bh	D0-D5	6	H Size	E-W output DC level (00: +250mV —— 3F: -250mV)	
6Ch	D0-D5	6	Parabola	E-W output amplitude (00: 0.1V_{p-p} —— 3F: 0.7V_{p-p})	

Sub address	Data	Bit	Function	Description	Note
6Dh	D0-D5	6	Trapezium	E-W trapezium (00: -50% —— 3F: +50%)	
6Eh	D0-D5	6	Upper Corner	E-W upper corner (00: -200% —— 3F: +200%)	
6Fh	D0-D5	6	Lower Corner	E-W lower corner (00: -200% —— 3F: +200%)	
70h	D0-D3	4	LIM	Chroma detect level for 2D YCS (0: minimum —— F: no limit)	
71h	D0-D5	6	V Position	V Ramp output DC level (00: -10% —— 3F: +10%)	
72h	D0-D5	6	AFC Bow	AFC Bow (00: +1.5µsec —— 3F: -1.5µsec)	
73h	D0-D5	6	AFC Angle	AFC Angle (00: +/-1.5µsec —— 3F: -/+1.5µsec)	
74h	D0-D3	4	AFC2 Ramp Pos	AFC2 Ramp position (0: -5.2µsec —— F: +5.2µsec)	
	D4	1	Angle OFF	AFC Angle/Bow disenable	
	D6	1	AFC2 SEL	AFC Angle/Bow and H correction disenable	
	D7	1	V Free 2	Adaptive vertical free-run mode (by H coincidence)	
75h	D0	1	Clock SEL	ΔΣ D/A clock select (0: enable to select "DS D/A CLK CTL, 1: same clock as A/D)	
	D2-D7	6	H BLK F Position	H bllanking (right side) timing (00: +2.6µsec —— 3F: -2.6µsec)	
76h	D2-D7	6	H BLK R Position	H bllanking (left side) timing (00: +2.6µsec —— 3F: -2.6µsec)	
77h	D1	1	V BLK Half Kill	V blanking half H killer enable	
	D2	1	AKB Ref PLS Pos	AKB reference pulse position (0: normal, 1: 3H delay)	
	D3-D4	2	V BLK Pos	V blanking width (0: normal —— 3: 3H wider, avairable only when AKB Ref PLS Pos="H")	
	D5	1	FBP BLK	H BLK mode select (0: adjustable by H BLK F/R Position, 1: FBP)	
78h	D0-D1	2	A/D Read Page	A/D read page select	
	D2-D3	2	V Sync LPF 1	V sync separation pre-LPF (rise edge) control (0: no filter —— 3: 2µsec)	
	D4-D5	2	V Sync LPF 2	V sync separation pre-LPF (fall edge) control (0: no filter —— 3: 2µsec)	
	D6-D7	2	VREF SEL	A/D reference voltage source select (use Vz)	
79h	D0-D6	7	DCT Vth	DC Transfer threshold level (0: low —— 7F: high)	
7Ah	D0-D4	5	DCT Gain	DC Transfer ratio control (0: 100% —— 1F: 80%)	
7Bh	D0-D7	8	AKB LIM 1	AKB LIM 1	
7Ch	D0-D7	8	AKB LIM 2	AKB LIM 2	
7Dh	D0-D7	8	AKB LIM 3	AKB LIM 3	
7Eh	D0-D7	8	AKB ADD 1	AKB ADD1	
7Fh	D0-D7	8	AKB ADD 2	AKB ADD 2	
80h	D0-D7	8	AKB COMP (R) L	AKB COMP (R) LSB	
81h	D0-D7	8	AKB COMP (G) L	AKB COMP (G) LSB	
82h	D0-D7	8	AKB COMP (B) L	AKB COMP (B) LSB	
83h	D0-D1	2	AKB COMP (R) H	AKB COMP (R) MSB	
	D2-D3	2	AKB COMP (G) H	AKB COMP (G) MSB	
	D4-D5	2	AKB COMP (B) H	AKB COMP (B) MSB	
	D6	1	AKB Enable	AKB enable (0: AKB level is held, 1: AKB level is refleshed at all time)	
	D7	1	V EN OFF	Disenable to reflesh ACC by vertinal rate	
84h	D0-D5	6	A/D D/A Test EN	Test mode select for A/D and D/A (only factory use)	
85h	D0-D5	6	AXIS HYS	AXIS hys	
86h	D0-D5	6	ROM HYS	Rom hys	
	D6-D7	2	AVE SEL AV	Ave sel av	
87h	D0-D6	7	B2 COMP	B2 comp	
88h	D0-D3	4	U In Offset	U input DC offset level (0: –10mV —— F: +10mV)	
	D4-D7	4	V In Offset	V input DC offset level (0: –10mV —— F: +10mV)	
89h	D0	1	ACL ON	ACL enable	
	D1	1	ACL Gain	ACL gain up	
	D2-D3	2	CLK SEL SAR A/D	SAR A/D clock select (0: 2fsc, 1: 4fsc, 2: 12MHz, 3: 6MHz)	
	D4-D5	2	AKB Speed	AKB speed	
	D6-D7	2	AKB SEL	AKB control (0: AKB disenable and available cutoff data, 1: AKB enable, 2: test mode)	
8Ah	D0-D1	2	DS CLK DIV SEL	ΔΣ D/A clock divider select (0: 1/4, 1: 1/2, 2: 1/1, 3: clock off)	
	D2	1	DS CLK Latch ON	ΔΣ D/A clock latched by 4fsc clock enable	
	D3	1	DS CLK Latch Pol	ΔΣ D/A clock latched by 4fsc clock polarity	
	D4-D5	2	VM Gain 2	VM gain2	
	D6	1	V PLS Width	V pulse width (0: standard, 1: wide)	
8Bh	D0-D7	8	AKB SWERR	AKB error detect threshold	V Latch
8Ch	D0-D7	8	AKB ERRC	AKB error detect time	V Latch
8Dh	D0-D7	8	AKB SWPON	AKB power on threshold	V Latch
8Eh	D0-D7	8	AKB PWERRC	AKB power on time	V Latch

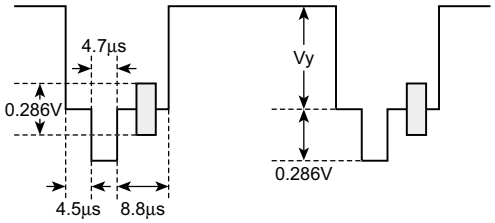
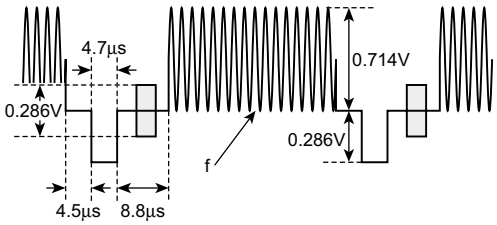
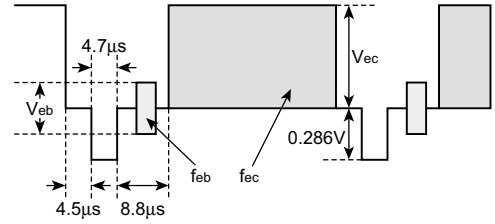
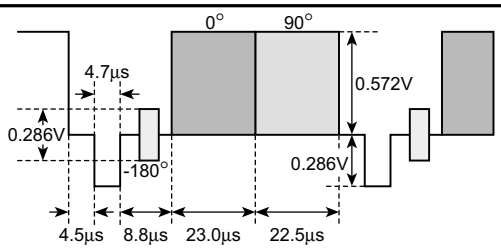
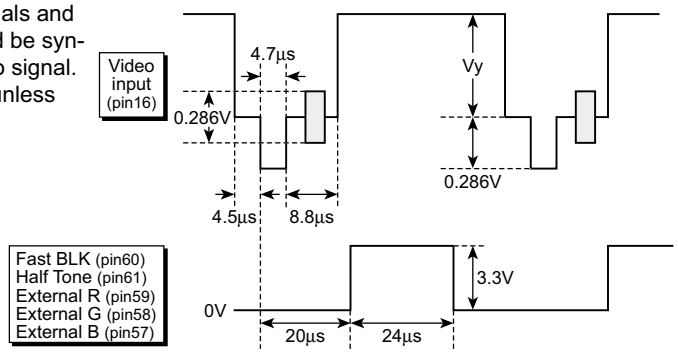
Sub address	Data	Bit	Function	Description	Note
90h	D2	1	DETNZ	Noise detector output	Read
	D4	1	AKB NG	AKB NG output	Read
	D5	1	AKB END	AKB end output	Read
	D6	1	S Det	S (Y/C) input detector output	Read
	D7	1	H COIN	Horizontal coincidence output	Read
91h	D0	1	K MONI	C-pro Killer detector output	Read
	D2	1	MV 180	Macrovision detector output	Read
	D3	1	Still Det	VCR still detector outut	Read
	D4	1	B/W Out	Burst PLL Killer detector output	Read
	D5	1	V COIN	Vertical coincidence output	Read
	D6	1	Killer Status	Color / Killer status output	Read
	D7	9	B2 ROM	B2 ROM data output	Read
92h	D0-D7				
93h	D0-D7	10	AKB A/D (R)	AKB A/D (R) output	Read
94h	D6-D7				
	D3-D4	2	C Gain	Analog ACC amp status	Read
	D5	1	AKB New (R)	AKB New (R) output	Read
95h	D0-D7	10	AKB A/D (G)	AKB A/D (G) output	Read
96h	D6-D7				
	D5	1	AKB New (G)	AKB New (G) output	Read
97h	D0-D7	10	AKB A/D (B)	AKB A/D (B) output	Read
98h	D6-D7				
	D5	1	AKB New (B)	AKB New (B) output	Read
99h	D0-D7	8	Y A/D	Y A/D output monitoring	Read
9Ah	D0-D7	8	C A/D	C A/D output monitoring	Read
9Bh	D6-D7	4	0001	Product identification	Read

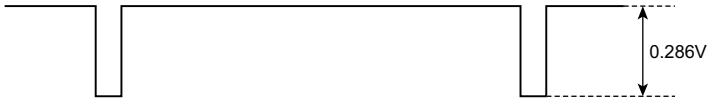
Electrical characteristics (ASIC part)

1. Test circuit



2. Input Signal

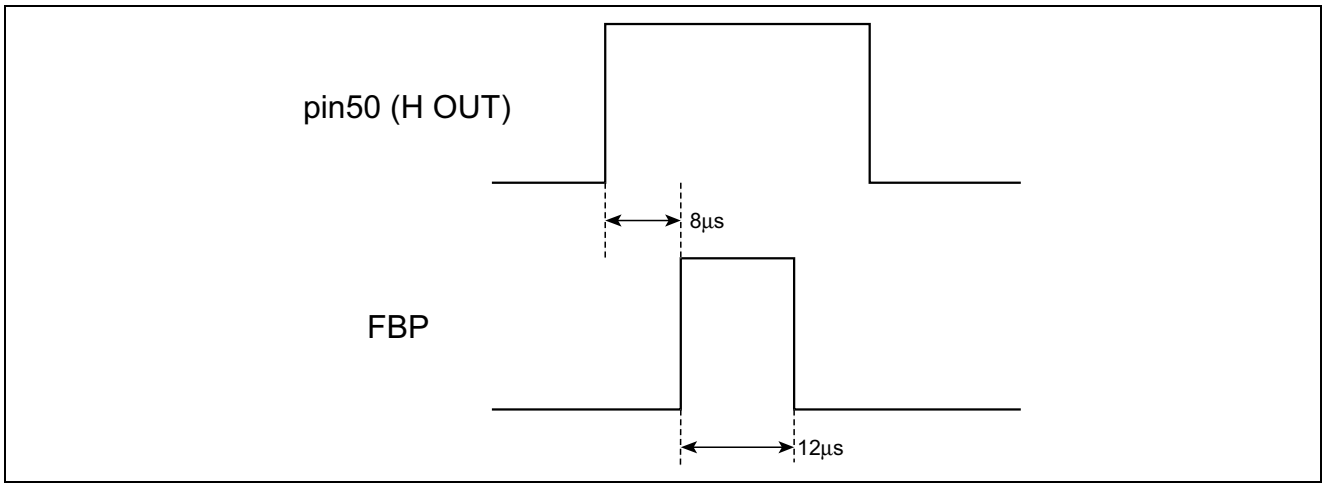
SG No.	Input signal (value at pin terminal is 50)
SG.A	NTSC system standard video signal. APL can be varied. Vy=0.714V (APL 100%), unless otherwise noted. The vertical signal should be interlaced at 60Hz. 
SG.B	The amplitude and frequency of Luminance signal can be varied by signal SG.A. The typical amplitude is 0.714V_{p-p}. The frequency of Luminance, (f) as stated in test. 
SG.C	NTSC system mono-chroma video signal. The amplitude and frequency of burst part and chroma part can be varied. The vertical signal should be interlaced at 60Hz. (Standard condition: V_y=0.286V V_{eb}=0.286V, V_{ec}=0.572V f_{eb}=f_{ec}=3.576545MHz) 
SG.D	NTSC system 2-phase chroma video signal. The vertical signal should be interlaced at 60Hz. (Standard condition: V_y=0.286V V_{eb}=0.286V, Vec=0.572V P_{eb}=-180°, P_{ec}1=0û, P_{ec}2=90°) 
SG.E	NTSC system rainbow color bar video signal. The vertical signal should be interlaced at 60Hz.
SG.F	External RGB (OSD) signals and falt blanking signal should be synchronized with input video signal. Vy=0.714V (APL100%), unless otherwise noted. 

SG No.	Input signal (value at pin terminal is 50Ω)
SG.G	Duty cycle 90%, frequency can be varied, amplitude can be varied (typ. 0.286V_{p-p}) 
SG.H	Duty cycle can be varied (typ. 95%), frequency can be varied (typ. 0.286V_{p-p}). 

3. Setup instruction for evaluation PCB

3.1 Horizontal blanking pulse adjustment

The timing and pulse width of the horizontal blanking pulse should be as shown in the following figure by adjusting the variable resistor of the single shot multi vibrator.



The variable resistor at pin15 of TTL IC 'M74LS221P' is used to fix the timing at 8s and that at pin7 is used to fix the pulse width at 12µs.

3.2. H VCO adjustment

Before measurement of M65582MF, HVCO must be adjusted by the following procedure.

Set the frequency at pin50 (H OUT) to about 15.734kHz by adjusting I^2C-Bus data of H VCO control (51H D0-D7).

4. Electric characteristics

(Ta=25°C, Vdd=5.0, 3.3V)

Parameter	Symbol	Input signal		Test points	Limits			Unit	Remarks
		Pins	SG		Max.	Typ.	Min.		
Standard conditions	DC								pin48 = 1.65V
3.3V supply current	ICC33	—	—	A	140	180	220	mA	Supply of ASIC
A/D reference voltage (Top)	VRT	—	—	22	1.6	1.7	1.8	V	
A/D reference voltage (Bottom)	VRB	—	—	24	0.4	0.5	0.6	V	

Parameter	Symbol	Input signal		Test points	Limits			Unit	Remarks
		Pins	SG		Max.	Typ.	Min.		
Standard conditions of video parameter	Y								pin48 = 1.65V
CVBS OUT output level	2AG	16,21, 23	SG.A	15	1.8	2.0	2.2	Vpp	
Luminance standard output level	YOUT	16,21, 23	SG.A	31,33, 35	560	700	840	mVpp	
Video frequency characteristics	FY	16,21, 23	SG.B	31,33, 35	–5	–2	1	dB	f=5MHz
VM output level	VM	16	SG.B	24	520	650	780	mVpp	f=3.58MHz

Parameter	Symbol	Input signal		Test points	Limits			Unit	Remarks
		Pins	SG		Max.	Typ.	Min.		
Standard conditions of chroma parameter	C								pin48 = 1.65V
ACC characteristic 1	ACC1	16	SG.C	31	–3	0	3	dB	Veb, Vec : +6dB of typical input level
ACC characteristic 2	ACC2	16	SG.C	31	–3	0	3	dB	Veb, Vec : -20dB of typical input level
APC pull-in range (upper)	APCU	16	SG.C	31	–300	—	—	Hz	feb=fec : variable
APC pull-in range (lower)	APCL	16	SG.C	31	—	—	300	Hz	feb=fec : variable
Demodulation phase angle	DEMP	16	SG.D	31,35	85	90	95	deg	

Symbol	Bus condition (Input initial data, unless otherwise noted. Refer to section 8.1 for the standard data.)																															
	00H	01H	02H	04H	05H	06H	08H	09H	0AH	0BH	0CH	0DH	0EH	10H	12H	16H	17H	18H	19H	1AH	1BH	32H	3AH	3BH	51H	65H	66H	67H	68H	69H	79H	7AH	83H	89H
DC	00	08	6E	10	0F	6F	40	40	40	20	A0	20	80	02	80	00	C0	00	C0	00	C0	05	20	20	adj	00	83	00	8F	06	05	00	2A	00
ICC33																																		
VRT																																		
VRB																																		

Symbol	Bus condition (Input initial data, unless otherwise noted. Refer to section 8.1 for the standard data.)																															
	00H	01H	02H	04H	05H	06H	08H	09H	0AH	0BH	0CH	0DH	0EH	10H	12H	16H	17H	18H	19H	1AH	1BH	32H	3AH	3BH	51H	65H	66H	67H	68H	69H	79H	7AH	83H	89H
Y	00	08	6E	10	0F	6F	40	40	40	20	A0	20	80	02	80	00	C0	00	C0	00	C0	05	20	20	adj	00	83	00	8F	06	05	00	2A	00
2AG								00																										
YOUT								00																										
FY								00																										
VM								00																					FF					

Symbol	Bus condition (Input initial data, unless otherwise noted. Refer to section 8.1 for the standard data.)																															
	00H	01H	02H	03H	08H	09H	0AH	0BH	0CH	0DH	0EH	10H	16H	17H	18H	19H	1AH	1BH	32H	41H	42H	45H	46H	47H	48H	49H	4CH	4DH	4EH	50H	51H	5DH	83H	89H
C	00	08	6E	08	40	40	40	20	A0	20	80	02	00	C0	00	C0	00	C0	05	01	C0	30	08	4B	00	00	91	04	14	71	adj	80	2A	00
ACC1																																83		
ACC2																																83		
APCU																																83		
APCL																																83		
DEMP																																		

Parameter	Symbol	Input signal		Test points	Limits			Unit	Remarks
		Pins	SG		Max.	Typ.	Min.		
Standard conditions of RGB parameter	RGB								pin48 = 1.65V
Ouput Pedestal voltage	VPED	16	SG.A	31,33, 35	2.7	3.0	3.3	V	Vy = 0.0V
Output Blanking voltage	VBLK	16	SG.A	31,33, 35	3.1	—	3.3	V	Vy = 0.0V
Matrix ratio R/B	MTXR	16	SG.E	31,35	0.8	1.0	1.2	—	
Matrix ratio G/B	MTXB	16	SG.E	31,35	0.2	0.3	0.4	—	
AKB reference pulse output level	AKBP	16	SG.A	31,33, 35	200	300	400	mV	Vy = 0.0V
OSD output level	OSD	16,57, 58,59	SG.F	31,33, 35	480	600	720	mVpp	

Parameter	Symbol	Input signal		Test points	Limits			Unit	Remarks
		Pins	SG		Max.	Typ.	Min.		
Standard conditions of deflection parameter	DEF								pin48 = 1.65V
Horizontal free-running frequency	FH	—	—	50	15.48	15.73	15.98	kHz	
Horizontal pull-in range (upper)	FPHU	16	SG.G	50	600	—	—	Hz	Vary frequency of input signal
Horizontal pull-in range (lower)	FPHL	16	SG.G	50	—	—	–600	Hz	Vary frequency of input signal
Horizontal pulse amplitude	HOUT	16	SG.A	50	2.7	3.0	3.3	V	
Horizontal pulse width	HPTW	16	SG.A	50	17	19	22	µsec	
Vertical free-running frequency	FV	—	—	50	57	60	63	Hz	
Vertical pull-in range (upper)	FPVU	16	SG.H	44,45	—	—	64	Hz	Vary frequency of input signal
Vertical pull-in range (lower)	FPVL	51	SG.H	44,45	56	—	—	Hz	Vary frequency of input signal
Vertical output level	VOUT	16	SG.A	44,45	1.0	1.2	1.4	Vpp	
Vertical ramp output DC voltage	VDC	16	SG.A	44,45	1.5	1.7	1.9	V	
E-W output level	EWOUT	16	SG.A	47	0.3	0.4	0.5	Vpp	
E-W output DC voltage	EWDC	16	SG.A	47	0.95	1.15	1.35	V	

Symbol	Bus condition (Input initial data, unless otherwise noted. Refer to section 8.1 for the standard data.)																															
	00H	01H	02H	04H	05H	08H	09H	0AH	0BH	0CH	0DH	0EH	10H	12H	16H	17H	18H	19H	1AH	1BH	32H	38H	3AH	3BH	51H	65H	66H	67H	68H	69H	79H	7AH	83H	89H
RGB	00	08	6E	10	0F	40	40	40	20	A0	20	80	02	80	00	C0	00	C0	00	C0	05	A0	20	20	adj	00	83	00	8F	06	05	00	2A	00
VPED								00																										
VBLK								00																										
MTXR								00																										
MTXB								00																										
AKBP								00														BF												
OSD								00																										

Symbol	Bus condition (Input initial data, unless otherwise noted. Refer to section 8.1 for the standard data.)																															
	00H	01H	02H	05H	0FH	13H	14H	15H	32H	34H	38H	46H	4CH	4FH	50H	51H	52H	53H	54H	5DH	6AH	6BH	6CH	6DH	6EH	6FH	71H	72H	73H	74H	75H	76H	77H	8AH
DEF	00	08	6E	0F	20	02	20	20	05	45	A0	08	91	60	71	adj	00	66	29	80	00	20	20	20	20	20	20	20	20	88	80	80	00	44
FH																																		
FPHU																																		
FPHL																																		
HOUT																																		
HPTW																																		
FV																																		
FPVU																																		
FPVL																																		
VOUT																																		
VDC																																		
EWOUT																																		
EWDC																																		

5. Electrical characteristics test method

Y BLOCK

2AG: CVBS OUT output level

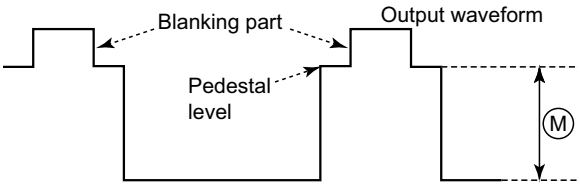
1. Input SG.A to pin 16.
2. Measure the amplitude (peak to peak) at pin 15.

Note: Use sub address 01H to select TV1 IN, TV2 IN, TV3 IN, Y(Y/C) IN, Y(YUV) IN.

YOUT: Video standard output level

1. Input SG.A to pin 16.
2. Measure the amplitude (pedestal to top part) at pins 31, 33 and 35.

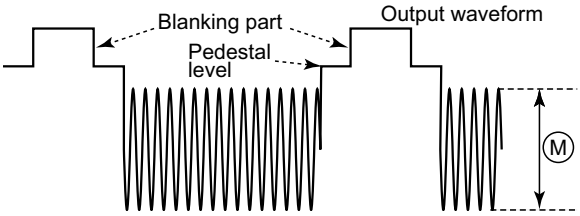
Note: Use sub address 01H to select TV1 IN, TV2 IN, TV3 IN, Y(Y/C) IN, Y(YUV) IN.



FY: Video frequency characteristic

1. Input SG.B (f=5MHz, 0.714Vp-p) to pin 16.
2. Measure the amplitude (peak to peak) except blanking part at pins 31, 33 and 35. The amplitude are defined as YB.
3. FY is defined as follows:

$$FY = 20 \log \frac{YB\ (V_{p\text{-}p})}{YOUT\ (V_{p\text{-}p})}$$



VM: VM output level

1. Input SG.B (f=3.58MHz, 0.714Vp-p) to pin 16.
2. Measure the amplitude (peak to peak) at pin 29.

C BLOCK

ACC1: ACC characteristic 1

1. Input SG.C (fec=feb+50kHz, Veb, Vec; standard level) to pin 16.
2. Measure the amplitude at pin 31. The amplitude is defined as CnorR.
3. And then, input SG.C (fec=feb+50kHz, Veb, Vec; +6dB) to pin 16.
4. Measure the amplitude at pin 31.
5. ACC1 is defined as follows:

$$ACC1 = 20 \log \frac{\text{measured value}\ (V_{p\text{-}p})}{CnorR\ (V_{p\text{-}p})}$$

ACC2: ACC characteristic 2

1. Input SG.C (fec=feb+50kHz, Veb, Vec; standard level) to pin 16.
2. Measure the amplitude at pin 31. The amplitude is defined as CnorR.
3. And then, input SG.C (fec=feb+50kHz, Veb, Vec; -20dB) to pin 16.
4. Measure the amplitude at pin 31.
5. ACC1 is defined as follows:

$$ACC2 = 20 \log \frac{\text{measured value } (V_{p\text{-}p})}{\text{CnorR } (V_{p\text{-}p})}$$

APCU: APC pull-in range (Upper)

APCL: APC pull-in range (Lower)

1. Input SG.C (fec=feb=3.579545MHz) to pin 16.
2. Increase the frequency until the waveform at pin 37 and input signal are asynchronous. And then, decrease the frequency and note the point when the waveform at pin 37 and input signal are synchronous; fU.
3. Decrease the frequency until the waveform at pin 37 and input signal are asynchronous. And then, increase the frequency and note the point when the waveform and input signal are synchronous; fL.
4. APCU and APCL are defined as follows:

$$APCU = fU - 3579545 \text{ (Hz)}$$

$$APCL = fL - 3579545 \text{ (Hz)}$$

DEMP: Demodulation phase angle

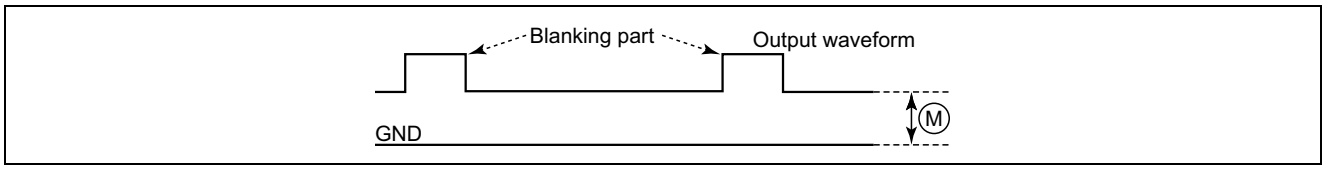
1. Input SG.D to pin 16.
2. Measure the amplitude at pin 31 (R-Y) and pin 35 (B-Y), and defined as VR-Y and VB-Y respectively.
3. DEMP is defined as follows:

$$DEMP = 180 - \text{Cos}^{-1} \frac{V_{R\text{-}Y} \ (mV_{p\text{-}p})}{V_{B\text{-}Y} \ (mV_{p\text{-}p})} \text{ (deg)}$$

RGB BLOCK

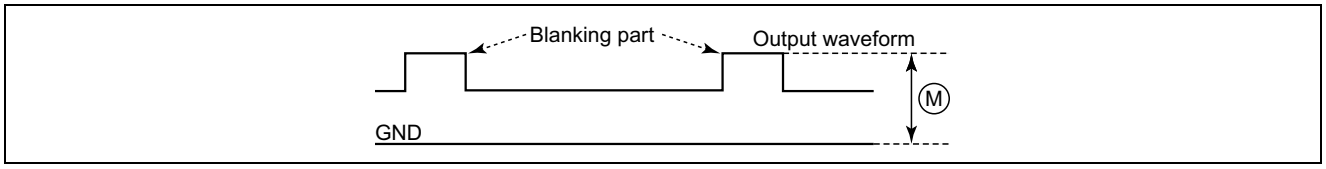
VPED: Output pedestal voltage

1. Input SG.A (Vy=0V) to pin 16.
2. Measure the voltage of pedestal part at pins 31, 33 and 35.



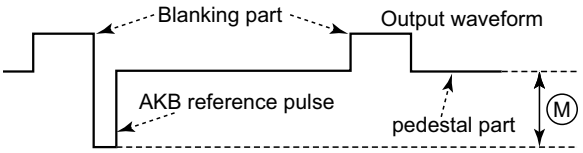
VBLK: Output blanking voltage

1. Input SG.A (Vy=0V) to pin 16.
2. Measure the voltage of blanking part at pins 31, 33 and 35.



AKBP: AKB reference pulse output level

1. Input SG.A (Vy=0V) to pin 16.
2. Measure the amplitude of AKB reference pulse at pins 31, 33 and 35.



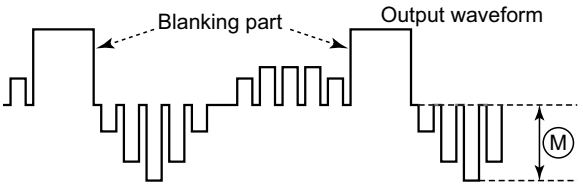
MTXRB: Matrix ratio R/B

MTXGB: Matrix ratio G/B

1. Input SG.E (rainbow color bar signal) to pin 16.
2. Measure the amplitude VR, VG and VB at pins 31, 33 and 35, respectively.
3. MTXRB and MTXGB are defined as follows:

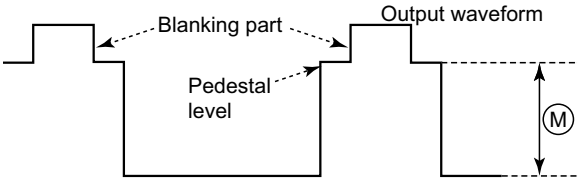
$$MTXRB = \frac{V_R\ (mV_{p\text{-}p})}{V_B\ (mV_{p\text{-}p})}$$

$$MTXGB = \frac{V_G\ (mV_{p\text{-}p})}{V_B\ (mV_{p\text{-}p})}$$



OSD: OSD output level

1. Input SG.F to pins 16, 57, 58, 59 and 60.
2. Measure the output amplitude at pins 31, 33 and 35 except that at blanking part.



DEFLECTION BLOCK

FH: Horizontal free-running frequency

1. Measure the output frequency at pin 50 when no signal is input.

FHUP: H-free-up frequency

1. Measure the output frequency at pin 50 when I 2 C bus data of H-free up (Sub 13h D0) is set '1'.no signal is input.
2. FHUP is defined as follows:

FHUP = measured value(Hz) – FH (Hz)

FPHU: Horizontal pull-in range (Upper)

FPHL: Horizontal pull-in range (Lower)

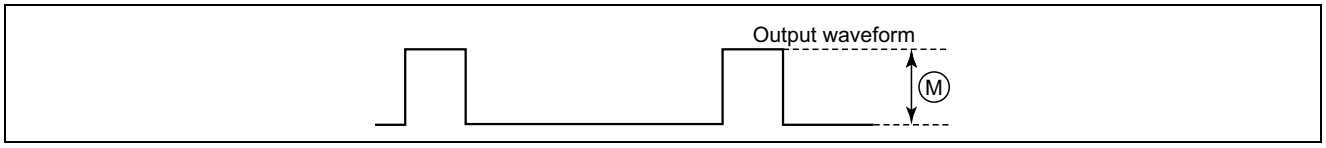
1. Input SG.G to pin 16.
2. Change the frequency of SG.G, and measure the frequency when the output signal at pin 50 and the input signal are synchronous. The horizontal pull-in range is measured by comparing with the horizontal frequency of video signal.
3. FPHU and FPHL are defined as follows:

FPHU = measured value (Hz) – 15734 (Hz)

FPHL = measured value (Hz) – 15734 (Hz)

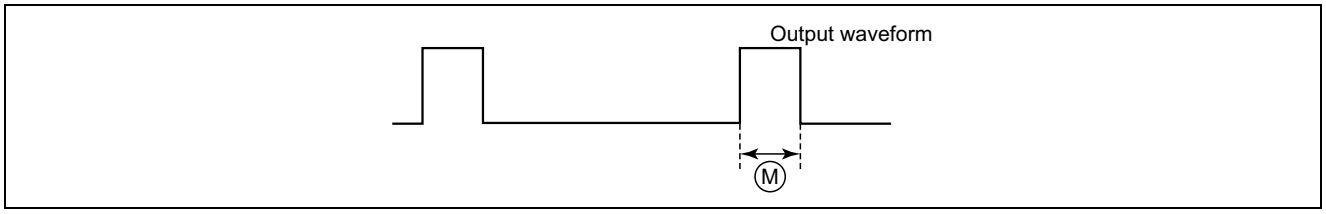
HOUT: Horizontal pulse amplitude

1. Input SG.A to pin 16.
2. Measure the amplitude at pin 50.



HPTW: Horizontal pulse width

1. Input SG.A to pin 16.
2. Measure the pulse width of output signal at pin 50.



FV: Vertical free-running frequency

1. Measure the output frequency at pins 44 and 45 when no signal is input.

FPVU: Vertical pull-in range (Upper)

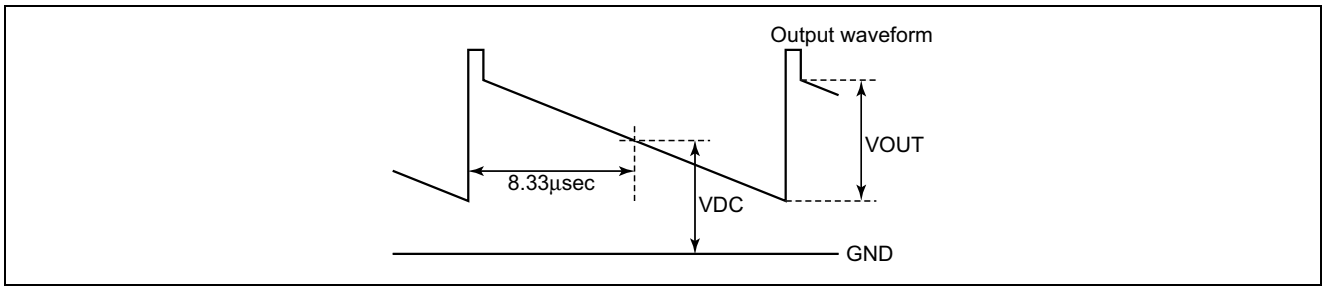
FPVL: Vertical pull-in range (Lower)

1. Input SG.H to pin 16.
2. Change the vertical frequency of SG.H, and measure the frequency when the output signal at pins 44 and 45 and the input signal are synchronous.

VOUT: Vertical ramp output level

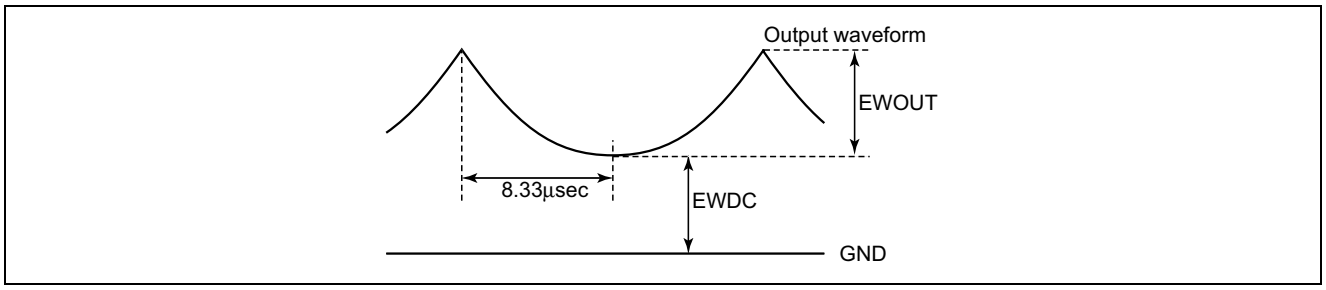
VDC: Vertical ramp output DC voltage

1. Input SG.A to pin 16.
2. Measure the output amplitude at pin 45; VOUT.
3. Measure the DC volatge at pin 45 when the timing is 8.33µsec from start point of vertical ramp; VDC.



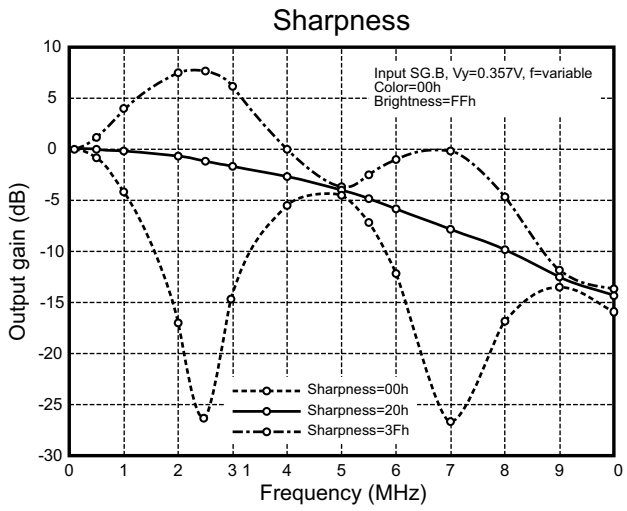
EWOUT: E-W output level

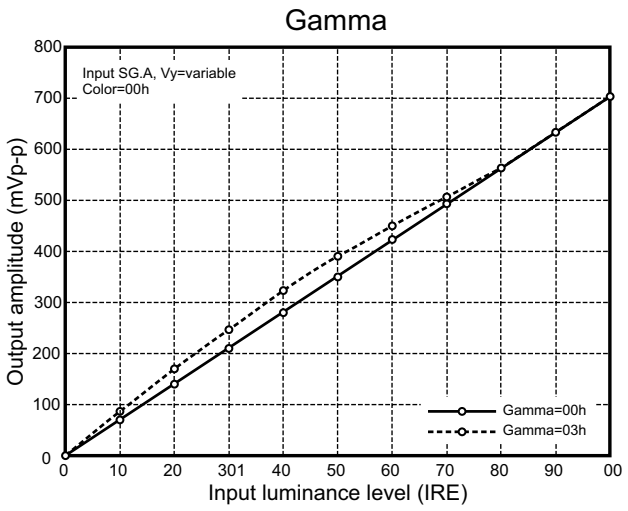
1. Input SG.A to pin 16.
2. Measure the output amplitude at pin 47; EWOUT.
3. Measure the DC volatge at pin 47 when the timing is 8.33µsec from start point of E-W; EWDC.

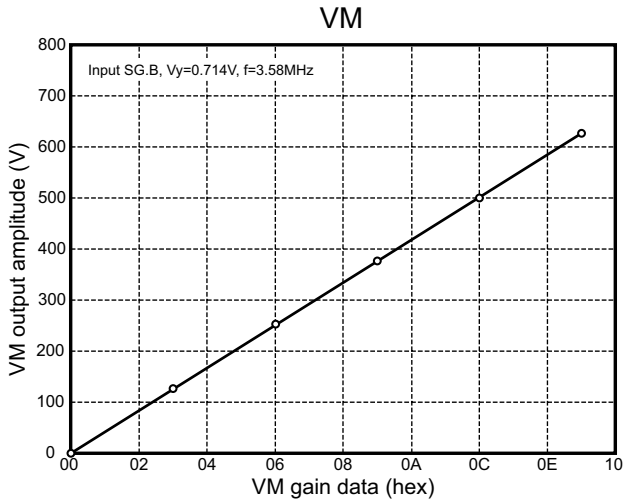


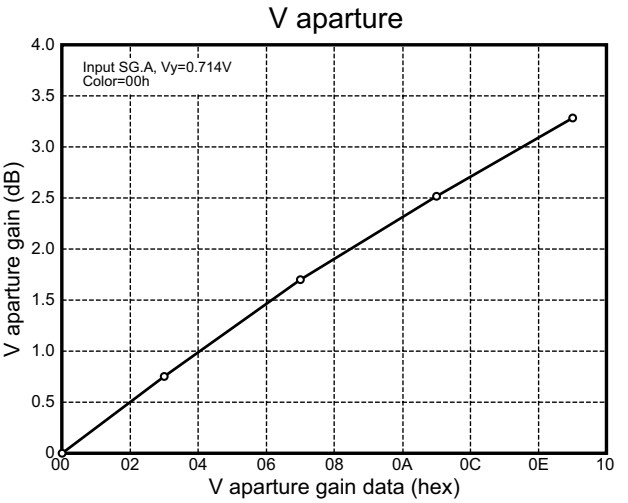
6. Example of the typical characteristics

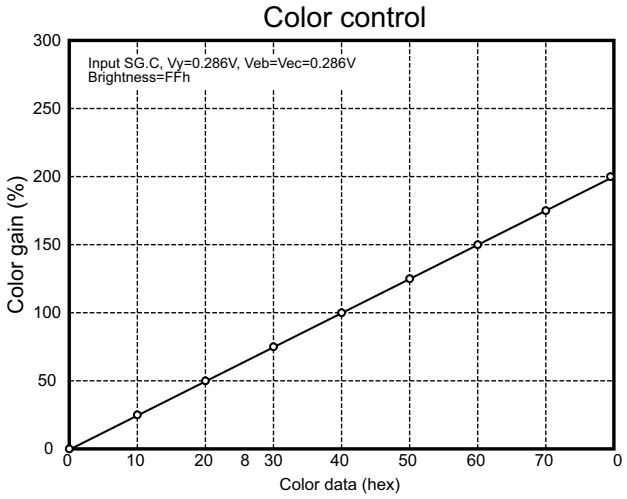
Note: 1. These characteristics are for reference, and not guaranteed by shipment test.
2. Bus condition is standard, unless otherwise noted (Refer to page 8).

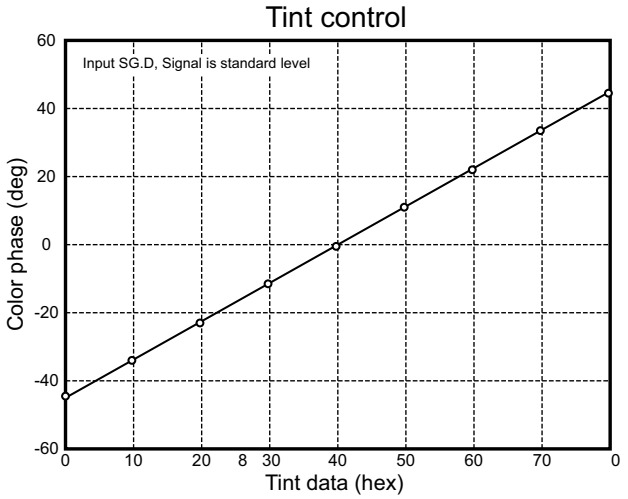




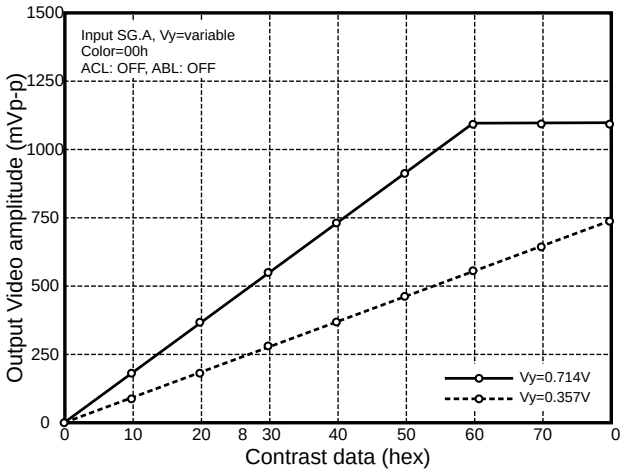




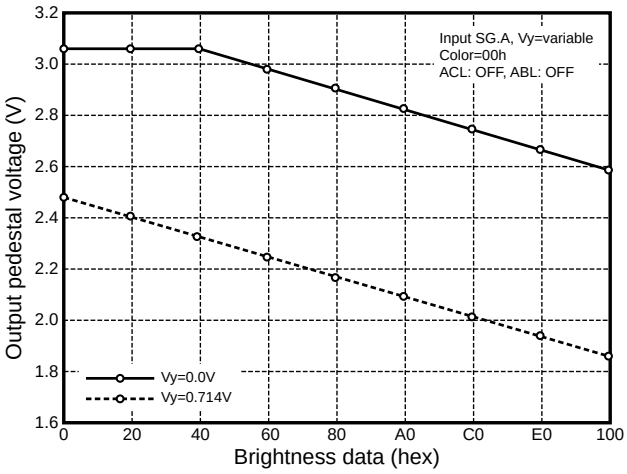




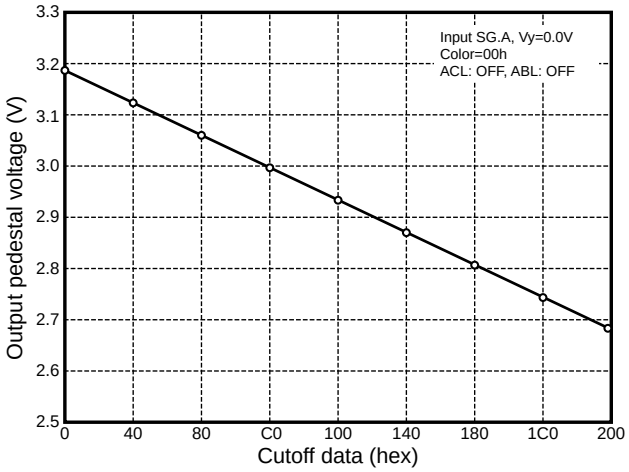
Contrast control



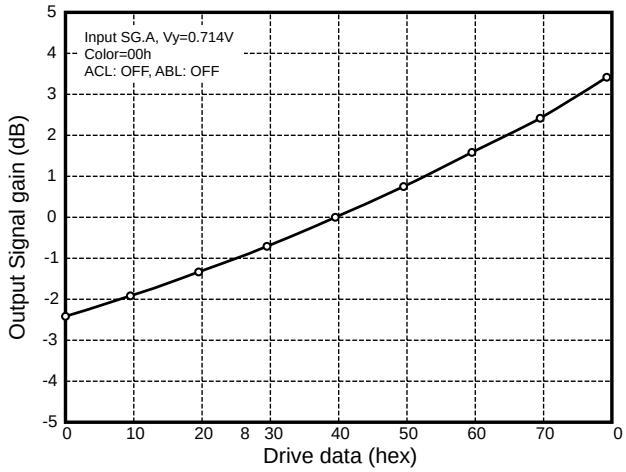
Brightness control



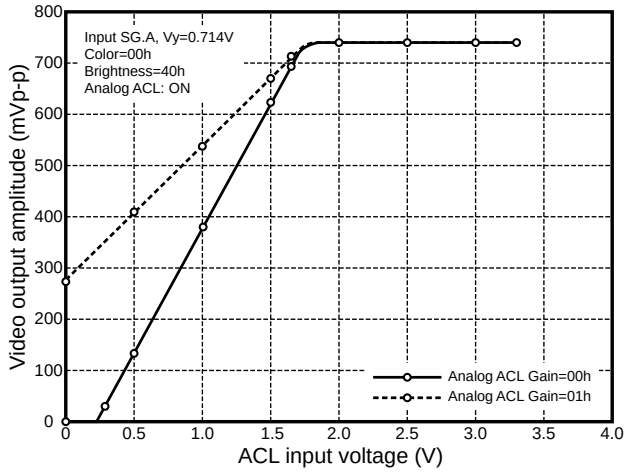
Cutoff control



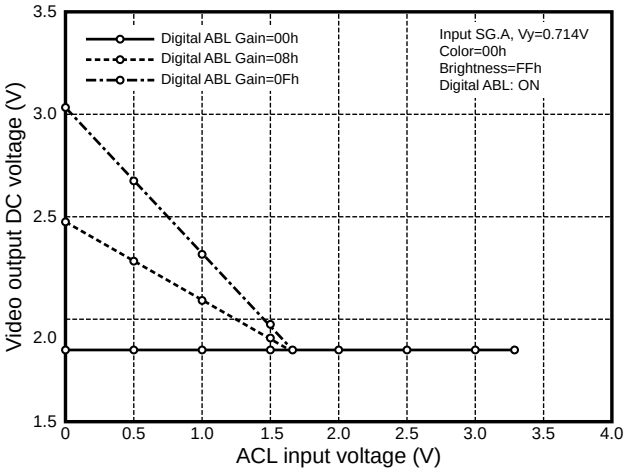
Drive control



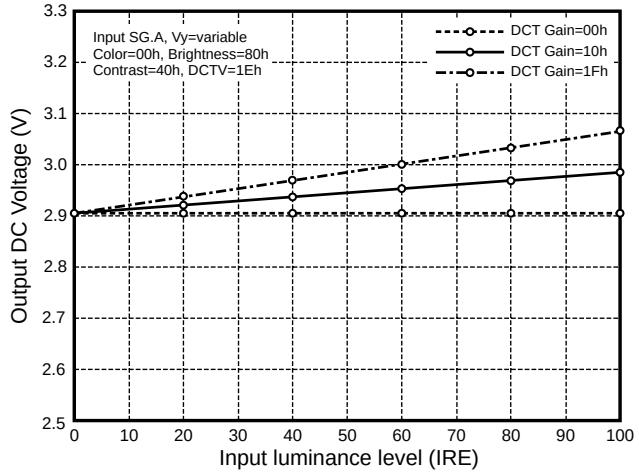
ACL characteristic



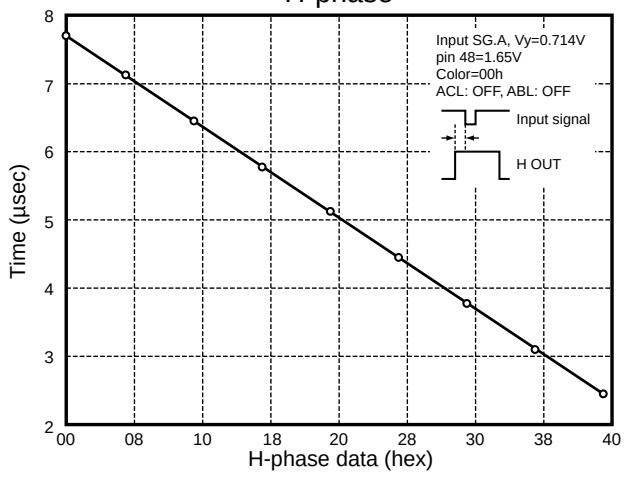
ABL characteristic



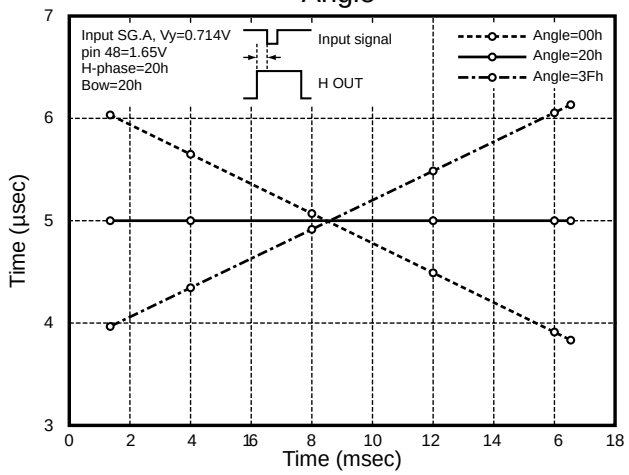
DCT



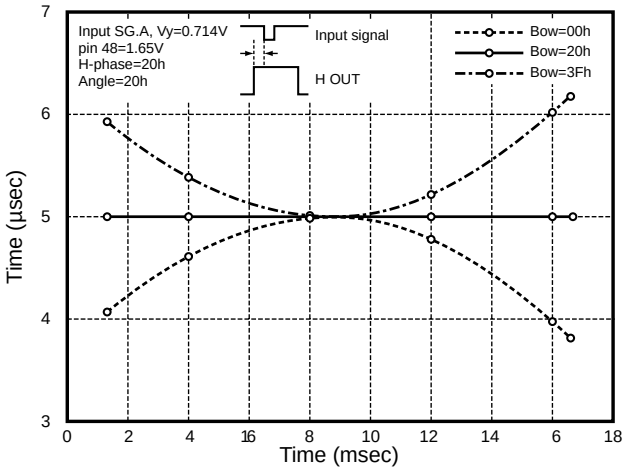
H-phase



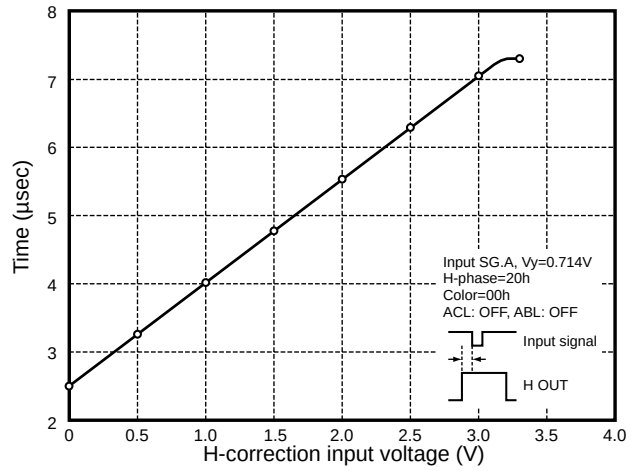
Angle



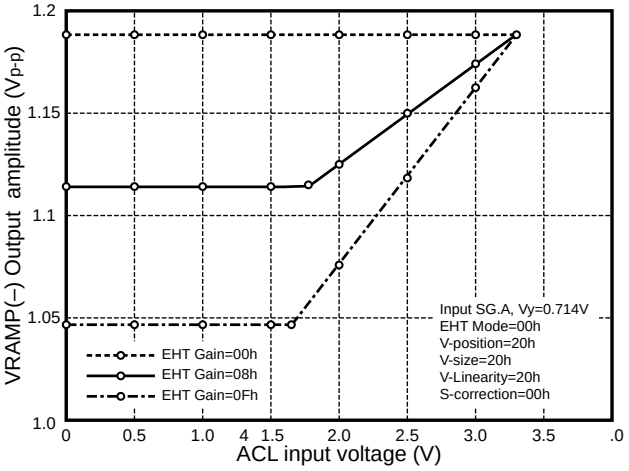
Bow



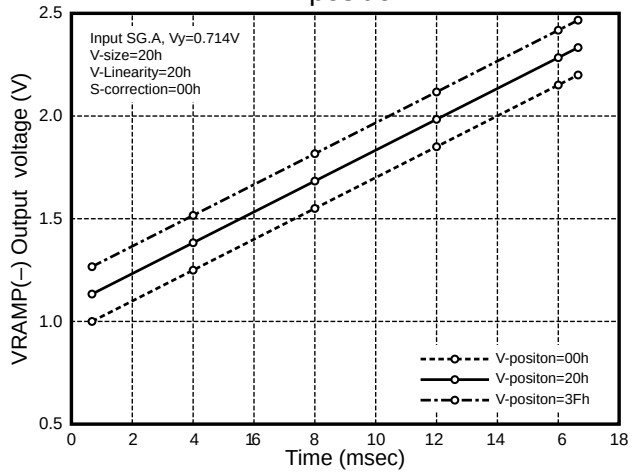
H-correction



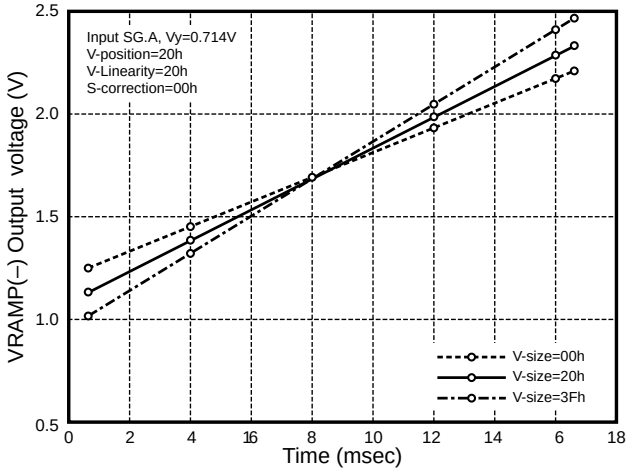
EHT



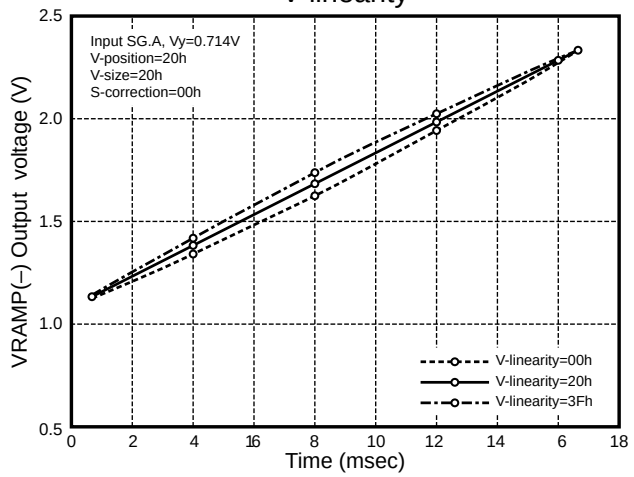
V-position



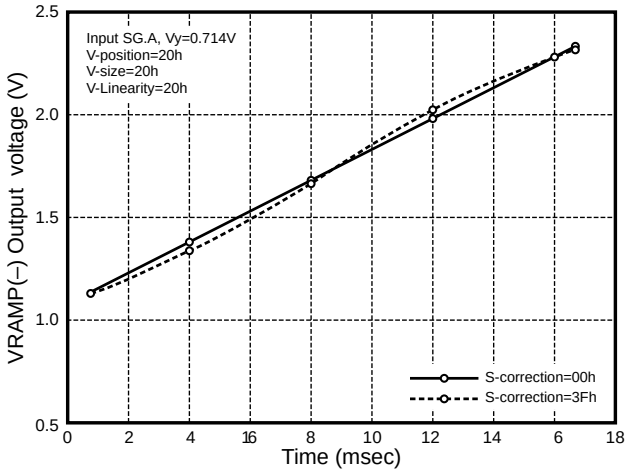
V-size



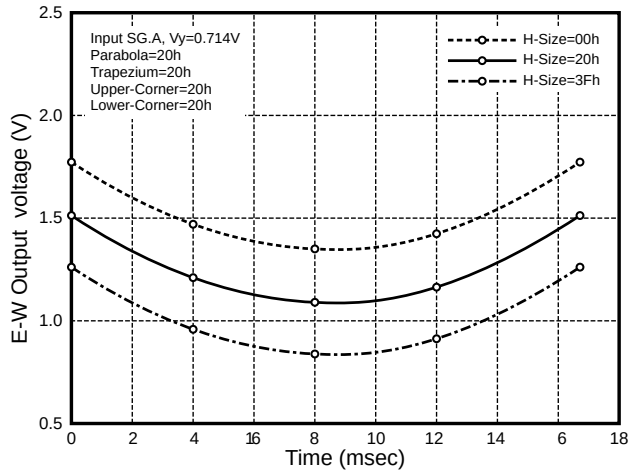
V-linearity



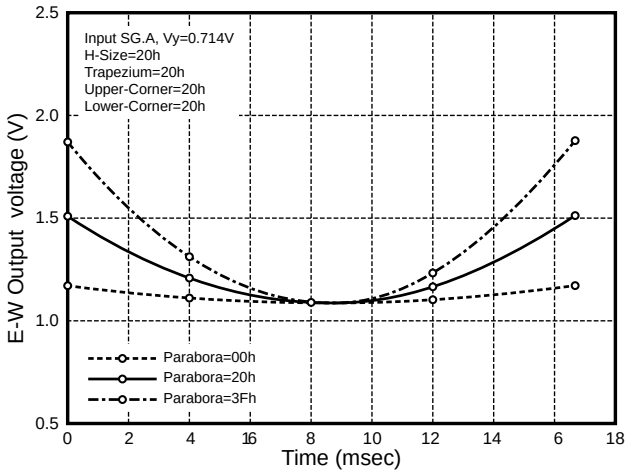
S-correction

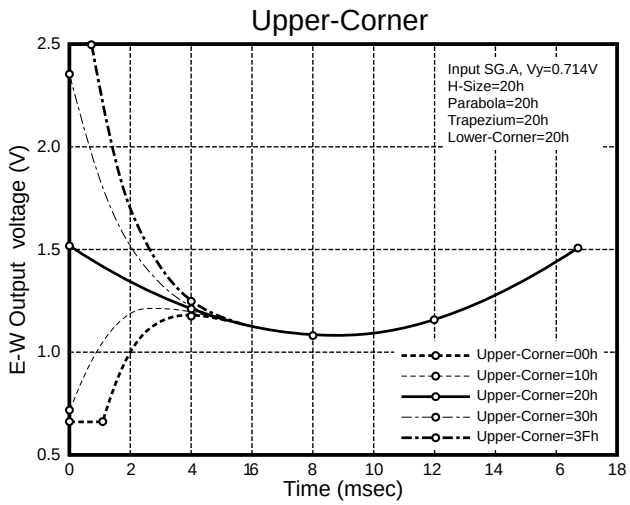


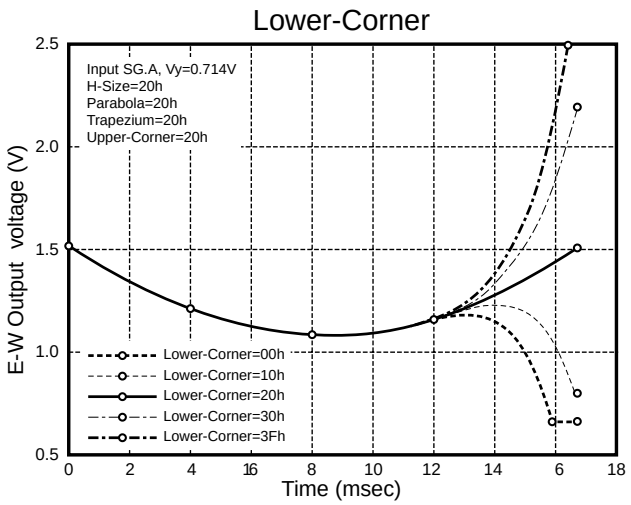
H-Size

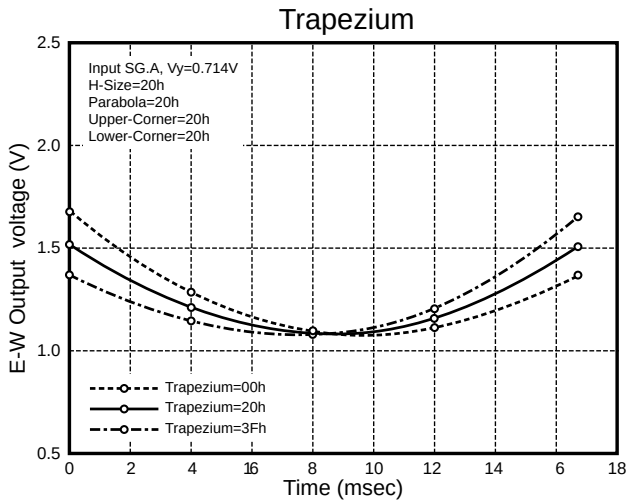


Parabola




Upper-Corner
Input SG.A, Vy=0.714V
H-Size=20h
Parabola=20h
Trapezium=20h
Lower-Corner=20h
Upper-Corner=00h
Upper-Corner=10h
Upper-Corner=20h
Upper-Corner=30h
Upper-Corner=3Fh
E-W Output voltage (V)
Time (msec)


Lower-Corner
Input SG.A, Vy=0.714V
H-Size=20h
Parabola=20h
Trapezium=20h
Upper-Corner=20h
Lower-Corner=00h
Lower-Corner=10h
Lower-Corner=20h
Lower-Corner=30h
Lower-Corner=3Fh
E-W Output voltage (V)
Time (msec)


Trapezium
Input SG.A, Vy=0.714V
H-Size=20h
Parabola=20h
Upper-Corner=20h
Lower-Corner=20h
Trapezium=00h
Trapezium=20h
Trapezium=3Fh
E-W Output voltage (V)
Time (msec)

Electrical characteristics (MCU part)

1. Electrical characteristics

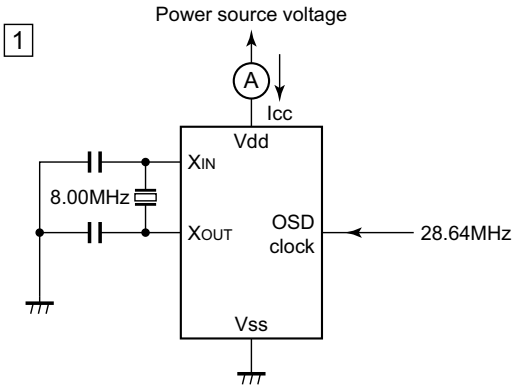
(VDD=55%, VSS=0V, f(XIN)=8MHz, Ta=-20°C to 70°C, unless otherwise noted)

Parameter		Symbol	Limits Min.	Typ.	Max.	Unit	Test conditions		Test Circuit
Power source current	System operation	Icc		15	30	mA	VDD=5.25V, f(XIN)-8MHz	OSD OFF Data slicer OFF	1
				30	45			OSD ON	
				60	200	µA	VDD=5.25V, f(XIN)=0, f(XCIN)=32kHz, OSD OFF, Data slicer OFF, Low-power dissipation mode set (CM5="0", CM6="1")		
	Wait mode			2	4	mA	VDD=5.25V, f(XIN)-8MHz		
				25	100	µA	VDD=5.25V, f(XIN)=0, f(XCIN)=32kHz, OSD OFF, Data slicer OFF, Low-power dissipation mode set (CM5="0", CM6="1")		
				1	10		VDD=5.25V, f(XIN)=0, f(XCIN)=0		
HIGH output voltage P10-P16, P20-P27, P40-P45		VOH	2.4			V	VDD=4.75V, IOH=-0.5mA		2
LOW output voltage P00-P07,P10, P15, P16, P20-P27, P40-P45		VOL			0.4	V	VDD=4.75V, IOH=0.5mA		
LOW output voltage P11-P14,					0.4		VDD=4.75V	IOL=3mA	
					0.6			IOL=6mA	
Hysteresis (See note 1) RESET, INT1, INT2, INT3, TIM2, TIM3, SIN, SCLK, SCL1, SCL2, SDA1, SDA2		VT+-VT-			1.3	V	VDD=5.0V		3
HIGH input leak current P00-P07, P10-P16, P20-P27, P40-P45, RESET		IIZH			5	µA	VDD=5.25V, VI=5.25V		4
LOW input leak current P00-P07, P10-P16, P20-P27, P40-P45, RESET		IIZL			5	µA	VDD=5.25V, VI=0V		4
I^2C-BUS·BUS switch connection resistor (between SCL1 and SCL2, SDA1 and SDA2)		RBS			130	Ω	VDD=4.75V		5

Notes : 1. P06, P07, P23-P25 have the hysteresis when these pins are used as interrupt input pins or timer input pins. P11-P14
have the hysteresis when these pins are used as multi-master I^2C-BUS interface ports. P20-P22 have the hysteresis when these pins are used as serial I/O pins.

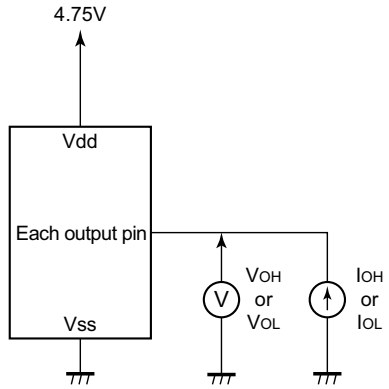
2. Test circuit

1



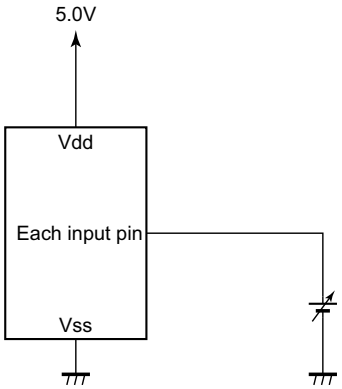
Pin Vdd is made the operation state and is measured the circuit, with a ceramic resonator.

2

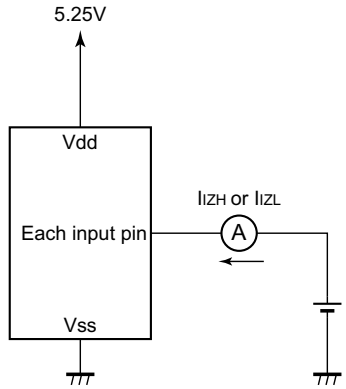


After setting each output pin to HIGH level when measuring V_{OH} and to LOW level when measuring V_{OL}, each pin is measured

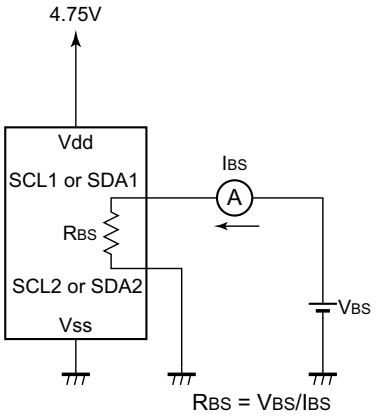
3



4



5

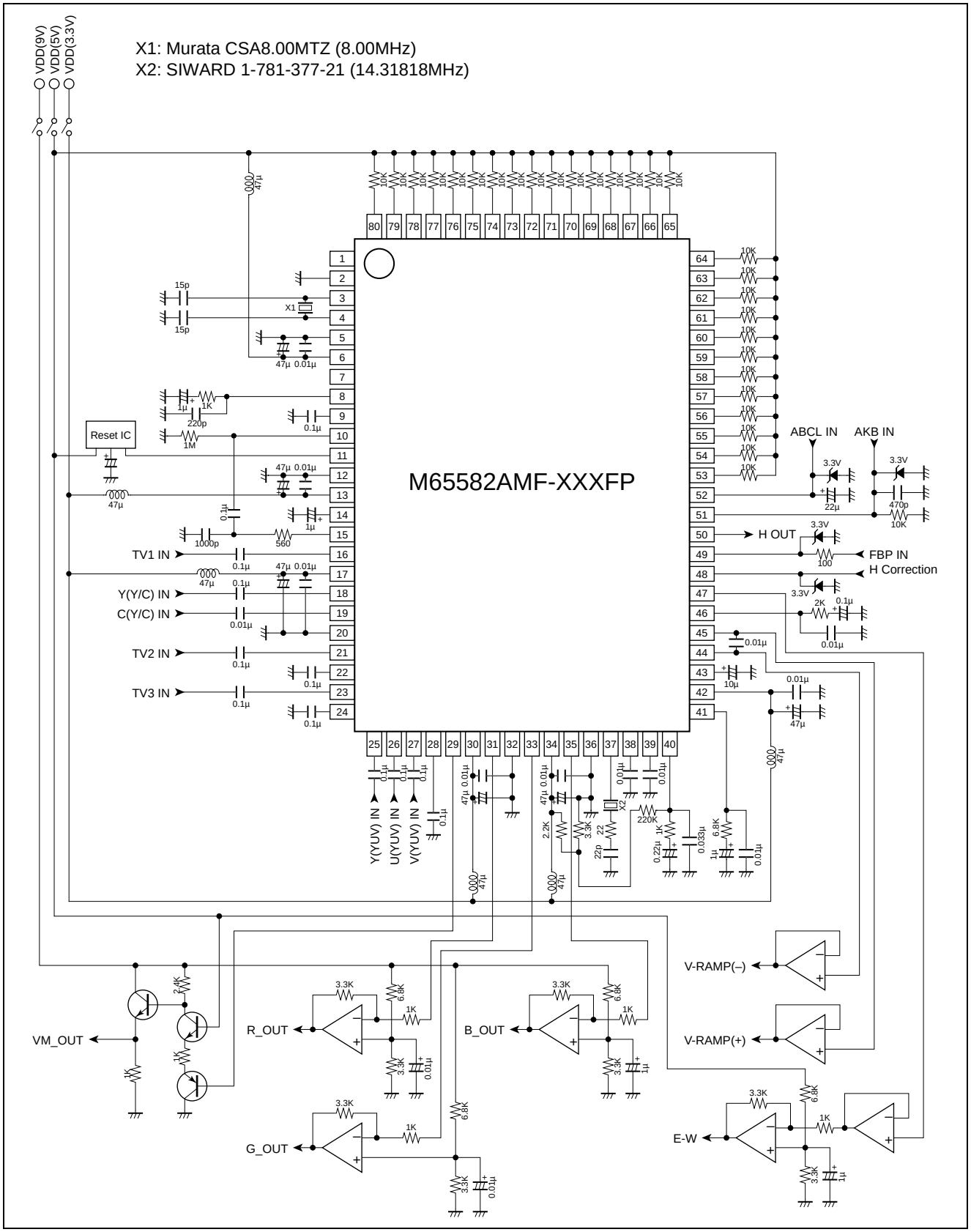


$R_{BS} = V_{BS}/I_{BS}$

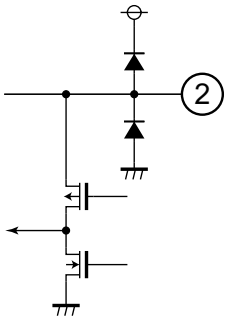
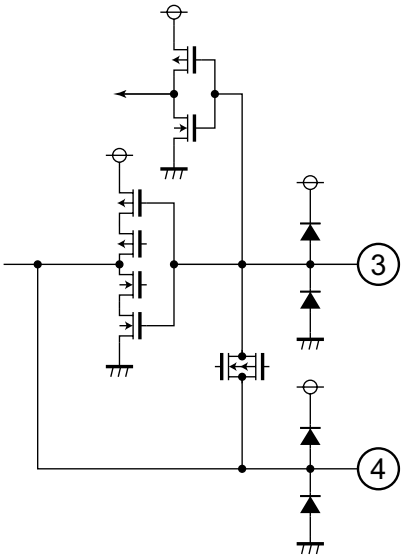
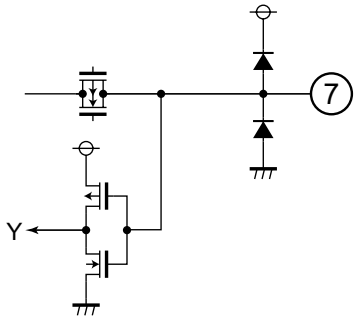
After setting each output pin OFF state, each pin is measured.
(4 , 5)

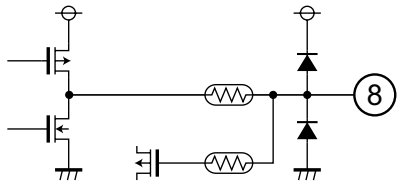
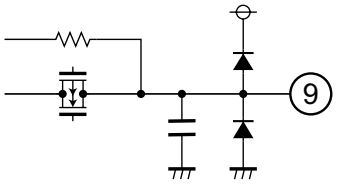
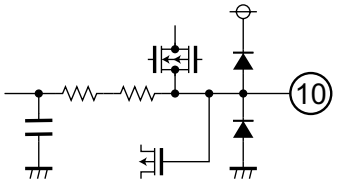
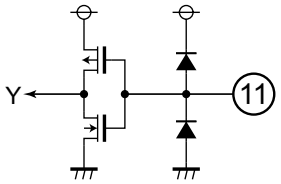
Application example

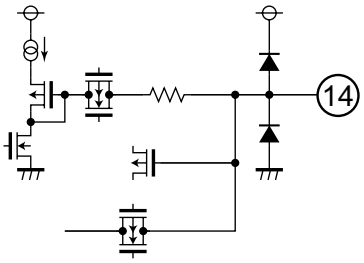
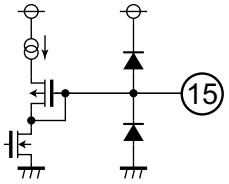
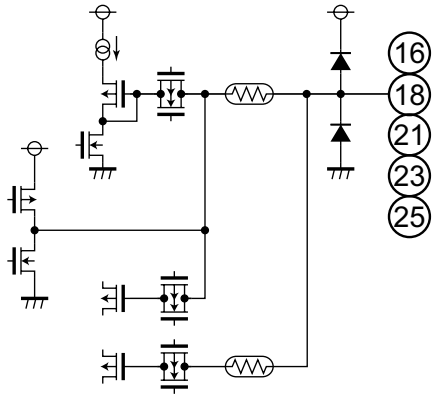
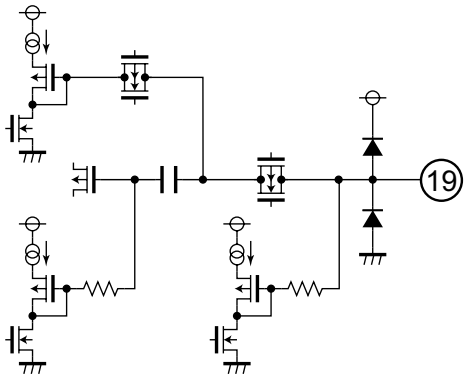
Note: If you will apply this application example to practice, please study it fully.

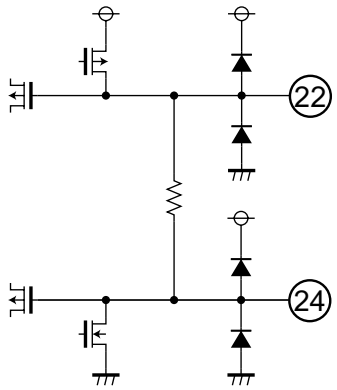
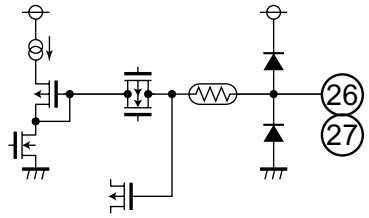
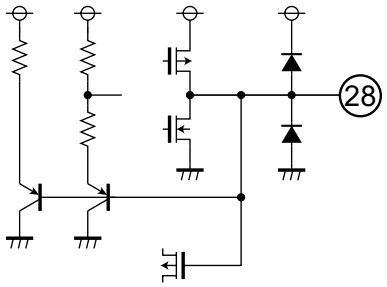
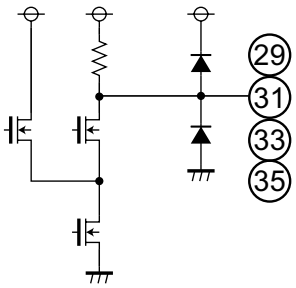


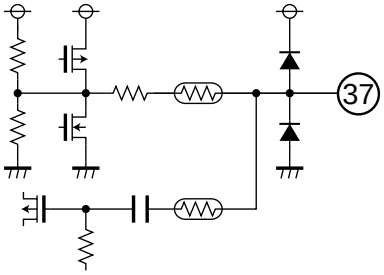
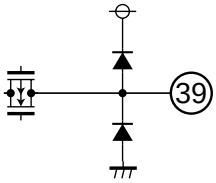
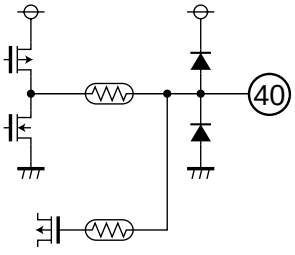
Description of Pin

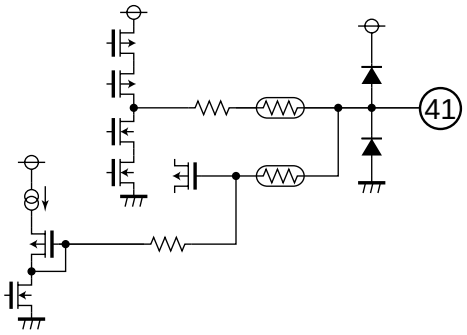
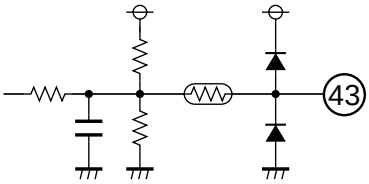
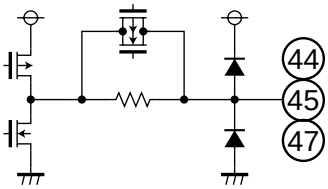
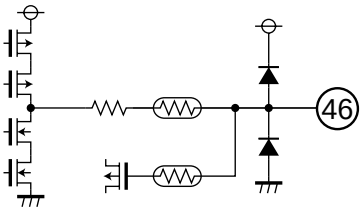
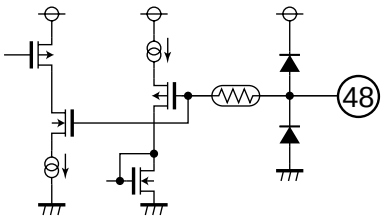
Pin No.	Name	Peripheral circuit of pins	Note
2	CN VSS		0V
3 4	X IN X OUT		
5	Vss (MCU)		Power source for MCU. 0V
6	Vdd (MCU)		Power source for MCU. 5.0V ± 5%
7	FILT		

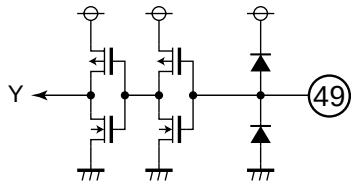
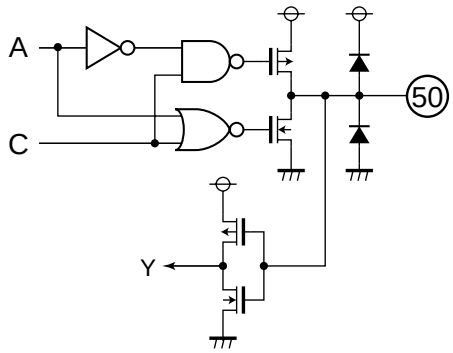
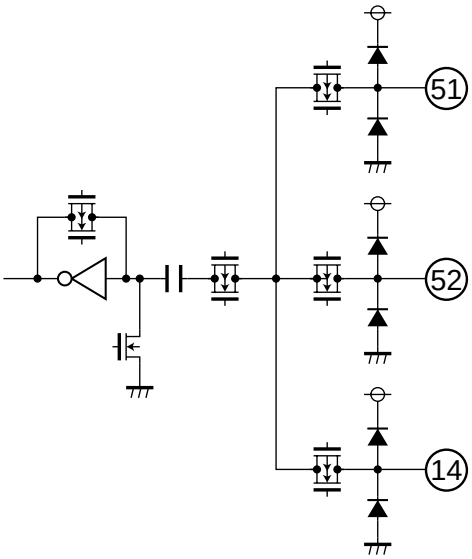
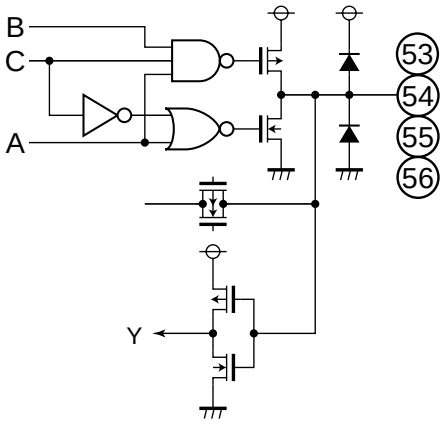
Pin No.	Name	Peripheral circuit of pins	Note
8	HLF		Impedance=N.A. (Additional filter on PCB board)
9	VHOLD		
10	CVIN		
11	RESET		CMOS INPUT (Impedance>100kΩ) V_{OL} = 0V : Reset state V_{OH} = 5V : Release from Reset state
12	Vss(Digital)		Power source for Digital blocks. 0V
13	Vdd(Digital)		Power source for Digital blocks. 3.3V ± 5%

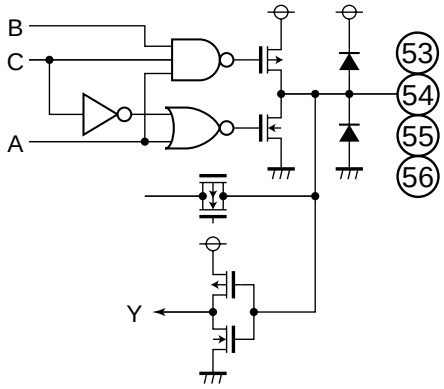
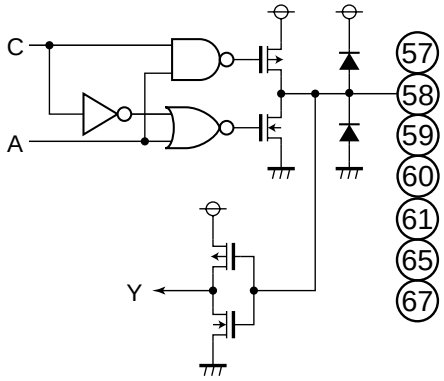
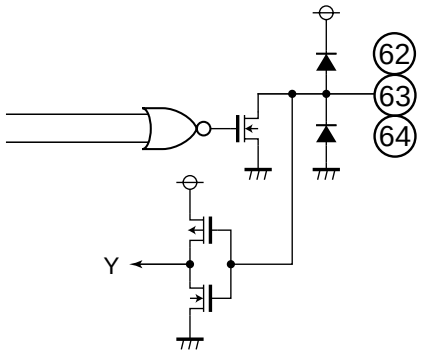
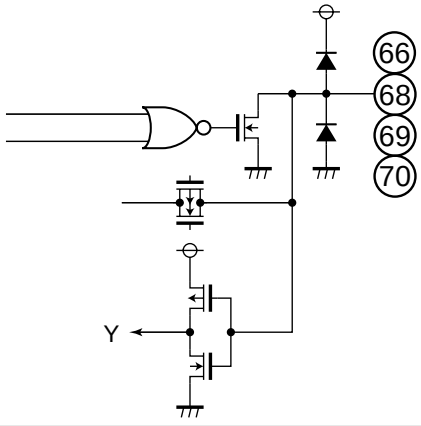
Pin No.	Name	Peripheral circuit of pins	Note
14	DCT FILTER		Impedance=N.A.
15	CVBS OUT		Impedance=150Ω DC : 0.55V (sync) AC : 1.75V_{p-p} (typ.)
16 18 21 23 25	TV1 IN Y(Y/C) IN TV2 IN TV3 IN Y(YUV) IN		Impedance=N.A. DC : 0.5V (sync) AC : 1.0V_{p-p} (typ.)
17	Vdd(Input)	———————	Power source for A/D etc. 3.3V ± 5%
19	C(Y/C) IN		Impedance=5kΩ DC : 1.0V AC : 0.286V_{p-p} (burst)

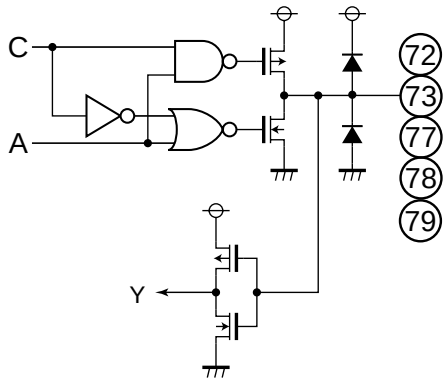
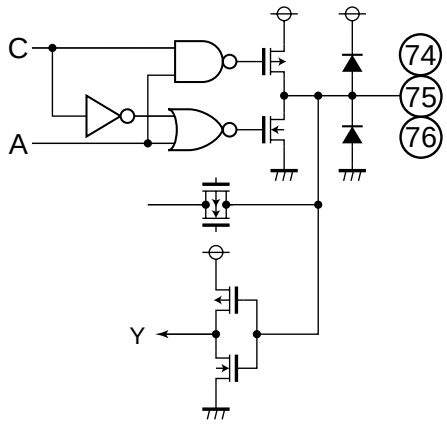
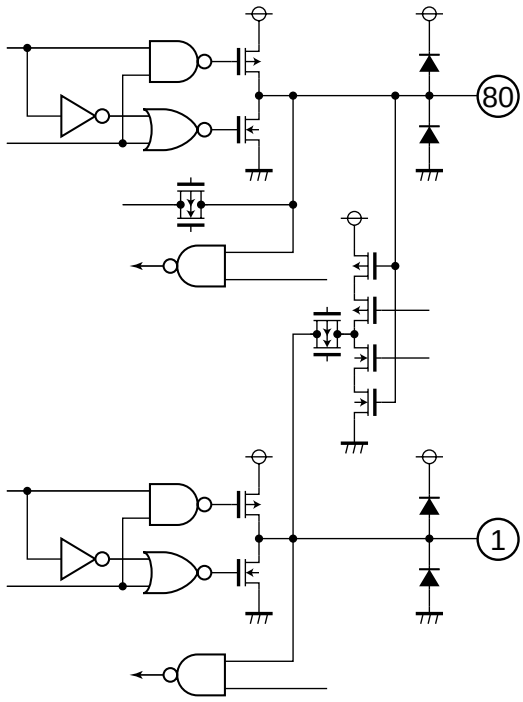
Pin No.	Name	Peripheral circuit of pins	Note
20	Vss(Input)		Power source for A/D etc. 0V
22 24	VRT VRB		Impedance=50Ω DC : 1.7V (VRT) 0.5V (VRB)
26 27	U(YUV) IN V(YUV) IN		Impedance=N.A. DC : 1.0V AC : 0.7V_{p-p} (typ.)
28	VZ OUT		Impedance=400Ω DC : 2.05V
29 31 33 35	VM R OUT G OUT B OUT		Impedance=500Ω DC : 1.65V (VM) 3V (blanking)

Pin No.	Name	Peripheral circuit of pins	Note
30	Vdd(Output)	———	Power source for D/A etc. 3.3V±5%
32	Vss(Output)	———	Power source for D/A etc. 0V
34	Vdd(VCXO)	———	Power source for VCXO etc. 3.3V±5%
36	Vss(DEF)	———	Power source for Deflection block. 0V
37	XTAL (NTSC)		Impedance≈1kΩ
38	N.C.	———	
39	TEST		Not useful (Connect 0.01μF or more capacitor externally)
40	APC FILTER		Impedance=N.A. (Additional filter on PCB board)

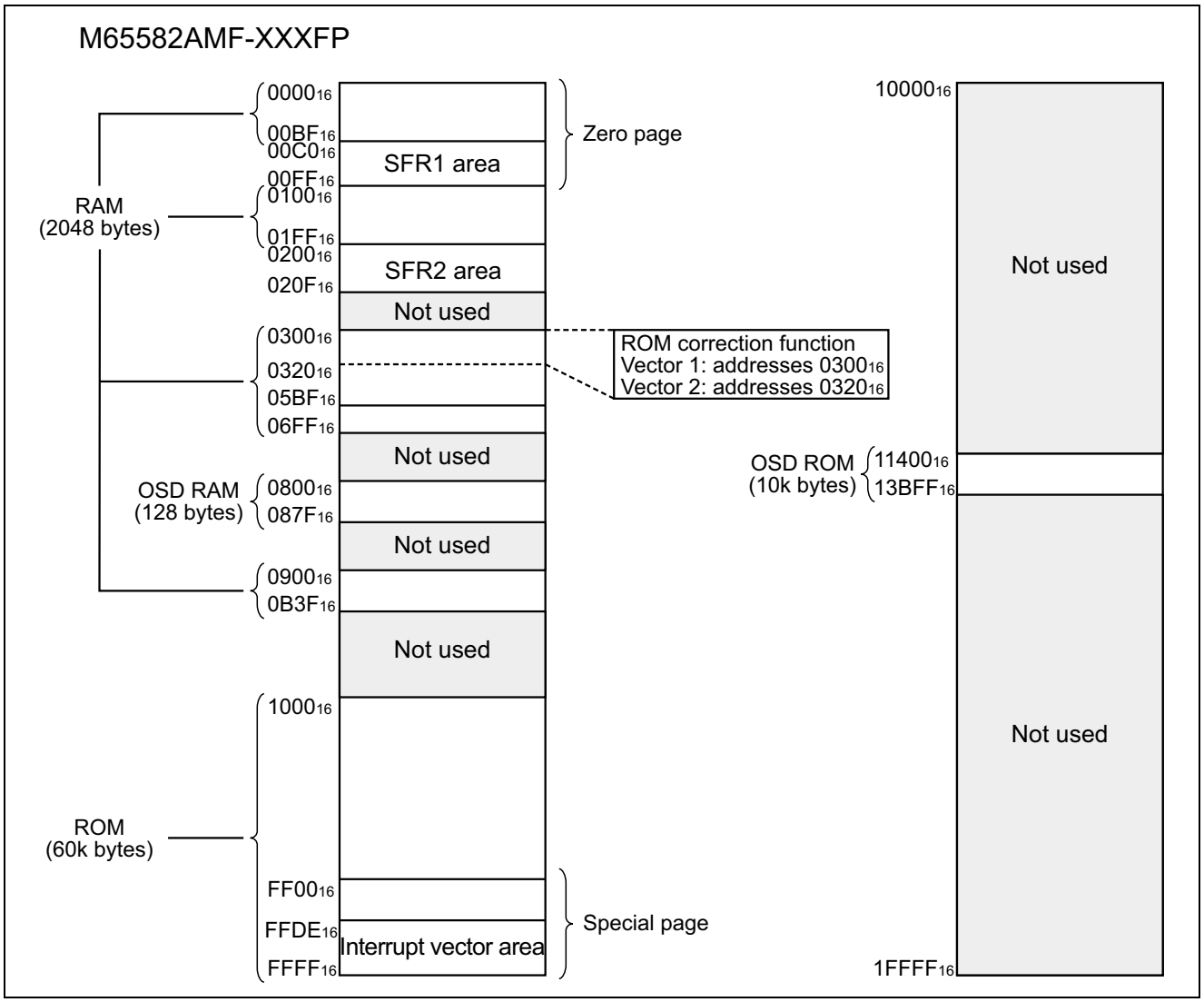
Pin No.	Name	Peripheral circuit of pins	Note
41	AFC1 FILTER		Impedance=N.A. (Additional filter on PCB board) DC : 1.65V
42	Vdd(DEF)		Power source for Deflection blocks. 3.3V±5%
43	VRAMP C		Impedance≈12.5kΩ
44 45 47	VRAMP(–) VRAMP(+) E-W		Impedance≈20kΩ AC : 1.0Vpp (typ.)
46	HVCO FB		Impedance=N.A. (Additional filter on PCB board) DC : 1.65V
48	H CORRE		Impedance>1MΩ Input voltage range : 0 to 3.3V 0V : H OUT +2.2µsec 3.3V : H OUT –2.2µsec

Pin No.	Name	Peripheral circuit of pins	Note
49	FBP IN		CMOS INPUT (Impedance>100kΩ) V_{IL}=0V : RGB output V_{IH}=3.3V : Blanlking
50	H OUT		CMOS IN/OUT 1 (Impedance>100kΩ (input) Impedance<100Ω (output))
51 52	AKB IN ACL IN		Input voltage range : 0 to 3.3V
53 54 55 56	P1$_4$/SDA2 P1$_3$/SDA1 P1$_2$/SCL2 P1$_1$/SCL1		CMOS IN/OUT 1 (Impedance>100kΩ (input) Impedance<100Ω (output))

Pin No.	Name	Peripheral circuit of pins	Note
53 54 55 56	P14/SDA2 P13/SDA1 P12/SCL2 P11/SCL1		CMOS IN/OUT 1 Impedance>100kΩ (input) Impedance<100Ω (output)
57 58 59 60 61 65 67	P40 P41 P42 P43 P10 P44 P45		CMOS IN/OUT 1 Impedance>100kΩ (input) Impedance<100Ω (output)
62 63 64 71	P00/PWM0 P01/PWM1 P02/PWM2 P07/INT1		CMOS IN/OUT Impedance>100kΩ (input) Impedance<100Ω (output)
66 68 69 70	P03/PWM3/AD1 P04/PWM4/AD2 P05/AD3 P06/INT2/AD4		CMOS IN/OUT Impedance>100kΩ (input) Impedance<100Ω (output)

Pin No.	Name	Peripheral circuit of pins	Note
72 73 77 78 79	P1$_5$ P1$_6$ P2$_3$/TIM3 P2$_4$/TIM2 P2$_5$/INT3		CMOS IN/OUT 1 (Impedance>100kΩ (input) Impedance<100Ω (output))
74 75 76	P2$_0$/SCLK/AD5 P2$_1$/SOUT/AD6 P2$_2$/SIN/AD7		CMOS IN/OUT (Impedance>100kΩ (input) Impedance<100Ω (output))
80 1	P2$_6$/XCIN P2$_7$/XCOUT		

Memory Map


M65582AMF-XXXFP
0000₁₆
00BF₁₆
00C0₁₆
00FF₁₆
0100₁₆
01FF₁₆
0200₁₆
020F₁₆
0300₁₆
0320₁₆
05BF₁₆
06FF₁₆
0800₁₆
087F₁₆
0900₁₆
0B3F₁₆
1000₁₆
FF00₁₆
FFDE₁₆
FFFF₁₆
SFR1 area
SFR2 area
Not used
Not used
Not used
Not used
Interrupt vector area
Zero page
Special page
RAM
(2048 bytes)
OSD RAM
(128 bytes)
ROM
(60k bytes)
ROM correction function
Vector 1: addresses 0300₁₆
Vector 2: addresses 0320₁₆
10000₁₆
11400₁₆
13BFF₁₆
1FFFF₁₆
Not used
OSD ROM
(10k bytes)
Not used

Package Dimensions

Plastic 80pin 14X20mm body LQFP

80P6U-A (MMP)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP80-P-1420-0.8	—		Cu Alloy

Under Planning

Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.6
A_1	0.05	0.125	0.2
A_2	—	1.4	—
b	0.32	0.37	0.47
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	19.9	20.0	20.1
e	—	0.8	—
H_D	15.8	16.0	16.2
H_E	21.8	22.0	22.2
L	0.35	0.5	0.65
L_1	—	1.0	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
x	—	—	0.2
y	—	—	0.1
θ	0°	—	8°
b_2	—	0.225	—
l_2	10	—	—
M_D	—	14.4	—
M_E	—	20.4	—

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Colophon 1.0