L64551
MIL-STD-1750A
Radiation-Hardened
MBU

Preliminary

LSI LOGIC

Description

The L64551 MBU (Memory Management and Block Protect Unit) from LSI Logic is a radiation-hardened, single-chip memory management unit which supports the L64501 CPU. While the L64501 provides the required 1750A functionality as defined in MIL-STD-1750A, the L64551 focuses on the system implementation aspects and optional features of the standard.

For example, the L64551 includes on-chip control logic and fast mapping RAMs to implement both a memory management unit (MMU) and a block protect unit (BPU). The MMU provides logical-to-physical address translation and logical protection, and the BPU provides physical block protection. Other on-chip functions include watch-dog and bus time-out timers, a memory fault status register (MFSR), multi-master bus arbitration, and an extended addressing capability for up to 8 M words of physical memory. The L64551 can interface directly with the L64501 CPU, also available from LSI Logic, to provide these optional MIL-STD-1750A enhancements and to optimize system performance.

To shorten the design cycle for L64501-based systems, L64551 MBU and L64501 CPU models are available in the LSI Logic Modular Design Environment™ or MDE™ software. The MDE software provides extensive design flexibility through its multichip and system simulation capabilities.

LSI Logic manufactures the L64551 MBU in a two-layer metal HCMOS process. The radiation-hardened L64551 operates at 25 MHz, guaranteed after exposure, over the military temperature range $-55°C$ to $125°C$, and utilizes a single $5V \pm 10\%$ power supply.

Features

- Total ionizing dose specification of 200K Rad (Si)
- No single event upset (SEU) latchup expected; test results available Q4 89
- SEU cross-section (cm^2/bit) to be determined; test results available Q4 89
- Threshold (MeV-cm^2 per milligram (LET)) to be determined; test results available Q4 89
- Guaranteed post-radiation clock frequency of 25 MHz
- MIL-STD-1750A (Notice 1) Instruction Set
- SEAFAC certification in an L64501-based system
- MMU, BPU, MFSR, timers, multi-master arbitration
- TTL-compatible interface
- MIL-STD-883C/38510 Class B and Class S screening options
- Silicon-gate epitaxial two-layer metal LMA9000 HCMOS technology
- Directly interfaces with L64501 CPU
- Available in 144-pin ceramic pin grid array (CPGA) and ceramic leaded chip carrier (CLDCC) packages
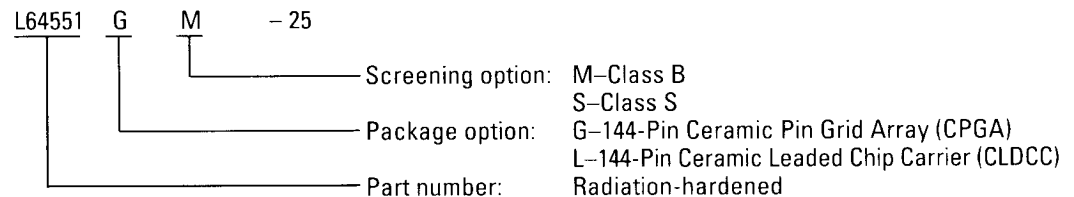
Radiation Test Data

SEU and total dose radiation data expected in Q4 89.

Technical Information

Refer to the L64500/64550 MIL-STD-1750A Microprocessor Technical Manual and datasheet, October, 1989.

Ordering Information

L64551   G   M   – 25

Screening option: M–Class B
                    S–Class S
Package option: G–144-Pin Ceramic Pin Grid Array (CPGA)
                    L–144-Pin Ceramic Leaded Chip Carrier (CLDCC)
Part number: Radiation-hardened

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